

INSTRUCTION MANUAL
MODELS 158 AND 159
PROGRAMMABLE
WAVEFORM GENERATORS
(Plus Option 159-005 Data)

WAVETEK
SAN DIEGO

9045 BALBOA AVENUE, SAN DIEGO, CALIFORNIA

INSTRUCTION MANUAL
MODELS 158 AND 159
PROGRAMMABLE
WAVEFORM GENERATORS
(Plus Option 159-005 Data)

© - 1982 - Wavetek

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO WAVETEK AND IS SOLELY FOR INSTRUMENT OPERATION AND MAINTENANCE. THE INFORMATION IN THIS DOCUMENT MAY NOT BE DUPLICATED IN ANY MANNER WITHOUT THE PRIOR APPROVAL IN WRITING OF WAVETEK.

WAVETEK®
SAN DIEGO

9045 Balboa Ave., San Diego, CA 92123
P. O. Box 651, San Diego, Calif. 92112
Tel 714/279-2200 TWX 910-335-2007

Manual Revision 7/82
Instrument Release R

WARRANTY

All Wavetek instruments are warranted against defects in material and workmanship for a period of one year after date of manufacture. Wavetek agrees to repair or replace any assembly or component (except batteries) found to be defective, under normal use, during this period. Wavetek's obligation under this warranty is limited solely to repairing any such instrument which in Wavetek's sole opinion proves to be defective within the scope of the warranty when returned to the factory or to an authorized service center. Transportation to the factory or service center is to be prepaid by purchaser. Shipment should not be made without prior authorization by Wavetek.

This warranty does not apply to any products repaired or altered by persons not authorized by Wavetek, or not in accordance with instructions furnished by Wavetek. If the instrument is defective as a result of misuse, improper repair, or abnormal conditions or operations, repairs will be billed at cost.

Wavetek assumes no responsibility for its product being used in a hazardous or dangerous manner either alone or in conjunction with other equipment. High voltage used in some instruments may be dangerous if misused. Special disclaimers apply to these instruments. Wavetek assumes no liability for secondary charges or consequential damages and, in any event, Wavetek's liability for breach of warranty under any contract or otherwise, shall not exceed the purchase price of the specific instrument shipped and against which a claim is made.

Any recommendations made by Wavetek for use of its products are based upon tests believed to be reliable, but Wavetek makes no warranty of the results to be obtained. This warranty is in lieu of all other warranties expressed or implied, and no representative or person is authorized to represent or assume for Wavetek any liability in connection with the sale of our products other than set forth herein.

CONTENTS

SECTION 1	INTRODUCTION	
	1.1 MODEL 158	1-1
	1.2 MODEL 159	1-1
	1.3 INTERFACE	1-1
	1.4 OPTIONS	1-1
	1.5 ACCESSORIES	1-1
	1.6 PHYSICAL DESCRIPTION	1-1
	1.7 SPECIFICATIONS	1-1
SECTION 2	INSTALLATION AND INTERFACE	
	2.1 MECHANICAL INSTALLATION	2-1
	2.2 ELECTRICAL INSTALLATION	2-1
SECTION 3	OPERATION	
	3.1 INITIAL CHECKOUT	3-1
	3.2 CONTROLS, INDICATORS AND PROGRAMMING	3-1
	3.3 OPERATING PROCEDURE	3-3
SECTION 4	CIRCUIT DESCRIPTION	
	4.1 LOGIC NOTATION AND TERMINOLOGY	4-1
	4.2 BASIC OPERATION	4-1
	4.3 INPUT/OUTPUT	4-1
	4.4 INTERFACE	4-1
	4.5 KEYBOARD	4-1
	4.6 DIGITAL BOARD CONTROL LOGIC	4-3
	4.7 FREQUENCY D/A LOGIC	4-5
	4.8 OFFSET D/A LOGIC	4-5
	4.9 AMPLITUDE D/A LOGIC	4-5
	4.10 DIGITAL BOARD DISPLAY (DRIVER) LOGIC	4-6
	4.11 DISPLAY LOGIC	4-6
	4.12 ANALOG BOARD	4-7
SECTION 5	CALIBRATION	
SECTION 6	TROUBLESHOOTING	
	6.1 CORRECTIVE MAINTENANCE	6-1
	6.2 TROUBLESHOOTING TECHNIQUES FOR INDIVIDUAL COMPONENTS	6-1
SECTION 7	PARTS LISTS AND SCHEMATIC DIAGRAMS	
APPENDIX A	GPIB, OPTION 005	A-1

SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

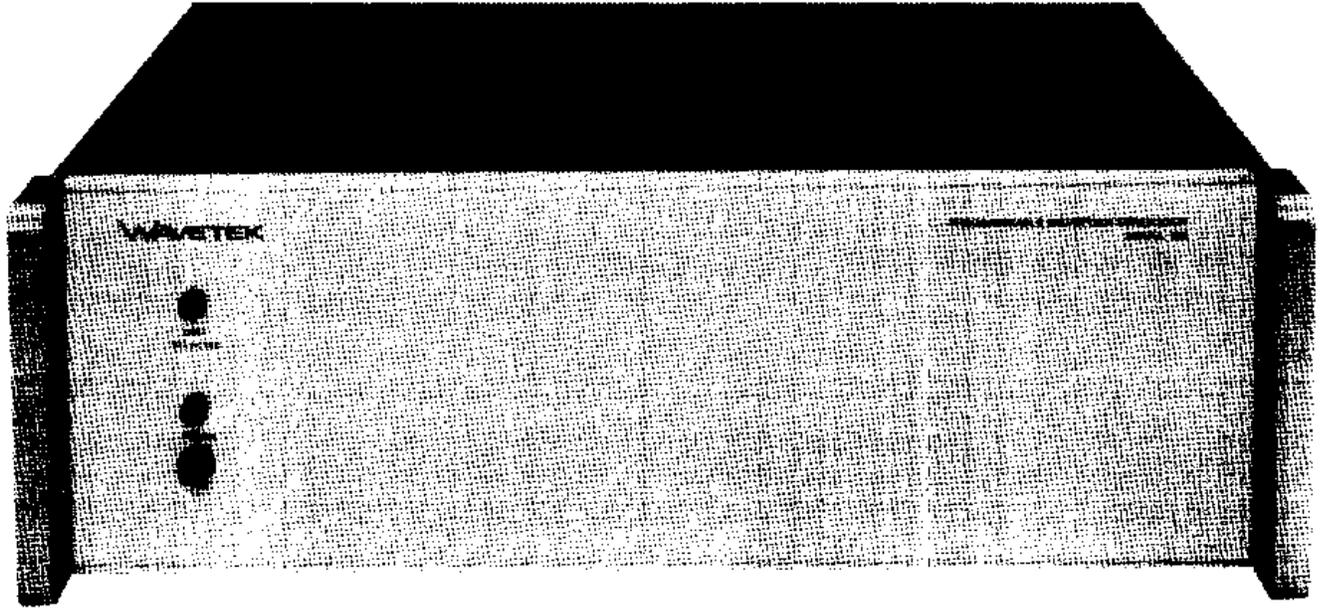
BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

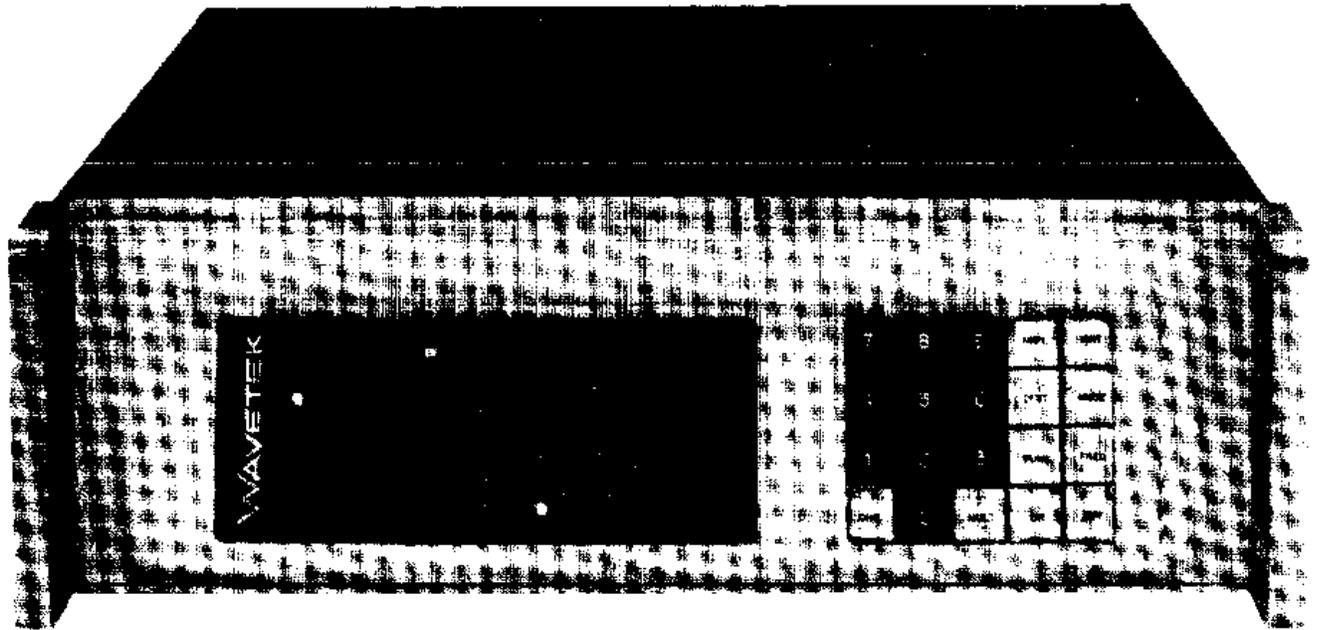
The instrument power receptical is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference:  or  stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.



Wavetek Model 158 Programmable Waveform Generator



Wavetek Model 159 Programmable Waveform Generator

Figure i – Model 158 and 159 Programmable Waveform Generators

1

SECTION

INTRODUCTION

1.1 MODEL 158

The Wavetek Model 158 Waveform Generator is a remote-control only Model 159 generator (without front panel controls and indicators). All information on the Model 159 generator also pertains to the Model 158 generator except local operation.

1.2 MODEL 159

The Wavetek Model 159 Waveform Generator is digitally controlled locally with front panel, keyboard pushbuttons, and remotely with a selection of 21 ASCII (7-level) "typing" characters (with appropriate external interface). The effect of each control is digitally displayed on the front panel with red LED (light emitting diode) indicators. Numeric readout of frequency, offset and amplitude is in 3-digit scientific notation.

Sine, triangle, square, and ramp waveforms of frequencies from 1 Hz to 3 MHz and amplitudes from 10 mV p-p to 10V p-p can be generated. Waveform generation can be continuous, triggered for just one cycle at a time, or gated for as many cycles or for as long as desired. Waveform center reference levels can be offset positive or negative from 10 mV to 5V and waveform phase, or polarity, can be inverted (180 degrees).

Along with the main 50 ohm output at the rear panel, which is the controlled waveform signal output, the generator delivers a square wave of the selected frequency for a synchronizing pulse output.

Analog inputs are received at the rear panel for a triggering input for triggered and gated operations, and a voltage controlled generator (VCG) input for frequency proportional to input dc levels. The 50Ω OUT signal can be swept in a 1000:1 frequency ratio, frequency modulated or dc programmed by the VCG input. The trigger and gate modes can be used for pulse output, one cycle output or tone bursts.

Up to nine generators can be connected in parallel with one another as a multiple unit group. Each generator is internally configured with its own address, or unit select code, from 1 to 9. For example, an installation may have one

master display and keyboard panel, which is used to address and command the slave generators. The status of the addressed generator would be displayed.

1.3 INTERFACE

The generator accepts TTL ground true 7-bit ASCII "typing" characters serially; the 7 bits of each character are accepted in parallel. A clock line in parallel with the data bits is used to clock in the data characters. Computer control is accepted as is keyboard control from another generator in multiple unit groups. With computer control, the generator keyboard control panel can be locked out, or disabled, to prevent control competition.

1.4 OPTIONS

Several interface options are available for the Model 158 and 159 generators. They include input isolation, RS232 and IEEE 488 compatible data converters.

1.5 ACCESSORIES

Accessories for the generators include interfaces for several mini-computers.

1.6 PHYSICAL DESCRIPTION

The mechanical characteristics of the Models 158 and 159 are given in Paragraph 1.7.8. The standard models come equipped with a 10 foot, 3 wire detachable power cord and rack mount adapters. Interface cabling requires Molex brand connectors (see Paragraph 2.2.3); one is furnished.

1.7 SPECIFICATIONS

1.7.1 Versatility

Waveforms

Sine , triangle , square , ramp  (50% duty cycle), and auxiliary TTL sync pulse. All selectable waveforms may be inverted.

Frequency Range

Sine, triangle, and square from 1 Hz to 3 MHz in 7 ranges with 3-digit resolution.

10^0	1 Hz to 9.99 Hz
10^1	10 Hz to 99.9 Hz
10^2	100 Hz to 999 Hz
10^3	1 kHz to 9.99 kHz
10^4	10 kHz to 99.9 kHz
10^5	100 kHz to 999 kHz
10^6	1 MHz to 3 MHz

Ramp from 1 Hz to 1 MHz in 6 ranges ($10^0 \rightarrow 10^5$).

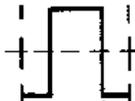
NOTE

Generator is usable from 0.01 Hz with derated accuracies.

Main Output

Three digits of amplitude from 10 mV to 10V p-p into 50Ω (20V p-p into an open circuit) in 3 ranges (10^0 , 10^1 , 10^2).

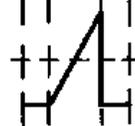
SQUARE
AND
SYNC



TRIANGLE



RAMP



SINE



NORMAL PHASE RELATIONSHIPS

DC Offset

Three digits of dc offset to $\pm 5V$ into 50Ω . DC offset plus waveform peak value may not exceed 10V peak into open circuit or 5V peak into 50Ω .

Sync Output

A TTL compatible 0 to 2.5V square wave output, which provides 50 mA sinking current to sync up to 30 TTL loads.

Data Entry

Front panel keyboard/display and remote programming (Model 159).

Remote programming only (Model 158).

1.7.2 Operational Modes

Continuous, triggered, and gated operation provided. In triggered mode, one cycle of selected signal output for each input trigger signal. In gated mode, signal output at selected frequency for duration of the input gate plus completion of the last cycle. Model 159 has front panel manual trigger.

Trigger/Gate Signal

Minimum	+2V
Maximum	50V
Input Impedance	1 k Ω

1.7.3 Analog Modulation Control

Frequency may be externally controlled by analog voltage (VCG) providing dc programming for FSK or wide band ac modulation. Input impedance is 5 k Ω .

VCG Control Signal

Approximately 2.5V	1000:1 frequency change
Approximately 7.5V	3000:1 frequency change (300% overrange in first 6 ranges)

VCG Small Signal Bandwidth

100 kHz

VCG Slew Rate

4% of range per μs

1.7.4 Accuracy

Horizontal Precision (Frequency Accuracy)

10 Hz to 100 kHz	$\pm 1\%$ of program value ± 1 digit
100 kHz to 1 MHz	$\pm 2\%$ of program value ± 1 digit
1 MHz to 3 MHz	$\pm 4\%$ of program value ± 1 digit

Vertical Precision (Amplitude Accuracy)

NOTE

Vertical precision stated is for 10^0 amplitude multiplier. For 10^1 and 10^2 , add 1% per step.

Vertical Precision (Amplitude Accuracy) (Continued)

Sine and Square Waveforms:

- 10 Hz to 100 kHz . . . ±2% of program value ±1 digit
- 100 kHz to 1 MHz . . . ±5% of program value ±1 digit

Triangle and Ramp Waveforms:

- 10 Hz to 10 kHz . . . ±2% of program value ±1 digit

DC Offset

±2% of program value ±1 digit

Sine Wave Frequency Response

Amplitude change with frequency less than:

- 0.1 dB to 100 kHz
- 0.5 dB to 1 MHz
- 1.0 dB to 3 MHz

Stability

- Short term ±0.05% for 10 minutes
- Long term ±0.25% for 24 hours

1.7.5 Purity

Sine Wave Distortion

Total harmonic distortion less than:

- 0.5% to 30 kHz ranges 10⁰ thru 10³
- 1.0% to 300 kHz ranges 10⁰ thru 10⁴

All harmonics:

34 dB down to 1 MHz

Time Symmetry

1% to 100 kHz

Amplitude Symmetry

All waveforms to 100 kHz are symmetrical about ground within 1% of maximum p-p amplitude.

Triangle Linearity

Greater than 99% to 100 kHz

Square Wave Rise and Fall Time

Less than 50 ns

Total Aberrations

Less than 5% of program value ±20 mV

1.7.6 Programming

Programming Transition Time

Unit accepts bytes at a 1 MHz rate. The output will become stable within 100 μs unless the range digit is changed; then output will be stable within 1 ms.

Isolation

Signal ground and program ground are common in the standard 158/159. Optical isolation is available.

Logic Level Requirements

State	Requirements
Low (Logic "1")	0V to 0.4V sinking 25 mA maximum
High (Logic "0")	2.4V or open

NOTE

1. Open input is 3.0V.
2. Input is terminated by 220Ω to +5V and 330Ω to ground.
3. Recommended driver: SN 7438.

Input Control Lines and Connector Layout

Mating Connector: Molex 03-09-2151 with 02-09-2118 pins

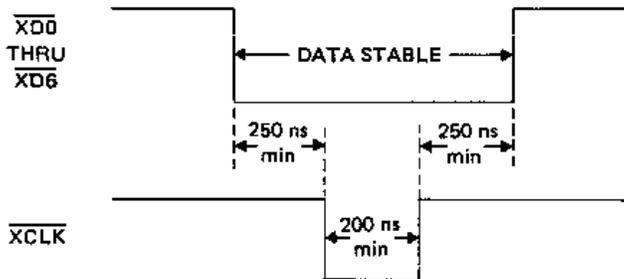
J9 Pin No.	Designation
13	XD0 } Least significant bit XD1 } XD2 } Input data lines XD3 } XD4 } XD5 } XD6 } Most significant bit
11	
8	
10	
9	
12	
14	XCLK Clock control
15	Common
7	Common
3	Keyboard Enable
1	Keyboard Enable Return

Keyboard to ASCII Conversion Table

Keyboard	ASCII	Keyboard	ASCII
AMPL	A	MULT	(Space) or E
UNIT	G	ON	H
OFST	D	OFF	I
MODE	B	0 thru 9	0 thru 9
FUNC	C	CHS	- (Minus)
FREQ	F		

Timing

Direct (No Isolation)



1.7.7 Environmental

Specifications apply for 25°C ±5°C. For operation from 0°C to +55°C, derate all specifications by a factor of 2. Unit may be stored from -40°C to +75°C without damage.

1.7.8 Mechanical

May be used on the bench or in a 19 inch rack. Rack adapter hardware and program mating connectors included.

Dimensions

17¼ in./43.8 cm wide, 5¼ in./13.3 cm high, 17 in./43.2 cm deep.

Weight

15 lb/6.8 kg net, 23 lb/10.4 kg shipping.

Power

90 to 110V, 105 to 125V, 180 to 220V, or 210 to 250V;
50 to 400 Hz. Less than 45 watts.

NOTE

Specifications apply for settings from 1.00 to 9.99

SECTION 2

INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The standard generator is a bench-top instrument with a collapsible tilt-bail to elevate its front end for convenient viewing.

The generator can also be rack mounted by attaching the rack mount adapters to the sides.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 105 - 125 Vac line supply and with a 3/4 amp slow-blow fuse.

Conversion for 90 to 110V, 180 to 220V, or 210 to 250V operation requires resetting two switches on the inside of the rear panel. To reset the switches, remove the top cover for access. Set the two switches and select the fuse for the ac line voltage according to the following table.

AC Line Voltage	Switch A	Switch B	Fuse (SB)
90 - 110	115	LO	3/4 amp
105 - 125	115	HI	3/4 amp
180 - 220	230	LO	3/8 amp
210 - 250	230	HI	3/8 amp

Connect the ac line cord to the mating connector at the rear of the unit.

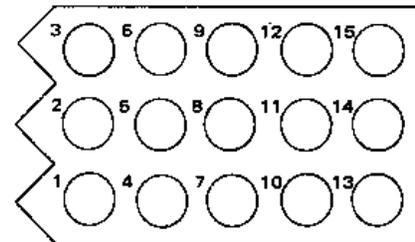
2.2.2 Signal Connections

Use 50Ω shielded cables equipped with female BNC connectors to distribute 50Ω OUT, SYNC OUT, TRIG IN and VCG IN signals when connecting this instrument to associated equipment.

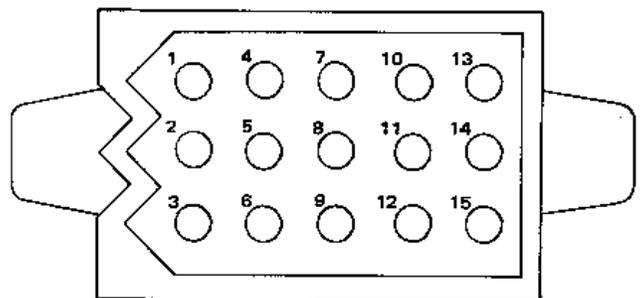
2.2.3 Control Connections

The remote (ASCII DATA IN/OUT) rear panel connection, harness wire colors, pin connections and signal names are given in Tables 2-1 and 2-2.

The remote connector is a Molex 03-09-1151 which mates with a Molex 03-09-2151 connector housing with up to 15 Molex 02-09-2118 pin contacts. Pin contacts are prepared using a Molex Model A6973 Crimping Tool to connect No. 18 or No. 22 wire (strip back 1/10 to 1/8 inch).



MOLEX 03-09-1151



MOLEX 03-09-2151

Figure 2-1. Connectors (Socket/Pin Sides)

Table 2-1. ASCII DATA IN/OUT AND HARNESS CONNECTORS

Pin	Connector						Code	Color	Code	Color
	ASCII Data In/Out (Rear Panel)		Keyboard Harness		Display Harness					
	Wire Color	Signal	Wire Color	Signal	Wire Color	Signal				
1	1	PCOM						8	Gray	
2	2							9	White	
3	3	KINH	2	KINH				90	White with black tracer	
4			1	+5V	7	+5V		91	White with brown tracer	
5	5							92	White with red tracer	
6	6	BUSY						93	White with orange tracer	
7	7	COM	91	COM	0	COM		94	White with yellow tracer	
8	8	XD2	8	KD2	1	DCLK		95	White with green tracer	
9	9	XD4	5	KD4						
10	90	XD3	3	KD3	2	DD0				
11	91	XD1	7	KD1	4	DD2				
12	92	XD5	4	KD5						
13	93	XD0	90	KD0	6	DSYNC				
14	94	XD6	6	KD6	3	DD3				
15	95	XCLK	9	KCLK	5	DD1				

PCOM:	Input Program Common
KINH:	Keyboard Inhibit (When connected to pin 7)
COM:	Signal Common
X:	External
D:	Data
0 - 6:	Bits 0 thru 6
CLK:	Clock
K:	Keyboard
D:	Display

Table 2-2. KEY, ASCII, HEXADECIMAL, AND BINARY CODES FOR PROGRAMMING FUNCTIONS

Control and Data Names	Model 159 Key	ASCII Character and TTY Keyboard	Hexa-Decimal Code	Binary (and ASCII Bus)						
				XD6 Bit 7	XD5 Bit 6	XD4 Bit 5	XD3 Bit 4	XD2 Bit 3	XD1 Bit 2	XD0 Bit 1
				Range (X 10 mult)*	(Space)	20	0	1	0	0
Invert phase/offset	CHS	-	2D	0	1	0	1	1	0	1
0	0	0	30	0	1	1	0	0	0	0
1	1	1	31	0	1	1	0	0	0	1
2	2	2	32	0	1	1	0	0	1	0
3	3	3	33	0	1	1	0	0	1	1
4	4	4	34	0	1	1	0	1	0	0
5	5	5	35	0	1	1	0	1	0	1
6	6	6	36	0	1	1	0	1	1	0
7	7	7	37	0	1	1	0	1	1	1
8	8	8	38	0	1	1	1	0	0	0
9	9	9	39	0	1	1	1	0	0	1
P-P amplitude	AMPL	A	41	1	0	0	0	0	0	1
Operating mode	MODE	B	42	1	0	0	0	0	1	0
Function (waveform)	FUNC	C	43	1	0	0	0	0	1	1
Reference offset	OFST	D	44	1	0	0	0	1	0	0
Range (X 10 mult)*	MULT	E	45	1	0	0	0	1	0	1
Frequency	FREQ	F	46	1	0	0	0	1	1	0
Unit select address	UNIT	G	47	1	0	0	0	1	1	1
Output on	ON	H	48	1	0	0	1	0	0	0
Output off	OFF	i	49	1	0	0	1	0	0	1

1 = True = Low
0 = False = High

*See the second entry of this control name.

3.1 INITIAL CHECKOUT

To ensure that the generator is operating properly, make the power and interface connections (Section 2), and operate the generator, function-by-function, as described in the following paragraphs.

3.2 CONTROLS, INDICATORS AND PROGRAMMING

Programming instructions and considerations for the Model 158 and 159 generators are the same, except for keyboard enable control that only applies to the Model 159 generator.

The Model 159 has a 20-pushbutton front panel keyboard to provide the same control as the Model 159 or 158 20 remotely programmed ASCII character bytes.

The 20 generator controls and their various code conversions are listed in Table 2-2. The Model 159 front panel controls and indicators are shown in Figure 3-1.

3.2.1 Power

Power is turned on and off with the PWR pushbutton. When the power is turned on, the generator is automatically addressed and is ready to accept commands. If a different generator is to be addressed, use the UNIT control (refer to Paragraph 3.2.4). Also, when the power comes on, the output is automatically disabled to allow the loading of a program; line transients on the output are also avoided. The generator must get an ON command to provide an output (refer to Paragraph 3.2.5).

3.2.2 Indicators

The Model 159 indicators turn on to indicate the various functions, modes, quantities, sign, and address programmed; the numerals displayed are significant as frequency, amplitude or offset, but only one category at any one time. The 3-digit number is always a 1-digit whole number and a 2-digit decimal. The three digits are displayed in order of entry, shifting right-to-left as shown in Table 3-1. The single digit is a power of ten. (Only the last three entered significant

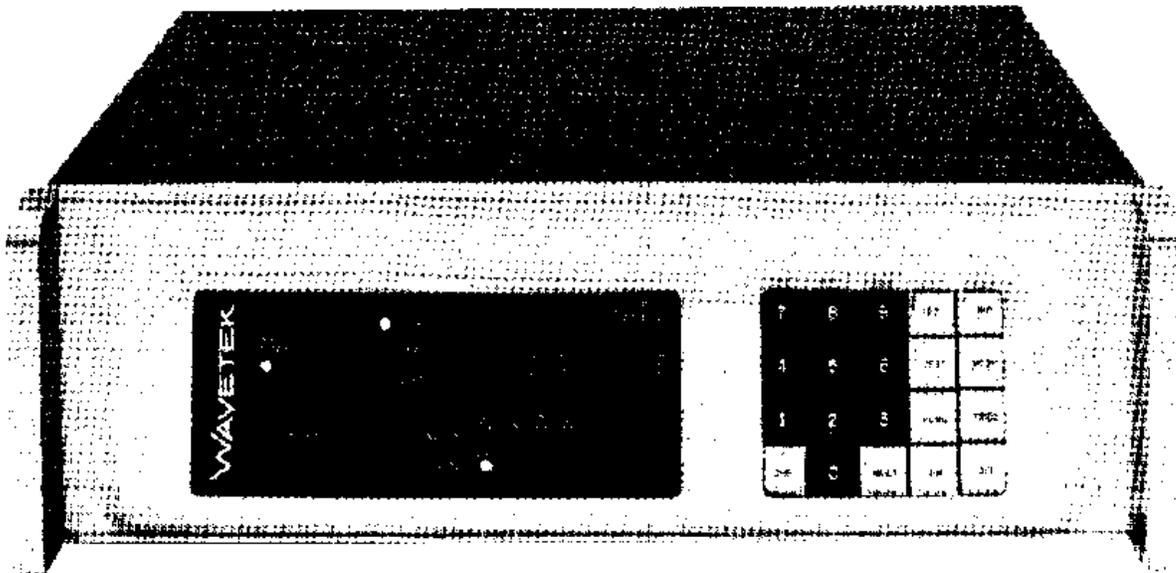


Figure 3-1. Model 159 Waveform Generator

digits and the last entered digit for the power of ten are stored. Any previously entered digits of the significant digits or the power of ten are shifted out of memory.)

3.2.3 Programming

Programming is mostly a matter of prefixing, by sequence, the numerical values and numeric codes with their intended use. For example, programming a continuous 5.79 kHz sine wave on Unit No. 1 is given in Table 3-1.

Table 3-1. EXAMPLE OF PROGRAMMING

Sequence	Wavetek Keyboard	Remote ASCII	Lighted Display
1	UNIT	G	---
2	1	1	SELECT
3	MODE	B	---
4	0	0	CONT
5	FUNC	C	---
6	0	0	~
7	FREQ	F	---
8	5	5	0.05
9	7	7	0.57
10	9	9	5.79
11	MULT	E	---
12	3	3	3 (power of ten)

Table 3-2. KEYBOARD TO ASCII CONVERSION TABLE

Keyboard	ASCII	Keyboard	ASCII
AMPL	A	MULT	{Space} or E
UNIT	G	ON	H
OFST	D	OFF	I
MODE	B	0 thru 9	0 thru 9
FUNC	C	CHS	- (Minus)
FREQ	F		

Generally, alpha characters (A thru I) are subsection addresses and are usually followed by one or more numeric digits representing a value or control selection.

NOTE

Any character may be separated by spaces, periods or other characters not defined here. Spaces may be inserted between alpha control characters and numeric fields; however, a space will move from a value field to the exponent field where scientific notation is used after at least one numeric digit has been received. (See Paragraphs 3.2.8 and 3.2.9.)

The generators are designed to accept a scientific notation input format. System programmers using FORTRAN will find that the result of the format statement

20 FORMAT (1 HF, 1PE13.3)

will control the frequency without additional processing.

The following paragraphs describe the program elements and give their ASCII codes. The Model 159 front panel keys correspond one-for-one with the ASCII codes; if there is any doubt as to correspondence, refer to Table 3-2.

3.2.4 Unit Selected Address

After the unit prefix (G), program one digit to select the unit. The unit addressed in a multiple-unit group responds to subsequent commands; other units do not. Generators are given the address of 1 at the factory unless specified otherwise at the time of purchase. Address changes are easily made in the field. Subsequent instructions will be accepted by the last unit addressed.

3.2.5 Output On/Off

The generator output is enabled by programming H and inhibited by programming I. H and I connect and disconnect the generator output to the external BNC connector.

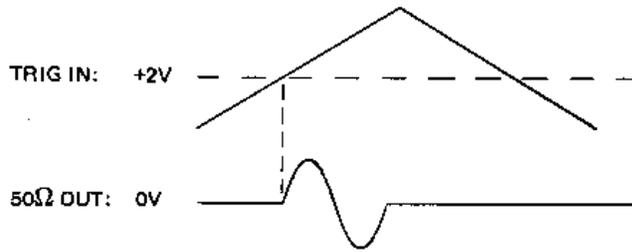
3.2.6 Operating Mode

Operating Mode	ASCII Character
Continuous	0
Triggered	1
Gated	2

After the mode prefix (B), program one digit to select the desired mode.

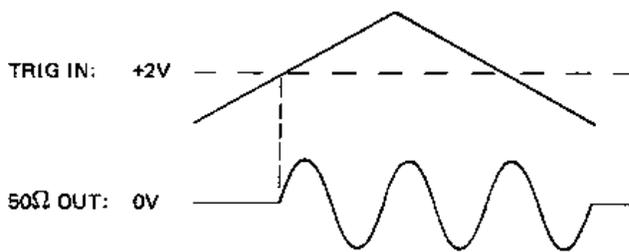
The generator output can be made to run continuously, triggered for just one cycle of waveform at a time, or gated for as many cycles or for as long as desired.

The triggered and gated modes require an external trigger level input at rear panel connector TRIG IN of at least +2V, not to exceed +50V; inputs below +2V are not to exceed -50V. In the triggered mode, one cycle of waveform is generated whenever the input at TRIG IN increases positively thru +2V.



In triggered mode, the generator may be "manually" triggered by pressing the "1" key or programming an ASCII 1.

In the gated mode, waveforms are generated for as long as the input at TRIG IN stays above +2V. When the input at TRIG IN falls below +2V, the last cycle of waveform is completed and the waveform stops.



3.2.7 Function (Waveform)

Waveform	ASCII Character
Sine	0
Triangle	1
Square	2
Ramp	3

After the function prefix (C), program one digit to select the desired waveform. Waveforms can be inverted during amplitude selection.

3.2.8 Frequency and Multiplier

After the frequency prefix (F), program a 3-digit number (1.00 to 9.99) for the three most significant digits; after the multiplier prefix (E or space), program the power of 10 (0 thru 6).

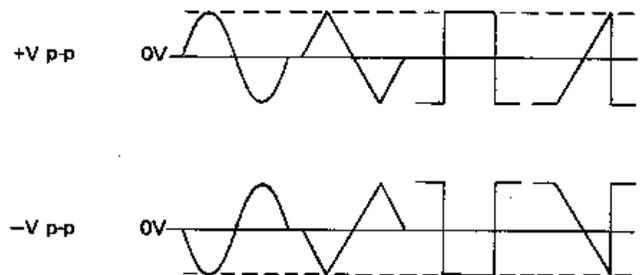
3.2.9 Amplitude and Multiplier

After the amplitude prefix (A), program (-) if waveform inversion is desired; then, program a 3-digit number (0.00 to 9.99) for the three most significant digits. After the multiplier prefix (E or space), program the power of 10 (0, 1 or 2). Powers 1 and 2 are automatically accepted as -1 and -2. Amplitude is volts peak-to-peak into a 50Ω load.

NOTE

DC offset plus waveform peak value may not exceed 10V peak into an open circuit or 5V peak into 50Ω.

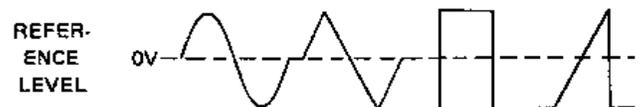
All waveforms including ramp have a center reference level. Notice the inversion caused by programming -V p-p. Normal waveforms start in the positive direction regardless of their offset. Inverted waveforms start in the negative direction regardless of their offset.



3.2.10 Signal Reference Offset

After the offset prefix (D), program (-) if negative offset is desired; then, program a 3-digit number (0.00 to 5.00) for the offset significant digits. The offset multiplier, or range, is the amplitude program multiplier. For example, if A150E1 and D350 are programmed, the waveform will be +0.15V p-p with an offset of +0.35V.

Offset control allows the generator output reference level to be offset, or displaced positive or negative to 5V. All waveforms including ramp have a center reference level from which the offset is made.



NOTE

DC offset plus waveform peak value may not exceed 10V peak into an open circuit or 5V peak into 50Ω.

3.3 OPERATING PROCEDURE

No preparation for operation is required beyond the completion of the initial installation checks. Allow the generator and associated equipment to warm up for specified generator accuracies. Refer to the control descriptions given in Paragraph 3.2 for actual keyboard or remote commands.

3.3.1 Operating as a Basic Waveform Generator

1. Terminate the 50Ω OUT connector with a 50Ω ±0.1% termination.
2. Select the desired waveform and continuous mode.
3. Select the desired frequency, output amplitude and offset.

NOTE

DC offset plus waveform peak value may not exceed 10V peak into an open circuit or 5V peak into 50Ω. Specifications apply for frequency and amplitude programs from 1.00 to 9.99.

3.3.2 Operating as a Voltage Controlled Generator

VCG operation is the same as the basic waveform operation plus the connection of a VCG voltage source to the VCG IN connector. Input impedance is 5 kΩ.

The VCG input can be used to externally control the frequency of the 50Ω OUT signal. A positive voltage applied to the VCG IN connector will increase the generator frequency, and a negative voltage will decrease the frequency. A 2.5V excursion can vary the frequency by a factor of 1000, and a 7.5V excursion will allow 300% overranging, as shown in the following table.

Range	1:3000 (300% Overrange)
10 ⁰	0.01 Hz to 30 Hz
10 ¹	0.1 Hz to 300 Hz
10 ²	1 Hz to 3 kHz
10 ³	10 Hz to 30 kHz
10 ⁴	100 Hz to 300 kHz
10 ⁵	1 kHz to 3 MHz

The nomograph of Figure 3-2 shows the characteristics of the VCG circuit. Column A gives the 3-digit program setting; column B, the VCG IN voltage; and column C, the factor representing the resultant frequency of the generator (multiply by range for actual frequency). As an example of nomograph use, suppose you want to operate at a basic frequency of 350 kHz and vary the frequency by VCG voltage from 100 kHz to 2 MHz. Mark the 3.50 3-digit program setting in column A on the nomograph. Draw a

line to each of the frequency limits in column C, 20.0 and 1.00. In the VCG IN Voltage column, the voltage range defined by these two lines is the VCG IN operating range. In the example, the VCG voltage range is from -0.60 to 4.15 volts.

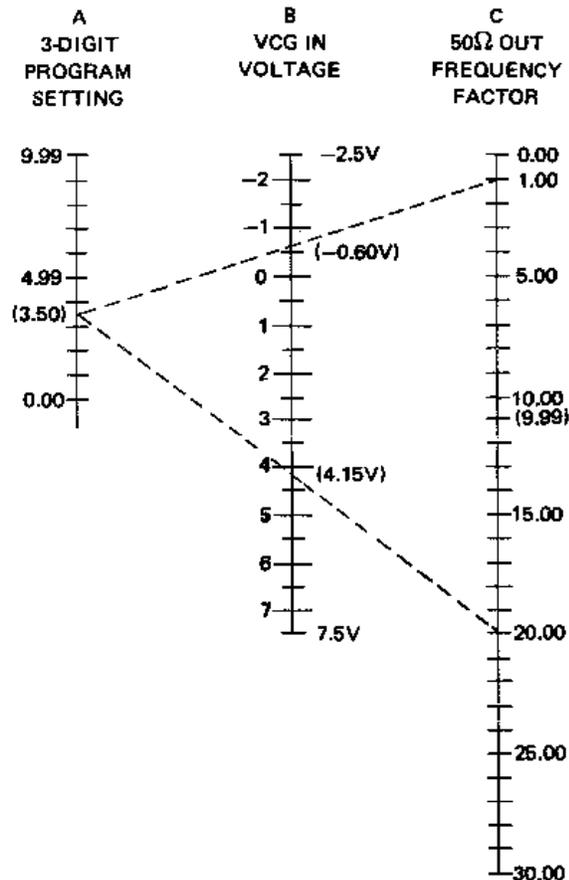


Figure 3-2. VCG Nomograph

3.3.3 Operating as a Triggered/Gated Waveform Generator

Trigger/gate operation is the same as the basic waveform operation plus the connection of a trigger source to the TRIG IN connector and the selection of TRIG or GATED mode, as applicable. The trigger/gate signal must be +2V, but less than ±50V. Input impedance is 1 kΩ. In triggered mode, the trigger signal will cause one cycle of output at the 50Ω OUT connector; in gate mode, the trigger signal will cause an integral burst of cycles lasting for the duration of the trigger signal plus the time required to complete the last cycle initiated during the trigger signal.

3.3.4 Operating as a DC Voltage Source

DC voltage output is not specified, but $\pm 5V$, 100 mA may be obtained by using offset voltage referred to the 0V level of the 50 Ω OUT during the nontrigger time of trigger mode.

1. Terminate the 50 Ω OUT connector with a 50 $\Omega \pm 0.1\%$ termination.
2. Select \wedge function and trigger mode.
3. Program 9.99×10^1 frequency.
4. Program 0.00×10^0 amplitude.
5. Ensure that no trigger signals are received.
6. Select the desired dc output by programming it as offset voltage.

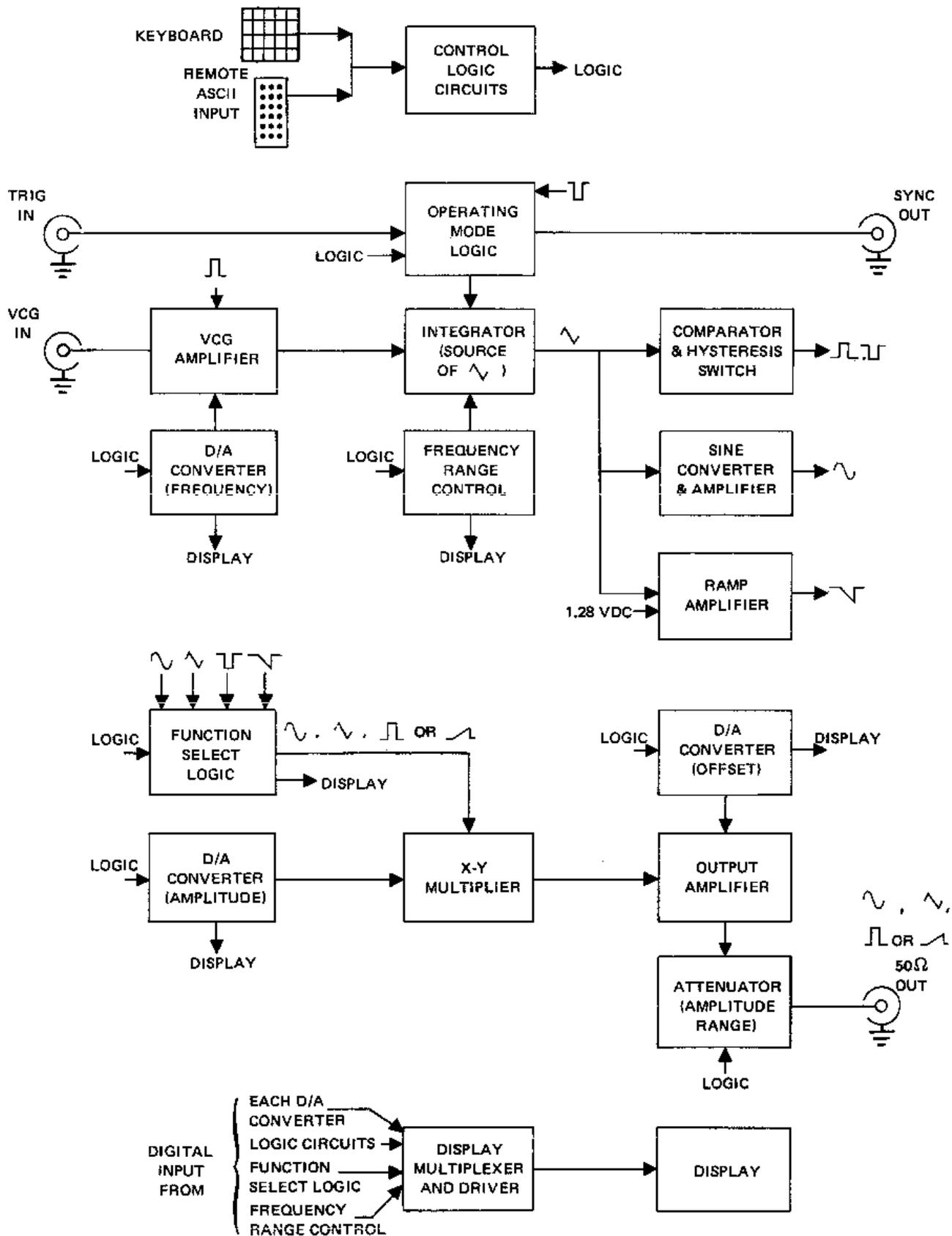


Figure 4-1. Overall Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 LOGIC NOTATION AND TERMINOLOGY

To avoid confusion in determining logic states, please read and understand the following ground rules used in this manual.

1. On the schematics, all signals are true when high unless their mnemonics are overscored; the overscore indicates true-when-low.
2. Pulse and clock refer to transient change of state, whereas status refers to a logic state which requires new input to change.

4.2 BASIC OPERATION

The overall operation can be easily followed in Figure 4-1. All digital programmed inputs are via the keyboard or the remote ASCII connector. Two input BNC connectors are for the TRIG IN and VCG (voltage control of generator) IN signals. The outputs are selectable , ,  or  waveform at the 50Ω OUT BNC. A sync output BNC is also provided for a TTL compatible square wave.

The integrator and comparator and hysteresis switch, acting upon each other, generate the basic waveforms of square and triangle. The mode of operation (triggered, gated or continuous) is logic controlled to act upon the integrator. Logic controls capacitance for generator frequency range and current, via a D/A converter and VCG amplifier, for specific frequency in the selected range. VCG IN voltage will also control frequency.

Diode arrays in the sine converter form the sine wave, and the square wave multiplexes the triangle wave and a voltage level to form the ramp waveform.

The waveform to be output is selected and multiplied with the selected amplitude, after which it is offset and attenuated as programmed.

The digital control data is multiplexed into the display bus for display panel illumination.

4.3 INPUT/OUTPUT

Seven-bit ASCII characters (see Table 2-2 and Drawing 158-200) and clock pulses are supplied to an ASCII data bus on the digital board thru the ASCII DATA IN/OUT connector or supplied by the keyboard to the digital board. (Generators with options will accept and convert other data formats. Once converted, the data is placed on the ASCII data bus.) The character bits are 0 to 0.4 volt for a binary 1 and $\geq 2.4V, < 5.0V$ or open for a binary 0. The character bits are designated D0 thru D6 and prefixed as to their type; i.e., X for in/out external, K for keyboard, and OPT for optional interface conversion.

The ASCII data bus is that set of eight lines handling D0 thru D6 and CLK. Keyboard input J2 is always a part of the bus as well as the termination socket XIC41 (shown in Drawing 158-218, Sheet 1).

Non-ASCII signals to the generator are VCG IN, which is connected to the analog board via the digital board, and TRIG IN, which goes to the trigger logic on the digital board. The generator main output signal is from the analog board to the rear panel 50Ω OUT BNC connector; this signal is a selectable , ,  or  that can be offset, inverted and varied in amplitude. The SYNC OUT signal is a fixed amplitude square wave that is TTL compatible.

4.4 INTERFACE (Drawing 158-218, Sheet 1)

By means of jumpers (Drawing 158-218, Sheet 1), the standard model signals bypass the option card connector J4, allowing J9 (ASCII DATA IN/OUT) to be connected directly to the ASCII data bus. The ASCII data bus may extend thru several instruments. In any case, the integrated circuit termination pack should be inserted only once on the ASCII data bus and at the far end of the bus from the keyboard or control device.

4.5 KEYBOARD (Drawing 159-216)

The keyboard transmits pressed-key data plus a clock pulse to the ASCII data bus. Proper time alignment of the seven data bits and clock is maintained by the IC9 clock circuit driving IC5, a binary counter, to generate a time code. The

counter and the decoder chips (IC3 and IC7C) select a column of keys that are scanned by the multiplexer IC4 to generate time "windows" for the data bits corresponding to each key function. IC4 outputs transmit the status of the selected input. For example, between IC5 count 0 and 1, a 7-bit code for key 0 is generated and ready to be placed on the ASCII data bus if the 0 key is pressed. If the key is pressed, the binary counter IC5 stops and the seven bits plus a clock pulse are placed on the data bus. When the key is released, the windows for keys 1, 2, 3, etc., are generated in sequence.

4.6 DIGITAL BOARD CONTROL LOGIC (Drawing 158-218, Sheet 2)

The stream of ASCII characters (seven parallel bits per character) is decoded into hexadecimal data. This data is then distributed throughout logic control circuitry to program all of the holding registers which control the operation of the generator. Refer to Table 2-2 for conversion of programmed signals, keyboard, hexadecimal, binary and logic bit terminology.

Four types of clock pulses are generated to categorize the bits of data: alpha clock, numerals clock, minus sign clock and range clock. These clock signals, along with the data bits, cause explicit control signals to be generated.

Control logic consists of the following collection of logic blocks:

1. Binary to hexadecimal conversion (0 thru 9, D, 20, 30 and 40)
2. Unit Enable (ITSME)
3. Minus Sign Clock (MCLK)
4. Alpha (Except Multiplier) Clock (40EC)
5. Numerals Clock (30C)
6. Numeral Enables
7. Range (X 10 Multiplier) Clock (RNGCLK)
8. Display Digits Reset (ADRSET)
9. Minus Sign Enable (MSIGN)
10. On/Off Control (ENABLE)
11. Two-Star Converter (D0* thru D3*)
12. Turn-On Reset (RESA, RESB)

4.2

13. Trigger Clock (TRIGC)
14. Mode Select (M0, M1)
15. Manual Trigger
16. Generator Enable ($\overline{\text{OPERATE}}$)
17. Function Select (F0, F1)

4.6.1 Binary to Hexadecimal Conversion (0 thru 9, D, 20, 30 and 40)

The seven bits of character and one clock bit are converted to hexadecimal code. The four least significant bits are converted to a decimal number from 0 thru 9 or D. The three most significant bits are converted to 20, 30 or 40 and enabled for the duration of the clock pulse. See the hexadecimal column in Table 2-2. As shown in the table, 2D is ASCII minus and 20 is ASCII space. Then, on the schematic 20 with D is minus and 20 with 0 is space (the space is one of two multiplier addresses). Hexadecimal 30 with 0 thru 9 are the result of numeric data, and hexadecimal 40 with 0 thru 9 are the result of alpha data.

4.6.2 Unit Enable (ITSME)

A jumper from E24 or E25, etc., to E29 determines the address of the generator as 1, 2, etc. When unit select and a number are programmed, and the number is the correct unit address, ITSME status is generated. ITSME enables alpha and numerals clock and the display.

4.6.3 Minus Sign Clock (MCLK)

MCLK is generated when a phase inversion or negative offset is programmed (ASCII -).

4.6.4 Alpha (Except Multiplier) Clock (40EC)

If the correct generator is addressed and any alpha other than multiplier is input, a clock pulse is generated (40EC and $\overline{40EC}$). This signal is used to clock all alpha related functions except the range (or X 10 multiplier). ITSME enables.

4.6.5 Numerals Clock (30C)

Numerals clock (30C) is used to distinguish between alphas

and numerics and to clock numeric related functions.

4.6.6 Numeral Enables

This circuit triggers the display digit reset one-shot and enables a portion of the range clock circuit only for the numeral programmed immediately after an alpha (except range). Output is

Numeral = High
Alpha = Low

4.6.7 Range (X 10 Multiplier) Clock (RNGCLK)

If a numeral was last programmed, an ASCII space programmed will generate a range clock pulse (RNGCLK). Or, if range (ASCII E) is programmed, a range clock pulse is generated. This pulse is used to set the range gate to enable the frequency range logic and the amplitude attenuator logic.

4.6.8 Display Digits Reset (ADRSET)

A high following a low from the numerals enable circuit triggers a 100 ns ADRSET pulse. This pulse is used to clear the registers for the display digits. Therefore, a numeral programmed after an alpha, such as frequency or amplitude, causes the registers to be cleared, but another programmed numeral will not cause the registers to clear.

4.6.9 Minus Sign Enable (MSIGN)

MSIGN status is generated on the falling edge of MCLK; that is, an inverted phase or offset has been programmed. MSIGN status is removed when an alpha is generated. MSIGN is used to change the polarity of the amplitude or offset.

4.6.10 On/Off Control (ENABLE)

The 50Ω OUT output is enabled when output-on is programmed. Output-on (ASCII H) generates ENABLE and $\overline{\text{ENABLE}}$. Output-off (ASCII I) inhibits ENABLE and $\overline{\text{ENABLE}}$.

4.6.11 Two-Star Converter

	Decimal									
	0	1	2	3	4	5	6	7	8	9
XD0		H		H		H		H		H
XD1			H	H			H	H		
XD2					H	H	H	H		
XD3									H	H
XD0*		H		H		H		H		H
XD1*			H	H			H	H	H	H
XD2*					H	H	H	H	H	H
XD3*									H	H

4.6.12 Turn-On Reset (RESA, RESB)

This one-shot multivibrator clears or presets all necessary holding registers at power-on time.

4.6.13 Trigger Clock (TRIGC)

When the operating mode is programmed (ASCII B), the gate IC49 is enabled in order for the following programmed numerals clock pulse (30C) to generate the trigger clock pulse (TRIGC). This pulse is used to gate the manual trigger D0 binary data bit and clock bits $\overline{1}$ and $\overline{2}$ of mode numerics at the mode select circuit to generate M0 and M1.

4.6.14 Mode Select (M0, M1)

$\overline{1}$	$\overline{2}$	MODE	M0	M1
H	H	CONT	L	L
L	H	TRIG	H	L
H	L	GATE	L	H

Numerics $\overline{1}$ and $\overline{2}$ determine status of M0 and M1 when clocked by TRIGC. These status signals define the operating mode of the generator in the trigger circuit and display.

4.6.15 Manual Trigger

After the trigger mode is programmed, any subsequent programmed ASCII binary bit D0, such as the numeral 1, will generate another TRIGC; the combination of TRIGC and D0 is a manual trigger pulse. The manual trigger rate must be slower than the generator frequency.

4.6.16 Generator Enable ($\overline{\text{OPERATE}}$)

See Paragraph 4.6.14 for M0 and M1 status for a given mode.

Continuous Mode. If continuous mode is programmed, M0 and M1 are low which holds $\overline{\text{OPERATE}}$ low, allowing the generator to run.

Gated Mode. In gated mode, M0 is low and M1 is high. Trig-mode gate is held high; gate-mode gate is gated and will respond to a trigger signal. When TRIG is high, $\overline{\text{OPERATE}}$ is low. When TRIG is low, the low is removed from the IC40B clear, and the completion of the SQR square wave at the IC40B clock input causes $\overline{\text{OPERATE}}$ to be high.

Triggered Mode. In triggered mode, M0 is high and M1 is low. Gated-mode gate is held high; trig-mode gate is gated and will respond to the TRIG or manual trigger signal. A trigger causes the trig-mode gate to go high, allowing OPERATE to be low. OPERATE feedback to IC40A removes the clear on IC40B and upon the completion of the SQR square wave at the IC40B clock input causes OPERATE to go high.

4.6.17 Function Select (F0, F1)

When the alpha for function is programmed (ASCII C), the gate IC49 is enabled in order for the following programmed numerals clock pulse (30C) to clock ASCII binary bits D0 and D1. D0 and D1 are the least significant bits of the programmed numeral. (0 = , 1 = , 2 =  and 3 = .) Outputs are as noted on the schematic.

4.7 FREQUENCY D/A LOGIC (Drawing 518-218, Sheet 6)

The programming of the frequency alpha (ASCII F) enables the clearing and clocking gates for the frequency numeric data holding registers. The programming of a numeral following the frequency alpha will clear the registers and enter the data in the LSD register. Subsequent programmed numerals will be entered serially without any clearing action. Output data of the registers controls the diode gates, which switch current thru weighting resistors into a summing node of an amplifier to create the analog voltage labeled D/F. The register output data is also used for display information.

If the range alpha (ASCII E) is programmed and frequency was the last programmed alpha, the frequency clearing and clocking gates are disabled and the gate for the range data holding register is enabled. Subsequent programmed numerals will enter the data at the range data holding register input. The outputs FR0, FR1 and FR2 of this register are decoded to decimal data which are used to control relays for selected range capacitors and frequency adjustment controls (see Schematic 158-219 and Paragraph 4.12.5). FR0, FR1 and FR2 are also used as display information.

4.8 OFFSET D/A LOGIC (Drawing 158-218, Sheet 5)

The programming of the offset alpha (ASCII D) enables the clearing and clocking gates for the offset numeric data holding registers. The programming of a numeral following the offset alpha will clear the registers and enter data in the LSD register. Subsequent programmed numerals will be entered serially without any clearing action. Output data of the registers controls the diode gates, which switch current thru weighting resistors into a summing node of an amplifier to create the analog voltage labeled DC OFFSET. The register output data is also used for display information.

If inversion is programmed (ASCII -) following offset, MOFFSET is generated which causes the electronic SPDT switch to control the polarity of the selected offset voltage.

4.9 AMPLITUDE D/A LOGIC (Drawing 518-218, Sheet 4)

The programming of the amplitude alpha (ASCII A) enables the clearing and clocking gates for the amplitude numeric data holding registers. The programming of a numeral following the amplitude alpha will clear the registers and enter the data in the LSD register. Subsequent programmed numerals will be entered serially without any clearing action. The output data of the registers controls the diode gates, which switch current thru weighting resistors into a summing node of an amplifier to create the analog voltage labeled D/V. The register output data is also used at the display driver circuit.

If the range alpha (ASCII E) is programmed and amplitude was the last programmed alpha, the frequency clearing and clocking gates are disabled and the gate for the range data holding registers clock is enabled. Subsequent programmed numerals will enter numeric data at the range data holding register inputs with the following results:

1	2	-20 dB	-40 dB	0 dB
H	L	L	H	L
H	H	L	L	H
L	H	H	L	L

Where 0 dB = X 10⁰ multiplier
 -20 dB = X 10⁻¹ multiplier
 -40 dB = X 10⁻² multiplier

Normal waveform phase has been set by the function select circuit signal F1 in the following manner:

Function	F1	MAMPL	Q7	Q8	Normal-Phase D/V Polarity
	L	L	On	Off	+
	L	L	On	Off	+
	H	H	Off	On	-
	H	H	Off	On	-

If inversion is programmed (ASCII -) following the amplitude alpha, MAMPL status is reversed, causing the electronic DPST switch controlling Q7 and Q8 to reverse the polarity of the analog signal D/V. D/V controls 50Ω OUT signal amplitude and polarity at the X-Y multiplier (see Schematic 518-219 and Paragraph 4.12.7).

**4.10 DIGITAL BOARD DISPLAY (DRIVER) LOGIC
(Schematic 158-218, Sheet 3)**

All of the status data from the holding registers are accumulated and multiplexed into the display logic. By multiplexing, the data is transferred to the display in a minimum amount of lines (DD0 thru DD3) and then is decoded on the display board. To synchronize the transferred data, a sync (\overline{DSYNC}) line and clock (\overline{DCLK}) pulse are provided for both multiplexing and decoding.

4.10.1 Clock and Multiplex Time Code

The divide-by-9 binary counter IC37, clocked at a 5 kHz rate, supplies the necessary time codes (K0, K1, K2, K3) for multiplexing the display data. The same 5 kHz clock also drives the clock pulse \overline{DCLK} for the display.

4.10.2 Select Frequency, Amplitude or Offset Display

\overline{SELF}	\overline{SELA}	\overline{SELOFF}	SD0	$\overline{SD0}$	SD1	$\overline{SD1}$
L	H	H	H	L	L	H
H	L	H	L	H	L	H
H	H	L	L	H	H	L

The SELF, SELA and SELOFF status signals from their respective D/A circuits generate the SD0 and SD1 codes which enable frequency, amplitude, offset, range or minus sign data for multiplexing. Because amplitude, frequency and offset share the same numerical display, this code necessarily ensures that only one set of data is enabled at a time.

4.10.3 Amplitude, Frequency and Offset Multiplexing

All three of the multiplexer outputs are paralleled and connected to the display bus thru the 2-star decoder. The three multiplexer chips, frequency, amplitude and offset, receive input data from the holding registers of their respective D/A converters. The multiplexers are enabled by the programming of frequency, amplitude or offset, which generate SD0 and SD1, and by time code $\overline{K2}$. In a specific multiplexer, the three groups (A, B and C) of four data bits each are placed on the bus (DD0, DD1, DD2 and DD3) by time codes K0 and K1. See the chart on the schematic and the ABC versus K0, K1 matrix on the multiplexer itself for logic and states and timing. The 2-star decoder converts the 2-star bit weighting back to conventional binary (see 2-star converter, Paragraph 4.6.11).

4.10.4 Amplitude and Frequency Range (X 10 Multiplier) Multiplexing

In the multiplexer A groups, -20 and -40 dB are amplitude attenuation, while FR bits of the B group are frequency selection bits. The A group or the B group is enabled for

multiplexing by SD0, which is high for frequency display and low for amplitude and offset. Multiplexing is controlled by time codes $\overline{K0}$, $\overline{K1}$ and $\overline{K2}$ (see the chart on the schematic).

4.10.5 Minus Signs, Function and Enable, and Mode and Unit Select Multiplexing

Multiplexing of the following signals is controlled by K2, $\overline{K0}$ and $\overline{K1}$, as shown on the schematic chart.

The minus sign for amplitude is gated by the selection of amplitude for display, $\overline{SD1}$ and $\overline{SD0}$ high. The minus sign for offset is gated by the selection of offset for display, $\overline{SD0}$ and SD1 high. 0 dB or SD0 high (the selection of frequency) will be used to inhibit the range minus sign for frequency and 0 dB amplitude. SD0 and SD1 states are used to light the display mode LEDs. F0 and F1 states are used to light the function (waveform) LEDs. \overline{ENABLE} is used to enable the display of the function symbol. M0 and M1 states cause the operating mode LEDs to light. ITSME causes the UNIT SELECTED LED to light.

4.10.6 Display Enable

Some systems may have several instruments connected to one display. Display enable ensures that only one instrument at a time drives the display. If this unit is selected (\overline{ITSME}), its display data will be gated. If it is not selected, but power is on, the subsequent K3 edge will cause a low to be generated, disabling the display data output.

4.11 DISPLAY LOGIC (Drawing D158-217)

The display board receives the multiplexed data character (bits DD0 thru DD3) from the digital board. At each character time, the bits represent one of the following display items or groups:

Data	Display	Enable Signal	Data Bits
Range Digit	DS1	D1G9	DD0 - DD3
Most Significant Digit	DS2	D1G1	DD0 - DD3
Middle Digit	DS3	D1G2	DD0 - DD3
Least Significant Digit	DS4	D1G3	DD0 - DD3
Display Mode	CR11 - CR13	D1G4	DD2 - DD3
3-Digit-Value Minus Sign	DS8	D1G4	DD0
X 10 Multiplier Minus Sign	DS7	D1G4	DD1
Function (Waveform)	CR1 - CR4	D1G5	DD0 - DD3
Operating Mode	CR8 - CR10	D1G6	DD0 - DD2
Unit Select	CR17	D1G6	DD3

The routing of the correct data to the correct display is determined by the clock pulse shifting the XSYNC bit thru the 9-bit parallel output shift register. The shift register outputs (DIG1 thru DIG9) enable the clock signal to clock the multiplexed data bits into the proper display holding registers at the proper time, thus correctly routing and de-skewing the data bits.

4.12 ANALOG BOARD (Drawing 158-219)

4.12.1 Generator Loop

The purpose of this loop is to generate symmetrical triangle and square waves simultaneously.

Control of current direction for capacitor C (Figure 4-2) charging is determined by whether diode switch CR1 (IC14-7) is forward biased (turned on) or reverse biased (turned off). Resistors R22, R40, R45, R52, R58 and R73 are matched to ensure equal currents.

When the voltage at point A is positive, diode CR1 is forward biased and CR2 is reverse biased. When CR1 is forward biased by the positive cycle of the square wave, current $2I$ (twice I) pulled by the 1st VCG amplifier comes from the square wave source. Because CR2 (IC14-6) is reverse biased, the current I from the 2nd VCG amplifier is

charging the capacitor C which causes the voltage at point B to decrease linearly. As soon as the voltage at point B reaches $-1.25V$, the output of the hysteresis switch will switch to a negative voltage. CR1 becomes reverse biased and CR2 becomes forward biased. The current pulled by the 1st VCG amplifier ($2I$) is now comprised of the current from the 2nd VCG amplifier (I) and exactly I from the capacitor C, which is the same amount as its charging current. The voltage at point B will increase. Again the hysteresis will switch positive when the voltage at point B reaches $+1.25V$. Thus, the triangle and square wave signals are generated simultaneously.

4.12.2 VCG Amplifier

The output frequency depends on the size of the capacitor selected and the amount of current I charging the capacitor. The magnitude of the current is controlled by the VCG amplifiers, which in turn are controlled by the voltage from the frequency D/A amplifier and the VCG input.

4.12.3 Sine Converter and Amplifier

The triangle is shaped into a sine wave thru three diode networks utilizing the nonlinearity of the diodes. The outputs of these diode networks are summed and amplified in the sine amplifier.

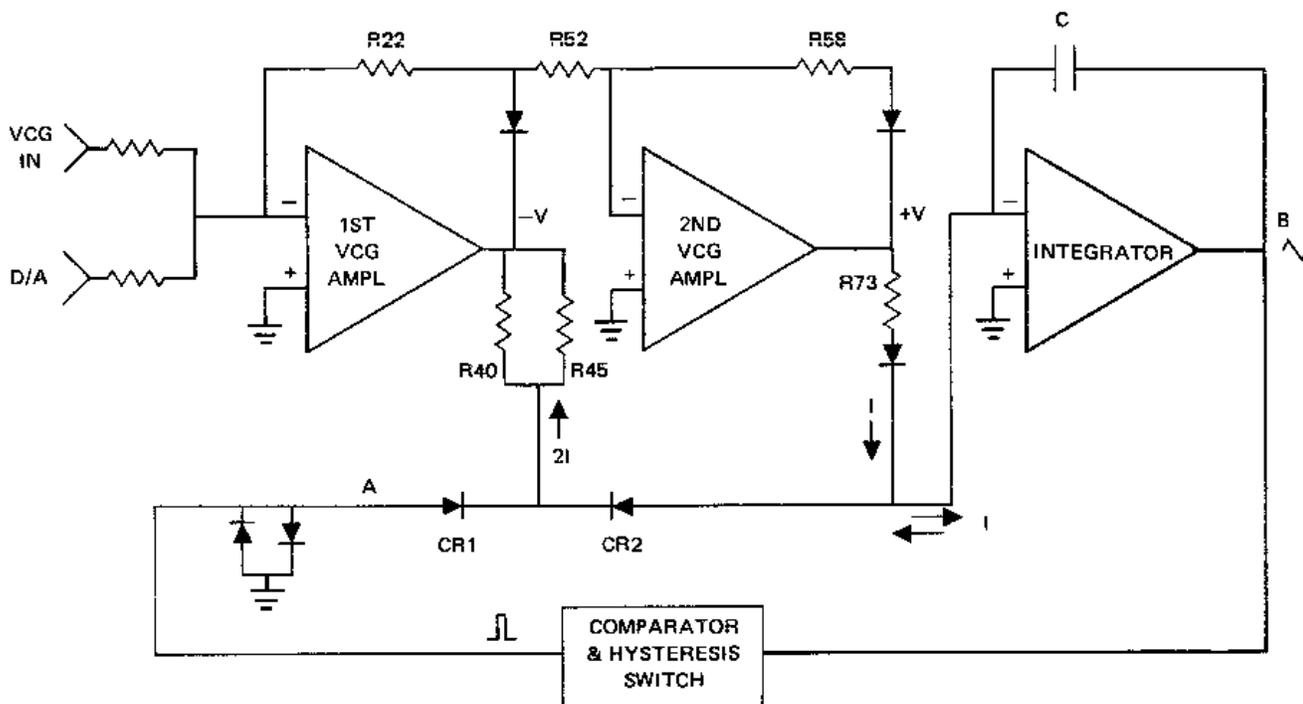


Figure 4-2. Generator Loop

4.12.4 Ramp Amplifier

A square wave from the comparator circuit (Figure 4-3) alternately enables the negative triangle ramp thru IC8A and the +1.25V from R64 thru IC8B to form the ramp waveform. The output resultant is +1.25V during one half cycle and the negative going portion of the triangle during the other half portion.

4.12.5 Frequency Range Logic

FR0	FR1	FR2	Power of 10
L	L	L	0
H	L	L	1
L	H	L	2
H	H	L	3
L	L	H	4
H	L	H	5
L	H	H	6
H	H	H	7

This circuit contains a binary to decimal decoder, which converts three lines of input data (FR0, FR1, FR2) to a one-line-of-eight output in order to drive the frequency range multiplier relays and control adjustments. FR0, FR1 and FR2 originate from holding register IC23 on the digital board (see Frequency D/A Logic, Paragraph 4.7).

4.12.6 Function Selector

F0	F1	Function
H	H	~
L	H	^
H	L	⏏
L	L	⏏

Selection of each waveform is accomplished by electronic switches. See Digital Board Schematic 158-218, Sheet 2, and Paragraph 4.6.17 for the origin of $\overline{F0}$ and $\overline{F1}$.

4.12.7 X-Y Multiplier and Output Amplifier

The selected waveform is fed into one input of the X-Y multiplier and a control voltage from the amplitude D/A amplifier is fed to the other input. Refer to Figure 4-4. The differential output from the X-Y multiplier is directly proportional to the product of the two inputs. One of the differential outputs is fed thru an inverting amplifier and then summed into a second inverting amplifier along with the other differential output from the x-y multiplier. The combined operation of these two inverting amplifiers is equal to one differential amplifier. Waveform inversion and addition is as shown in Figure 4-4.

4.12.8 Attenuator Select Logic

Attenuation of 0 dB, -20 dB or -40 dB is accomplished by selecting one-of-three range relays and an enable relay allowing the output amplifier to be enabled or disabled to the 50Ω OUT connector.

4.12.9 Generator Enable

The triangle generator loop will free run continuously only if the OPERATE voltage is low. Refer to Figure 4-5. When the OPERATE voltage is high, the output of the integrator will be clamped to the input, which stops the generator from free running. The J-K flip-flop is used to control the timing so that the triangle will always stop at the end of the cycle. The triangle will stop at time t_3 if GATE ENABLE is reset high between times t_1 and t_2 as shown in the timing diagram of Figure 4-5. OPERATE originates from the digital board generator enable circuit (refer to Schematic 158-218, Sheet 2, and Paragraph 4.6.16).

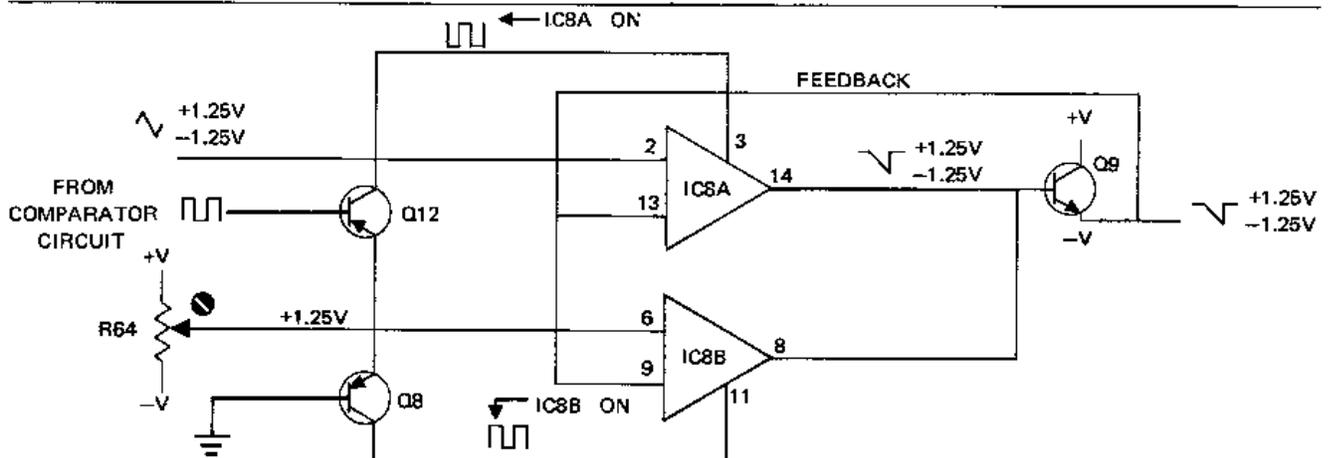


Figure 4-3. Ramp Amplifier

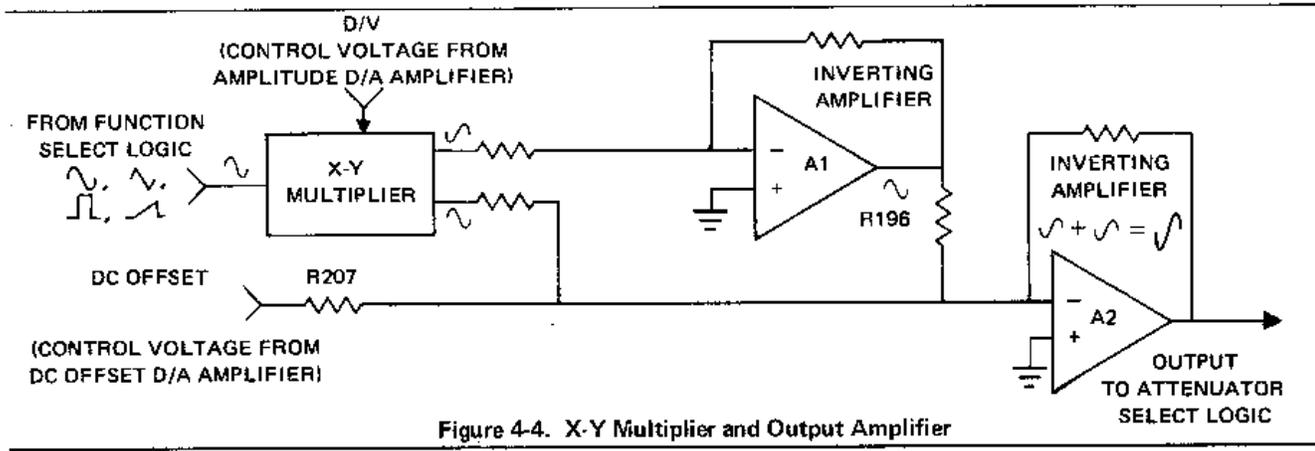


Figure 4-4. X-Y Multiplier and Output Amplifier

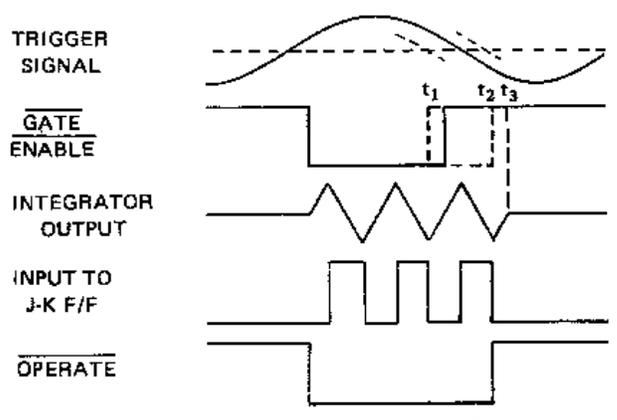
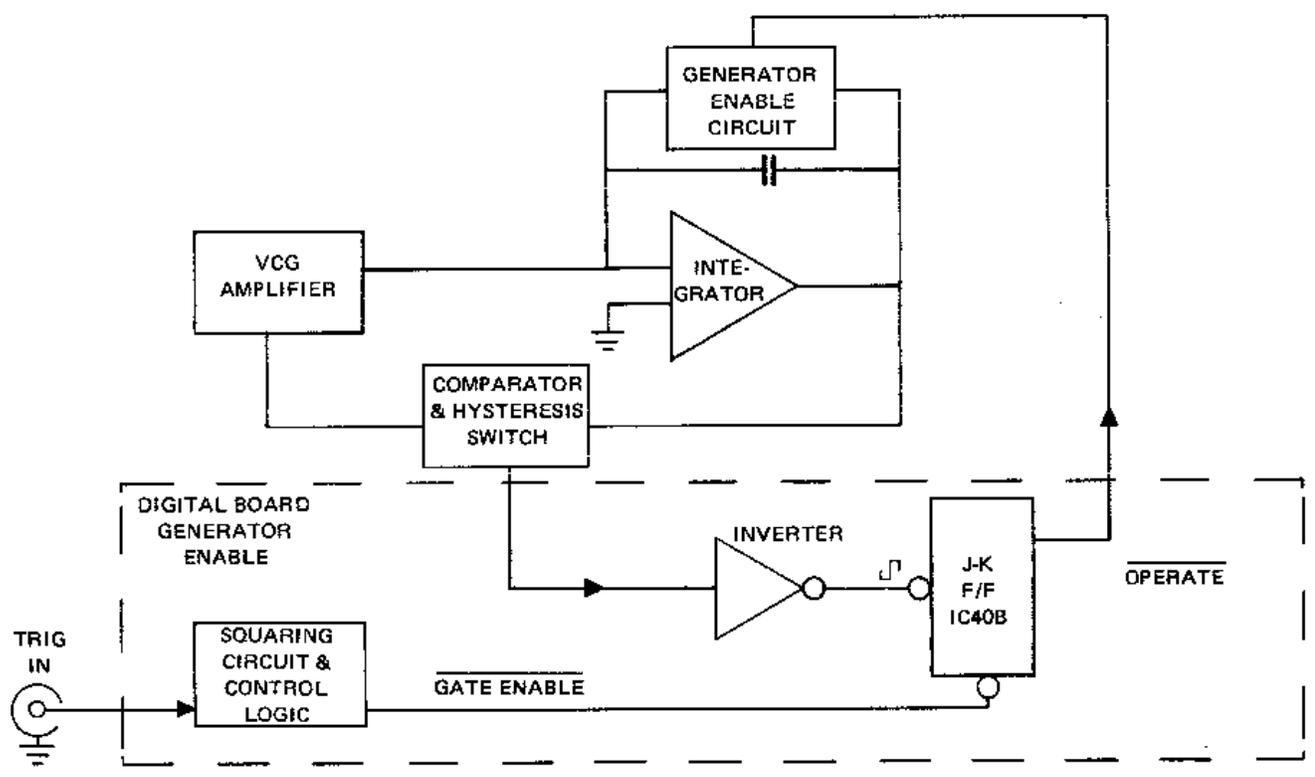


Figure 4-5. Trigger/Gate Block and Timing Diagrams

5

SECTION 5 CALIBRATION

After referring to the following preliminary data, perform calibration, as necessary, per Table 5-1. If performing partial calibration, check previous settings and adjustments for applicability.

1. Refer to calibration drawing, Figure 5-2, and calibration chart (Table 5-1).
2. Unless otherwise noted, all measurements made at the 50Ω OUT connector should be terminated into a 50Ω (±0.1%) load.
3. TPs (Test Points) and adjustments are prefixed as follows:
 - A1 – Power Supply
 - A2 – Digital Board
 - A3 – Analog Board
4. Before connecting the unit to an ac source, check the ac line circuit to make sure the 115/230 and Ht/LO switches are set at the correct position (see Paragraph 2.2.1).
5. Start the calibration by setting the front panel switches or program for the following:

Power	On
Unit Select	Select unit to be calibrated
Mode	Continuous
Frequency	9.99E2
Amplitude	9.99E0
Offset	0.00
Function	∧
Output On/Off	On
6. Allow the unit to warm up at least 30 minutes for final calibration.

Table 5-1. CALIBRATION CHART

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Power Supply Regulation	Voltmeter	A3TP2 (+15V), A3TP1 (Gnd)	See initial conditions.	1	A1R24	+15V ±20 mV	
		A3TP3 (-15V), A3TP1		2	—	-15V ±50 mV	
		A3TP4 (+5V), A3TP1		3	—	+5V ±250 mV	
Triangle Amplitude	Oscilloscope	A3TP5, A3TP1 (Gnd)		4	A3R59	+1.25V ±5 mV	
		A3TP5, A3TP1		5	A3R62	-1.25V ±5 mV	
Symmetry	Oscilloscope	50Ω OUT	Func  Freq 0.10E4	6	A3R16	Minimum frequency change*	*While opening and shorting VCG IN to BNC case.
				7	A3R90, A3R17*	Time symmetry error <1%	*Use if necessary for adjustment of proper frequency.
				8	A3R44, A3R17*	Time symmetry error <1%	*Use if necessary for adjustment of proper frequency. Repeat 7 and 8, as necessary, for optimum results.

Table 5-1. CALIBRATION CHART (Continued)

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Frequency	Counter	SYNC OUT	Freq 9.99E3	9	A3R2	9.99 kHz	Repeat 9, 10 and 11 for optimum results. If adjustment is made, repeat 11.
			9.99E5	10	A3C33	999 kHz	
			1.00E3	11	A3R17	1.00 kHz	
			0.00E3	12	A3R17	<10 Hz	
			9.99E0	13	A3R15	9.99 Hz	
			9.99E1	14	A3R11	99.9 Hz	
			9.99E2	15	A3R6	999 Hz	
			9.99E4	16	A3C15	99.9 kHz	
			3.00E6	17	A3R5	3.00 MHz	
			1.00E6	18	A3R5	1.00 MHz	Repeat 17 and 18 for optimum results.
X-Y Multiplier	Oscilloscope	A3TP5, A3TP1 (Gnd) 50Ω OUT	Func  Freq 9.99E2 Ampl 0.00E0 Ofst 0.00 Mode Trig	19	A3R119	0V ±5 mV	Obtain minimum voltage shift when switching between + and - offset. Adjust A3R217 to keep voltage at zero. Recheck 21. Readjust A3R217 to keep voltage at zero.
			Short A3TP5 to A3TP1 <i>MONITOR 50Ω out</i>	20	A2R28	Minimum voltage shift (±5 mV) <i>dc</i>	
			Ampl 0.00	21	A3R182	<10 mV <i>dc</i>	
			Ampl 9.99	22	A3R182	<10 mV <i>dc</i>	
			Remove A3TP5 short Ampl 0.00E0 Mode Cont	23	A3R186	Minimum signal	
			Ampl 0.02E0	24	A3R201	Most linear triangle waveform	
			Ampl 0.00E0	25	A3R186, A2R99	Minimum + and - amplitude	
						Obtain minimum signal in both + and - amplitude.	

Table 5-1. CALIBRATION CHART (Continued)

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Sine Distortion	Oscilloscope, LF Sine Distortion Amplifier with X 1 probe	A3TP5* 50Ω OUT	Func 	26	A3R137, A3R138	Minimum sine distortion	*See Figure 5-1 for test setup.
				27	A3R190	Minimum sine distortion	Typically <0.2%. See Figure 5-1 for test setup.
			Freq* 9.99E3 9.99E2	28	A3R137, A3R138, A3R190	Minimum sine distortion	*Optimize for both settings.
				29			Repeat 19 thru 23.
Output Amplitude and DC Offset	Voltmeter	50Ω OUT	Short A3TP5 to A3TP1 Func  Ampl 0.00E0 Ofst 5.00 Mode Trig	30	A2R30	+5.00 Vdc ±10 mV	
			Ofst -5.00	31	A2R34	-5.00 Vdc ±10 mV	
			Ofst 0.00	32	A2R28	Minimum voltage shift (<5 mV)*	*While switching from + and - dc offset. Adjust A3R217 to keep voltage at zero.
				33			Repeat 30, 31 and 32 to optimize.
			Remove A3TP5 short Ampl 9.99E0 Mode Cont	34	A2R107	9.99V p-p  ±10 mV	
			Ampl -9.99E0	35	A2R111	9.99V p-p  ±10 mV	
			Func  Ampl 9.99E0	36	A3R55, A3R48	±5.00V peak ±10 mV	
			Ampl -9.99E0	37	A3R55, A3R48	50% of observed error*	*Split error with 36.
			Func 	38	A3R98, A3R116	±5.00V peak ±10 mV	R98 - Amplitude R116 - Symmetry
			Func 	39	A3R79, A3R64	±5.00V peak ±10 mV	R79 - Symmetry R64 - Separation

Table 5-1. CALIBRATION CHART (Continued)

Check	Tester	Calibrated Points	Program	Seq	Control	Desired Results	Remarks
Output Amplitude and DC Offset (Continued)			Func \square Freq 9.99E5 Ampl 1.00E0	40	A3C53, A3C56	Best square wave in both + and - amplitude	

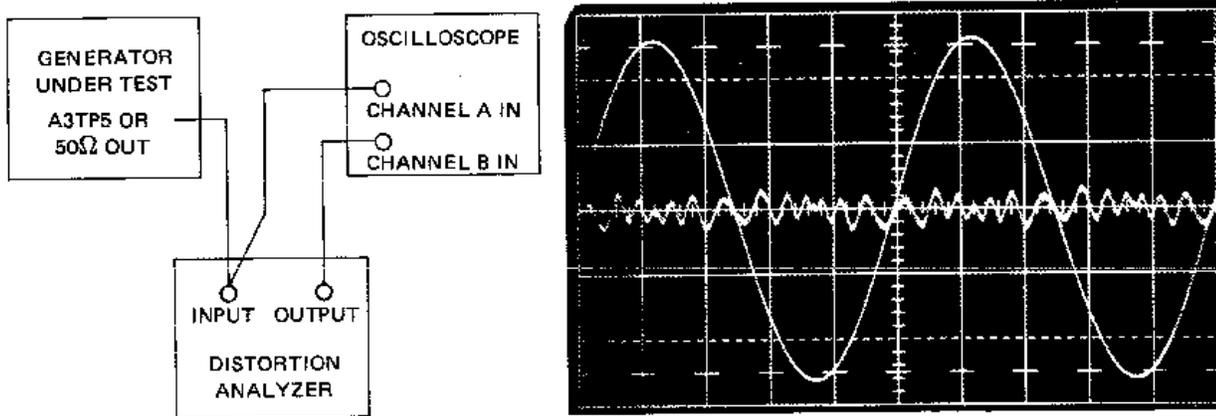


Figure 5-1. Distortion Analysis Test Setup

6

SECTION

TROUBLESHOOTING

6.1 CORRECTIVE MAINTENANCE

This portion of the manual presents a systematic approach to troubleshooting. It is composed of three parts:

Part 1. Troubleshooting Techniques for Individual Components (Paragraph 6.2) – Frequently you can quickly locate a defective component by this technique without understanding the detailed function of the circuit. It is also a necessary technique when extensive troubleshooting in the component level is required.

Part 2. Quick Troubleshooting Guide (Paragraph 6.3) – Start by observing the symptoms of malfunctioning; then use the guide to find the defective components or malfunctioning circuits.

Part 3. Key Signals, Voltages and States (Table 6-1) – This is a supplemental procedure to Part 2 and used to locate defective components within the malfunctioning circuits.

6.2 TROUBLESHOOTING TECHNIQUES FOR INDIVIDUAL COMPONENTS

6.2.1 Bipolar Transistor

1. A transistor is defective if more than one volt (typically 0.7V) across the base/emitter junction is measured in the forward direction.
2. A transistor, when used as a switch, may have a few volts reverse bias voltage.

6.3 QUICK TROUBLESHOOTING GUIDE

Symptom	Corrective Action
Blown Line Fuse	<p>Replace fuse. If it blows again, check the following:</p> <ol style="list-style-type: none"> 1. One of the four transistors mounted on the rear panel is shorted to itself or to chassis ground. 2. Bypass capacitors for power supply are shorted. 3. Follow algorithm (Figure 6-1) to locate short in a particular supply.

6.2.2 Diode

A diode is defective if it has greater than one volt (typically 0.7V) forward voltage across it (except Zener and LED).

6.2.3 Operational Amplifier (e.g., 741, CA3030)

The + and – inputs of an operational amplifier should have less than 15 mV difference when operating under normal conditions.

6.2.4 FET (Field Effect Transistor)

1. No gate current should be drawn by the gate. If so, the FET is defective.
2. The gate-to-source voltage is always reversed biased under normal operating conditions. If otherwise, the FET is defective.

6.2.5 Capacitor

1. Shorted capacitors have zero volts across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

Symptom	Corrective Action
+15V Power Supply Malfunction	<ol style="list-style-type: none"> 1. Voltage low: <ol style="list-style-type: none"> a. Transformer output low. b. Extra current loading; check for overheated and defective component. Use P1, P2 and P3 for isolation of current loading. 2. Voltage high: <ol style="list-style-type: none"> a. Power transistor Q1 and Q2 shorted. b. IC1 defective.
Other Power Supply Malfunctions	<ol style="list-style-type: none"> 1. Use similar procedure for troubleshooting as in the +15V power supply malfunctions. 2. Follow Figure 6-1 to locate problem in a particular power supply.
No Output Signals	<ol style="list-style-type: none"> 1. If no  signal is present at output of integrator, follow Figure 6-2 for troubleshooting. 2. If no signal is present at TP5, check function selector in Table 6-1. 3. If no signal is seen at junction of R243 and R245, follow Figure 6-3, output amplifier.
 but no  ,  or 	Follow Table 6-1 to check out the corresponding circuit.
Frequency Accuracy Out of Specification	<ol style="list-style-type: none"> 1. Check frequency calibration. 2. Check for frequency change when changing frequency bit-by-bit; if problem appears to be in frequency setting, check D/A circuitry.
Amplitude Accuracy Out of Specification	<ol style="list-style-type: none"> 1. Check calibration. 2. Check for amplitude change when changing amplitude bit-by-bit; if problem appears to be in amplitude setting, check D/A circuitry. 3. Check for saturation of output amplifier (50Ω loaded; amplitude plus dc offset should not exceed 10V p-p).
DC Offset Accuracy Out of Specification	<ol style="list-style-type: none"> 1. Check calibration. 2. Check for offset change when changing offset bit-by-bit; if problem appears to be in offset setting, check D/A circuitry.
TRIG and GATED Mode Inoperative	<ol style="list-style-type: none"> 1. Check for correct signals in the trigger circuit using Table 6-1.

Table 6-1. KEY SIGNALS, VOLTAGES AND STATES AT THE ANALOG BOARD

Frequency Range Logic				
FR2	FR1	FR0	IC6 Pin In Low State	Frequency Range (Ex = X 10 ^x)
L	L	L	10	E0
L	L	H	11	E1
L	H	L	12	E2
L	H	H	13	E3
H	L	L	4	E4
H	L	H	3	E5
H	H	L	2	E6
H	H	H	1	E7

Generator Enable Circuit (Analog Board)

	Continuous	Trig/Gated (No Ext Trigger)
1. P3 pin 31 (OPERATE)	Low State	High State
2. Q14 base	0V	≈ 0.7V

Integrator

1. IC9 pin 4	≈ 0V
2. IC9 pin 5	≈ 1.4V
3. IC11 pin 12	≈ 2.5V p-p 
4. R135 & R136 junction	2.5V p-p 

Comparator Switch

1. Q2 & Q6 emitters	≈ +9V	
2. IC7 pins 2 & 8	≈ -1V	
3. Q2 base	≈ +8V with 0.5V p-p 	opposite phase of Q2 base
4. Q6 base	≈ +8V with 0.5V p-p 	
5. Q1 emitter	≈ +2V/-1.5V 	
6. Q7 emitter	≈ +2V/-2.5V 	

Ramp Amplifier

1. Q8 & Q12 emitters	+0.7V/-2V 
2. IC8 pin 1	≈ +11V
3. IC8 pins 3 & 11	≈ -3V with ≈ 0.5V p-p  opposite phase from pin 3 to pin 11
4. IC8 pin 6	+1.25V
5. IC8 pin 2	2.5V p-p 
6. Q9 emitter	2.5V p-p 

VCG

Voltages depend upon frequency setting.

1. P3 pin 46 (D/F) 0 to -10V
2. IC1 pin 6 0 to +3.7V
3. Q3 emitter -0.7V to -4.0V
4. IC3 pin 6 +0.7V to +4.0V

Sine Converter and Amplifier

1. IC12 pin 6 ≈ 1.2 mV p-p 
2. IC10 pin 4 ≈ 250 mV p-p 
3. IC10 pin 12 2.5V p-p 

Function Selector

F0	F1	Function	Collector of			
			Q43	Q18	Q19	Q20
H	H		≈ +5V	≈ -14V	≈ -14V	≈ -14V
H	L		≈ -14V	≈ +5V	≈ -14V	≈ -14V
L	H		≈ -14V	≈ -14V	≈ +5V	≈ -14V
L	L		≈ -14V	≈ -14V	≈ -14V	≈ +5V

X-Y Multiplier, Inverting Amplifier and Output Amplifier

1. P3 pin 7 (D/V)	-2V to +2V depending on amplitude setting and polarity
2. IC17 pin 4	Selected  ,  ,  or 
3. IC17 pins 3 & 13	≈ -13V
4. IC17 pin 1	≈ 6V
5. IC17 pins 2 & 14	≈ 11V with low level amplitude of selected function
6. Q27 emitter	≈ -4V
7. Q21 base	≈ +13V
8. Q22 base	≈ -13V
9. Q28 emitter	≈ +6V
10. Q32 emitter	≈ +6V
11. Q33 base	≈ +13V
12. Q34 base	≈ -13V
13. Q37 & Q38 collectors	≈ twice programmed amplitude p-p
14. R243 & R245 junction	≈ twice programmed amplitude p-p
15. Q21, Q22, Q27 thru Q38, Q41 & Q42	On in any normal state (i.e., base/emitter drop should be ≈ 0.7V in forward bias direction)
16. Q39 & Q40	On only when output sinks or sources > 100 mA

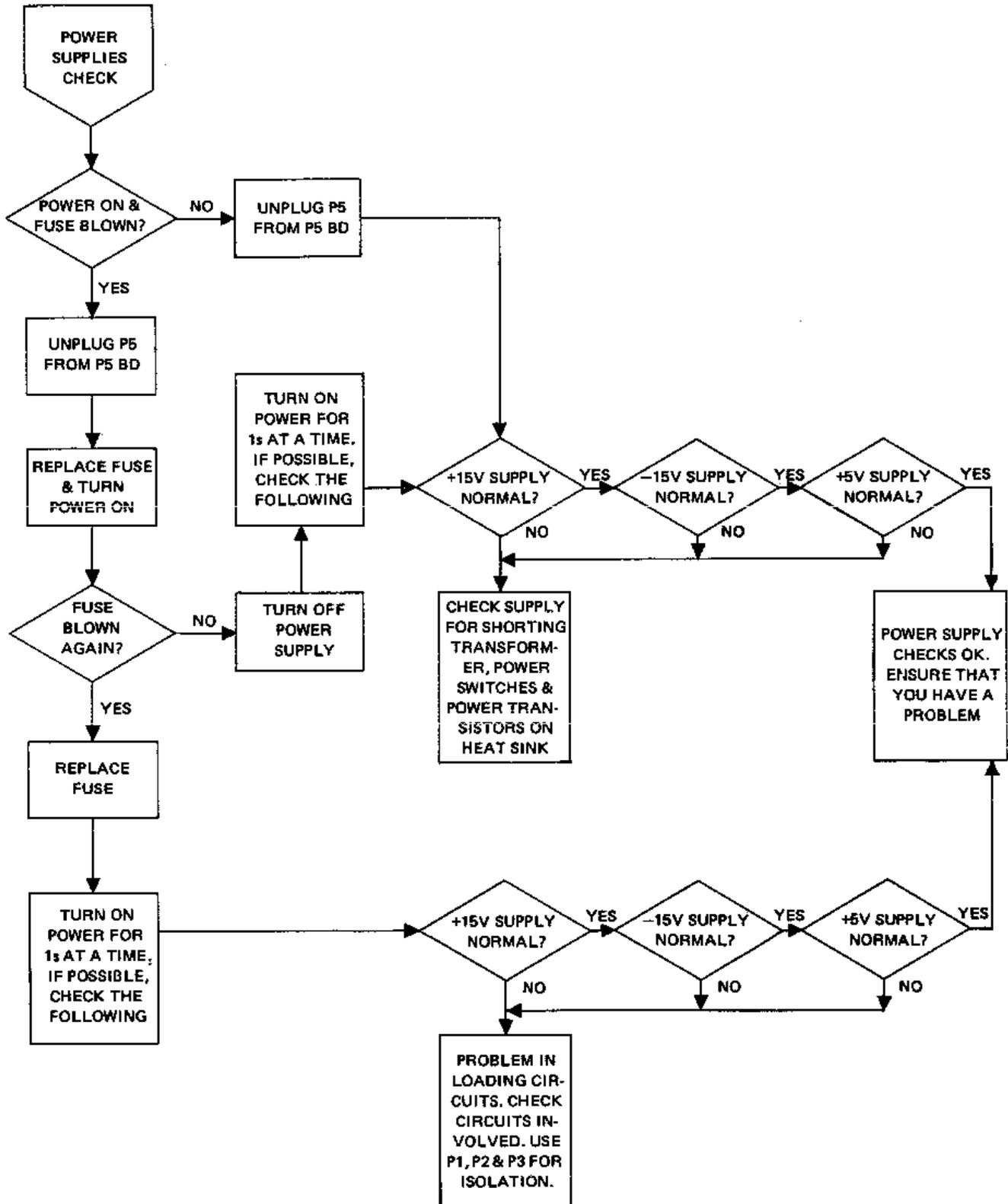


Figure 6-1. Power Supply Algorithm

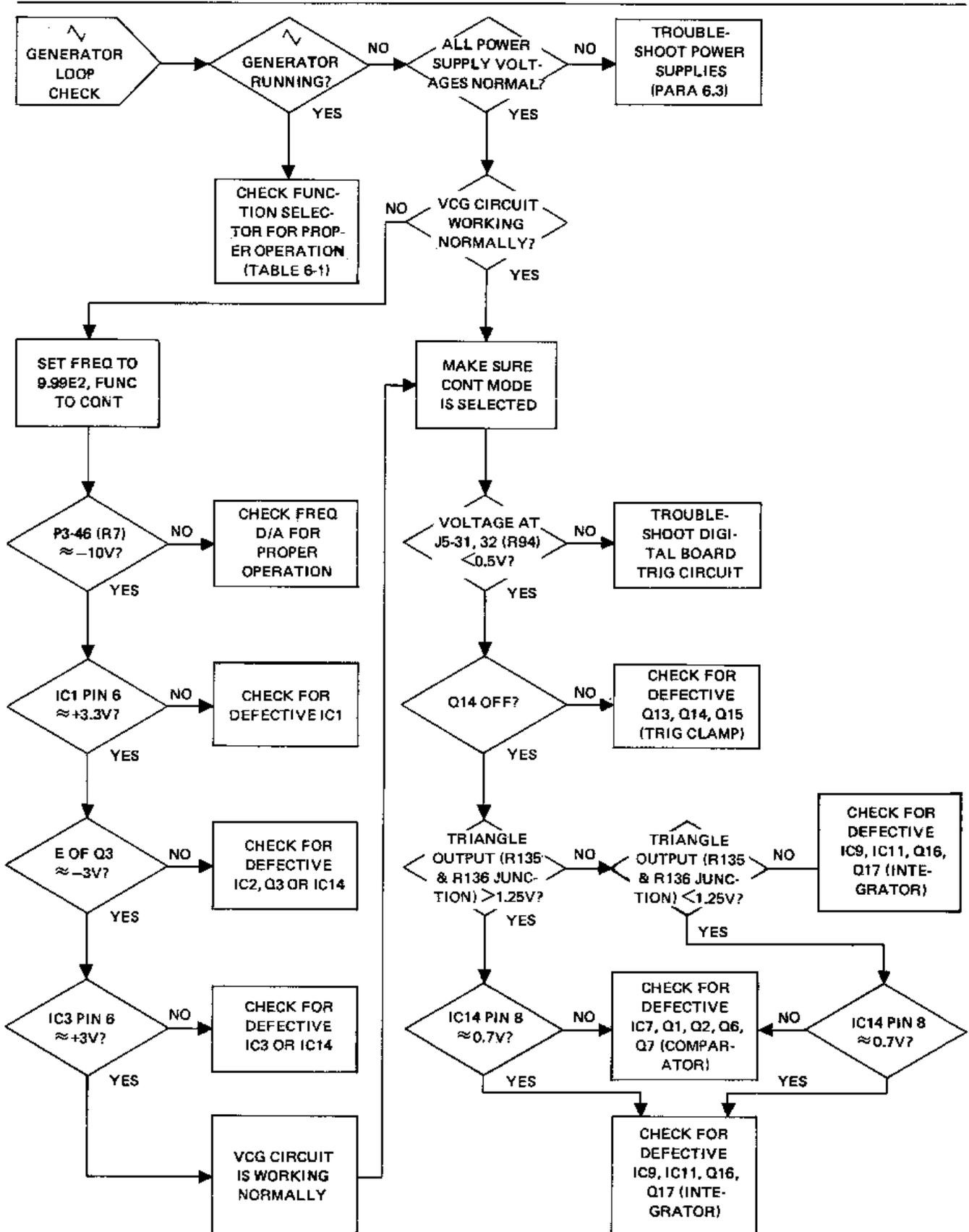


Figure 6-2. Integrator, Comparator and VCG Algorithm

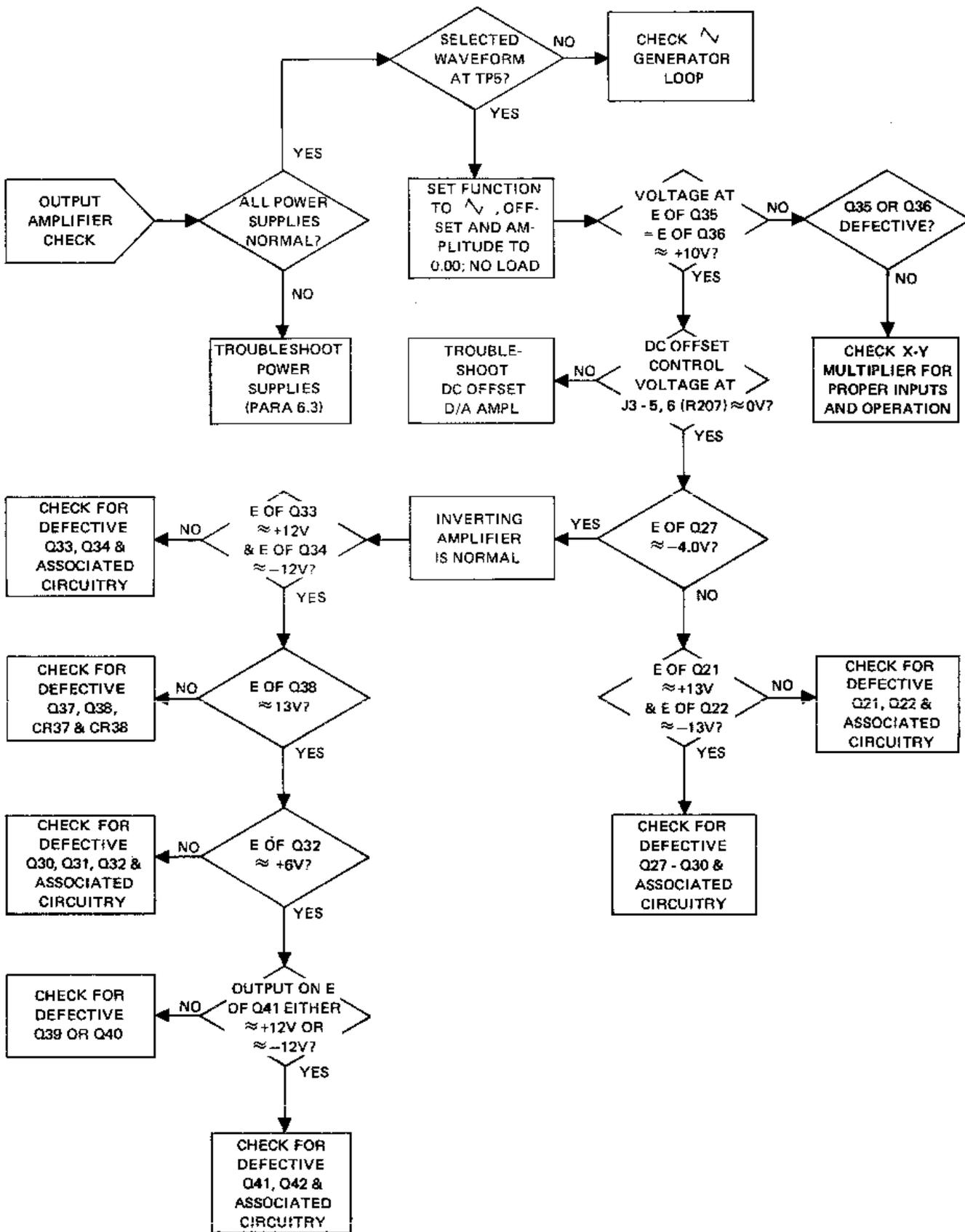


Figure 6-3. Output Amplifier Algorithm

SECTION 7

PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

Drawings	Old Number	New Number
Instrument Schematic	158-200	0004-00-0045
Chassis Assembly	159-000	0102-00-0304
Chassis Parts Lists	159-000	1101-00-0045
Digital Board Schematic	158-218	0103-00-0819
Digital Board Assembly	158-018	0101-00-0819
Digital Board Parts List	158-018	1100-00-0819
Analog Board Schematic	158-219	0103-00-0107
Analog Board Assembly	158-019	0101-00-0107
Analog Board Parts List	158-019	1101-00-0107
Front Panel Assembly	159-046	0102-00-0333
Front Panel Parts List	159-046	1101-00-0075
Key Board Schematic	158-247	0103-00-0109
Key Board Assembly	158-047	0101-00-0109
Key Board Parts List	158-047	1100-00-0109
Display Board Schematic	158-251	0103-00-0105
Display Board Assembly	158-051	0101-00-0105
Display Board Parts List	158-051	1100-00-0105
Rear Panel Assembly	158-034	0102-00-0332
Rear Panel Parts List	158-034	1101-00-0074
Power Supply Schematic	158-220	0103-00-0108
Power Supply Assembly	158-020	0101-00-0108
Power Supply Parts List	158-202	1100-00-0108
158 Instrument Schematic	158-235	0004-00-0081
158 Modification	158-000	0102-00-0303
158 Modification Parts List	158-000	1101-00-0044
158 Front Panel Assembly	158-038	0102-00-0336
158 Front Panel Parts List	158-038	1101-00-0078
158 Cable Assembly	158-039	1203-00-0005

7.3 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

Drawings	Number
005 Interconnect Diagram	0004-00-0080
GPIB Interface Schematic	0103-00-0972
GPIB Interface Assembly	0101-00-0972
GPIB Interface Parts List	1100-00-0972
005 Modification Drawing	0102-00-0351
005 Modification Parts List	1101-00-0229
005 Cable Assembly	1207-00-0004
005 ASCII I/O Cable Assembly	1203-00-0003

REV	ECN	BY	DATE	APP
A	ECN 1133	DJ	2/14/74	
B	ECN 1268	DJ	4-17-74	APS
C	# 1420	David Seltman	3-7-79	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

D

C

B

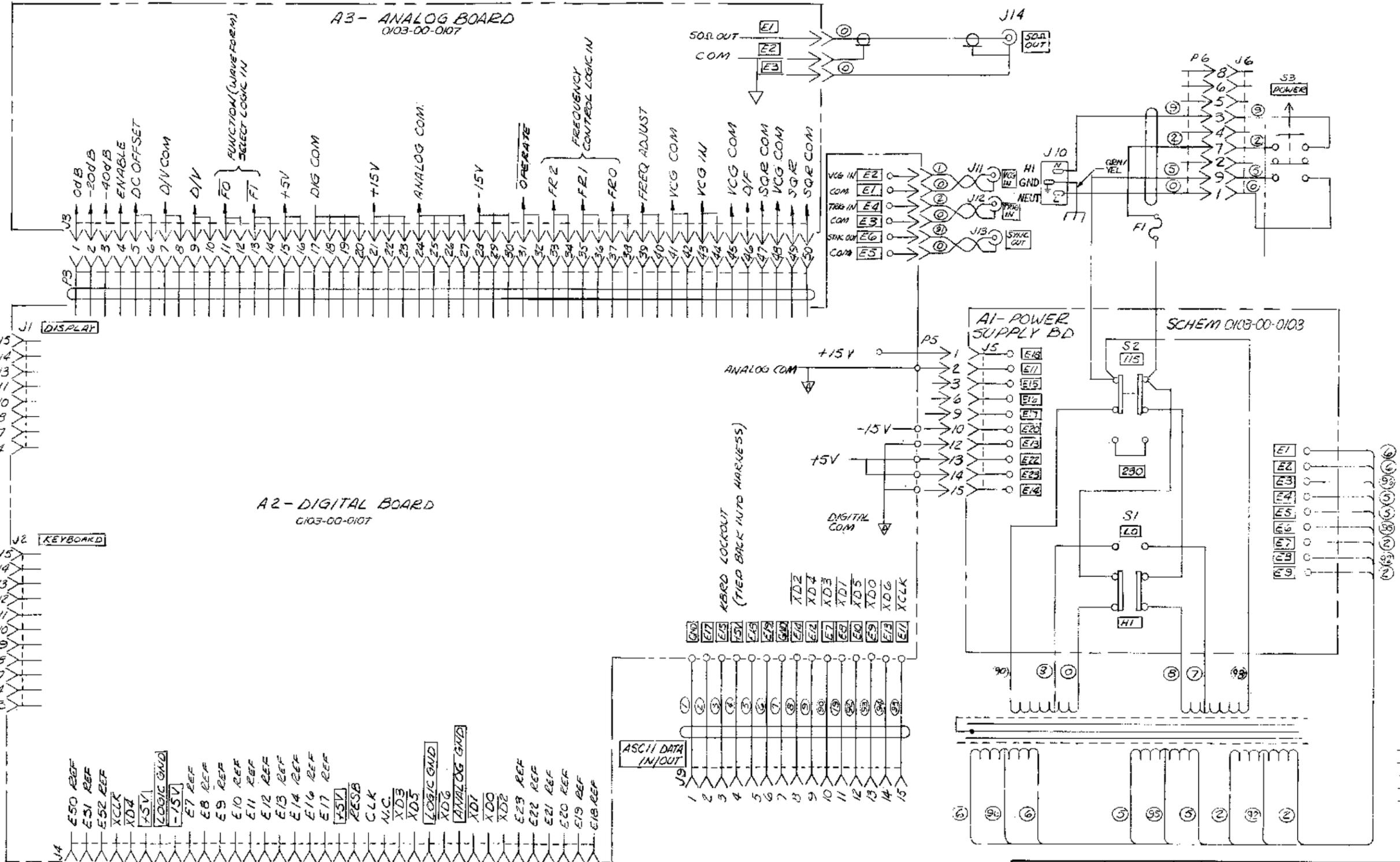
A

D

C

B

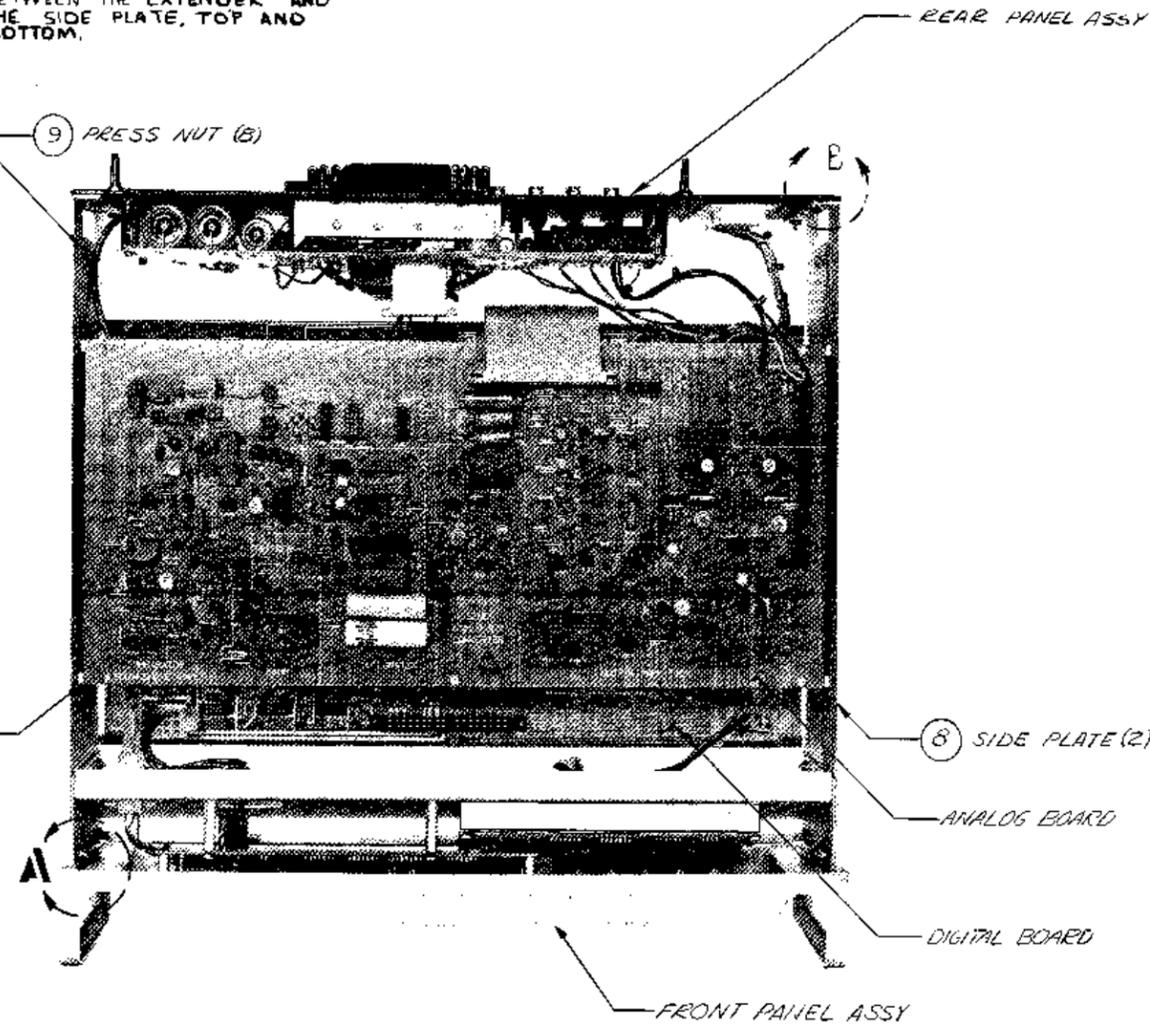
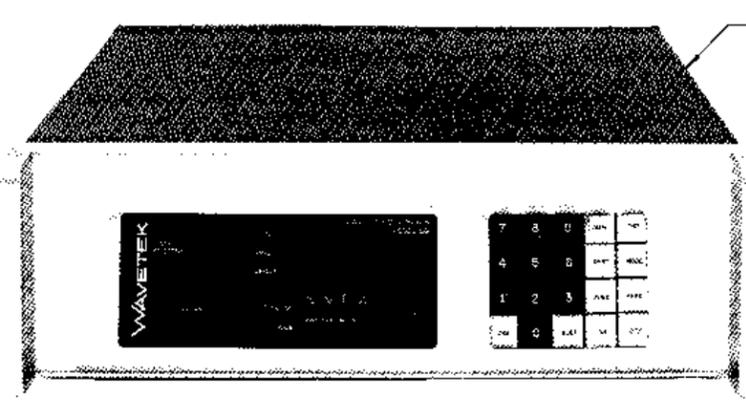
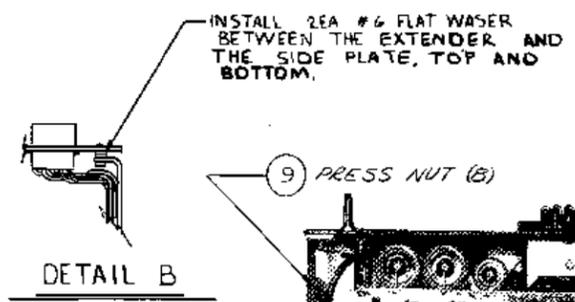
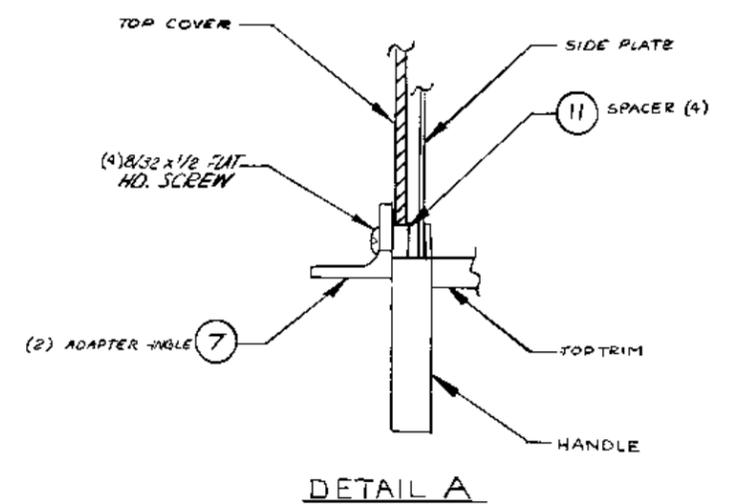
A



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: <i>Ch Cox</i>	DATE: 5-7-74	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL:	PREPARED BY: <i>W. Seltman</i>	DATE: 4/2/74	
FINISH: WAVETEK #PDC:SS	TOLERANCE UNLESS OTHERWISE SPECIFIED: .XX - .010 ANGLES: 1: XX - 030	DO NOT SCALE DWG	INTERCONNECT DIAGRAM -NO OPTION-
SCALE:	MODEL NO. 158/159	DWG NO. 0004-00-0065	
	CODE IDENT: 23338	SHEET: 1 OF 1	

REV	ECN	BY	DATE	APP
A	1069	CE	9/10/78	SP
B	ECN 1125	EG	10/16/78	SP
C	11916	EG	1/25/79	SP
D	ECN 1754	RO	8/2/78	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



TOP VIEW WITH COVERS REMOVED

1. ITEM 6 & 7 ARE NOT SHOWN.
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DESIGNER C.C. Cox	DATE 5/24/78	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	RELEASED BY R.P. Williams	DATE 6/2/78	TITLE ASSEMBLY CHASSIS	
FINISH WAVETEK PROCESS	RELEASED BY APS	DATE 7/1/78	MODEL NO. 159	DWG NO. 0102-00-0304D
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - DIM ANGLES -1 XX - DSD			SCALE NONE	CODE (BY N) 23338
DO NOT SCALE DWG			SHEET	OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
-----	-----	----	------	-----

REFERENCE DESIGNATORS	PART DESCRIPTION	UNIG-MFGR-PART-NO	MFR	WAVETEK NO.	QTY/PCT
NONE	ASST DRNG, CHASSIS	0102-00-0500	WVTK	0102-00-0500	1
5	COVER ASST	150-045	WVTK	1201-00-0039	1
8	PLATE, SIDE	150-310	WVTK	1400-00-0673	2
7	BRKT, ANGLE, R/A	146-375-PAINT	WVTK	1400-00-2712	2
11	SPACER, R/A	147-362	WVTK	1400-00-3693	4
9	INSERT # 6	74-11-106-13	SOTCO	2800-09-0017	8
10	FAST, CHASSIS	1591-011	USECO	2800-09-0022	2
NONE	PKR CORD	0-7700-008-61	PACMD	6001-86-0005	1

WAVETEK PARTS LIST	TITLE STD CHASSIS	ASSEMBLY NO. 1101-00-0045	REV D
	PAGE: 1		

1101-00-0045-001

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO CALIFORNIA
MATERIAL	PROV ENGR	TITLE	
FINISH WAVETEK PROCESS	RELEASE APPROV	CHASSIS	
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± 0.10 ANGLES: 1 XX ± 0.30	MODEL NO	REV
	DO NOT SCALE DWG	158/159	1101-00-0045
SCALE	CODE IDENT	2333B	SHEET 1 OF 1

OPTIONAL INTERFACE
CONVERSION PCA

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

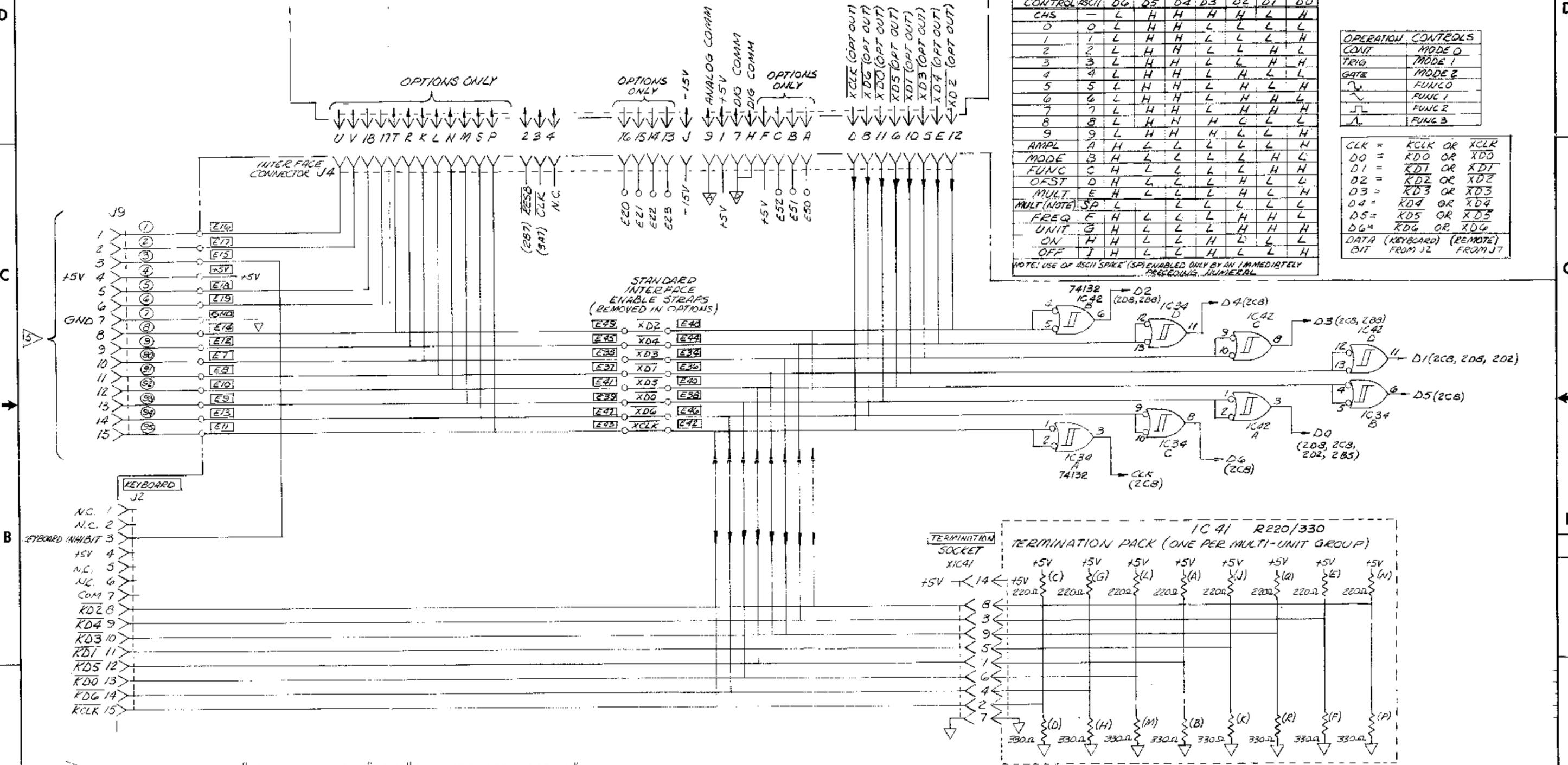
ECN 316D DC 3/10

CONTROL ASCII	D6	D5	D4	D3	D2	D1	D0
CHS	-	L	H	H	H	L	H
0	0	L	H	H	L	L	L
1	1	L	H	H	L	L	H
2	2	L	H	H	L	L	H
3	3	L	H	H	L	L	H
4	4	L	H	H	L	L	L
5	5	L	H	H	L	H	L
6	6	L	H	H	L	H	L
7	7	L	H	H	L	H	H
8	8	L	H	H	L	L	L
9	9	L	H	H	L	L	H
AMPL	A	H	L	L	L	L	H
MODE	B	H	L	L	L	L	H
FUNC	C	H	L	L	L	L	H
OFST	D	H	L	L	L	L	H
MULT	E	H	L	L	L	L	H
MULT (NOTE)	SP	L	L	L	L	L	L
FREQ	F	H	L	L	L	H	L
UNIT	G	H	L	L	L	H	H
ON	H	H	L	L	H	L	L
OFF	I	H	L	L	H	L	H

OPERATION CONTROLS

CONT	MODE 0
TRIG	MODE 1
GATE	MODE 2
⌋	FUNC 0
⌋	FUNC 1
⌋	FUNC 2
⌋	FUNC 3

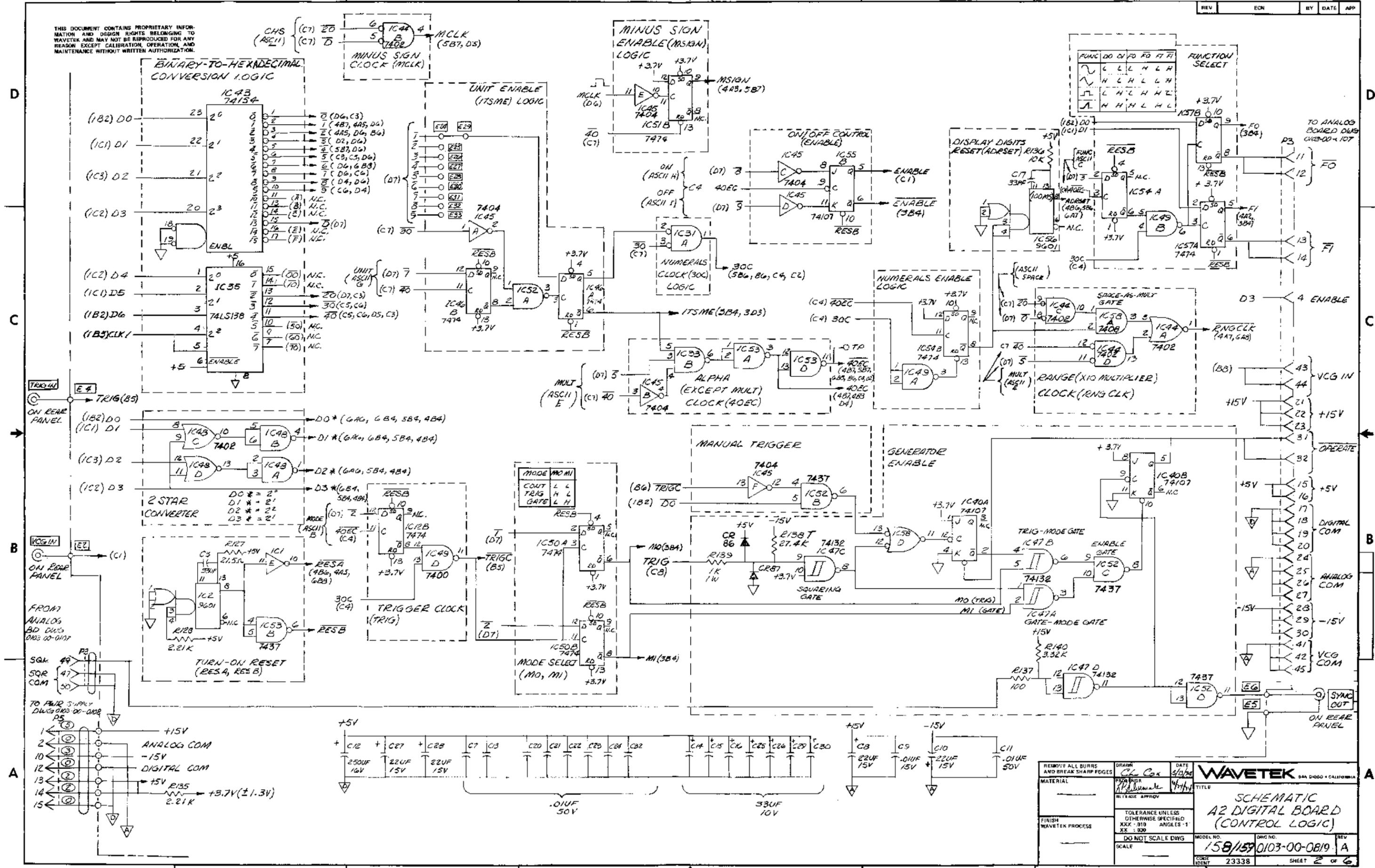
CLK = KCLK OR XCLK
 D0 = KD0 OR XDD
 D1 = KD1 OR XDT
 D2 = KD2 OR XDZ
 D3 = KD3 OR XD3
 D4 = KD4 OR XD4
 D5 = KD5 OR XD5
 D6 = KD6 OR XD6
 DATA (KEYBOARD) (REMOTE)
 BIT FROM J2 FROM J7



5 CONNECTOR FOR "ASCII DATA IN/OUT" OR "ISOLATED ASCII DATA IN" FOR APPROPRIATE PIN ASSIGNMENT SEE INTERCONNECT DIAGRAM.
 4 BAR OVER MNEMONIC DENOTES TRUE-WHEN-LOW.
 3. ○ DENOTES WIRE COLOR PER RESISTOR CODE.
 2. □ DENOTES ACTUAL LABELING ON BOARD.
 1. □* DENOTES OPEN COLLECTOR.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE 5/7/74	
MATERIAL	DR. [Signature]	
FINISH WAVETEK PROCESS	SCALE	TITLE SCHEMATIC A2-DIGITAL BOARD INTERFACE BUS
10% TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 010 ANGLES 1:7 XX - 1:20	DO NOT SCALE DWG	PART NO. 158/159 PART NO. 0103-00-0819 CODE 23338 SHEET 1 OF 6

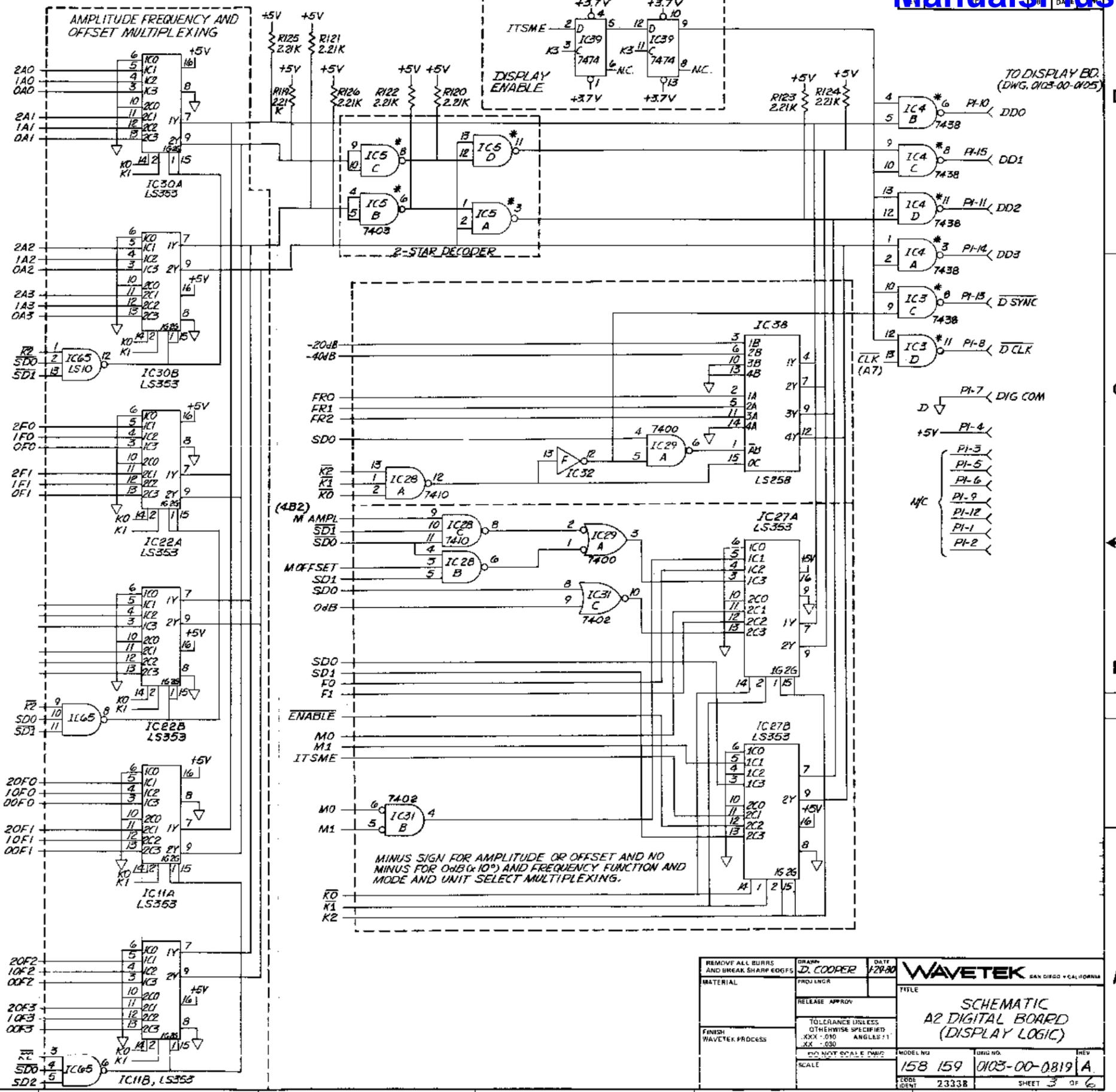
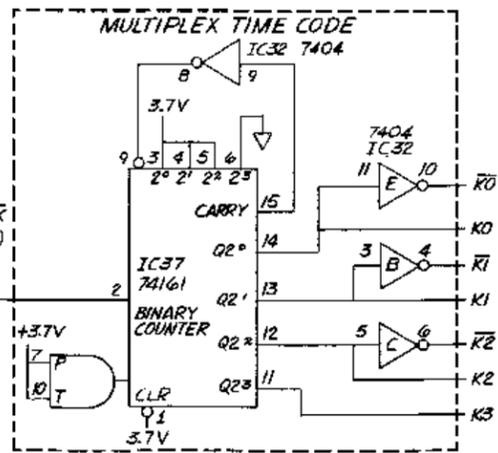
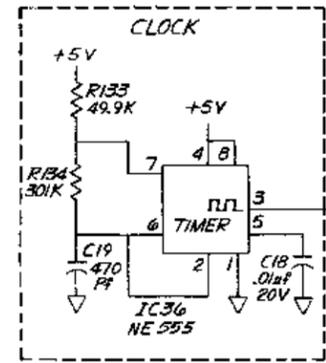
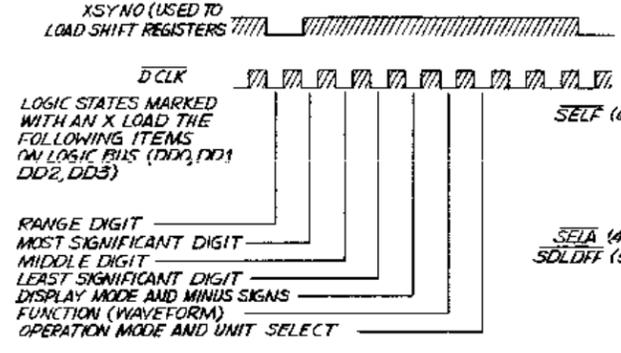
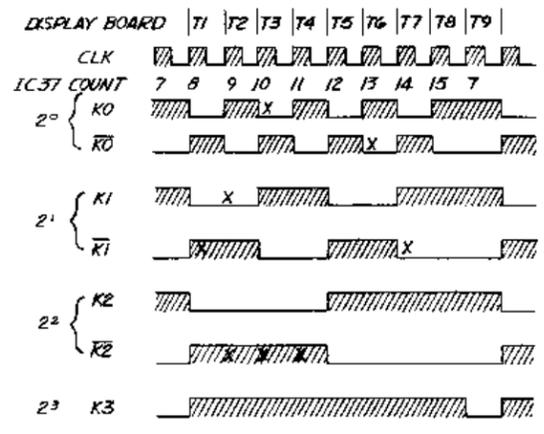
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



REMOVE ALL BURRS AND BREAK SHARP EDGES		DATE: 4/10/79	WAVETEK SANTA CLAYTON, CALIFORNIA
DRAWN: C. Cox		TITLE: SCHEMATIC A2 DIGITAL BOARD (CONTROL LOGIC)	
MATERIAL:	DESIGNED BY: A.P. ...	RELEASE APPROV:	MODEL NO.: 158/159
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX - 010 ANGLES - 1 XX - 030	DO NOT SCALE DWG	DWG NO.: 0103-00-0819
SCALE:	SCALE:	SCALE:	REV: A
CODE IDENT: 23338		SHEET 2 OF 6	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

MULTIPLEX LOGIC FOR DISPLAY BUS (DDO DD1 DD2 DD3)

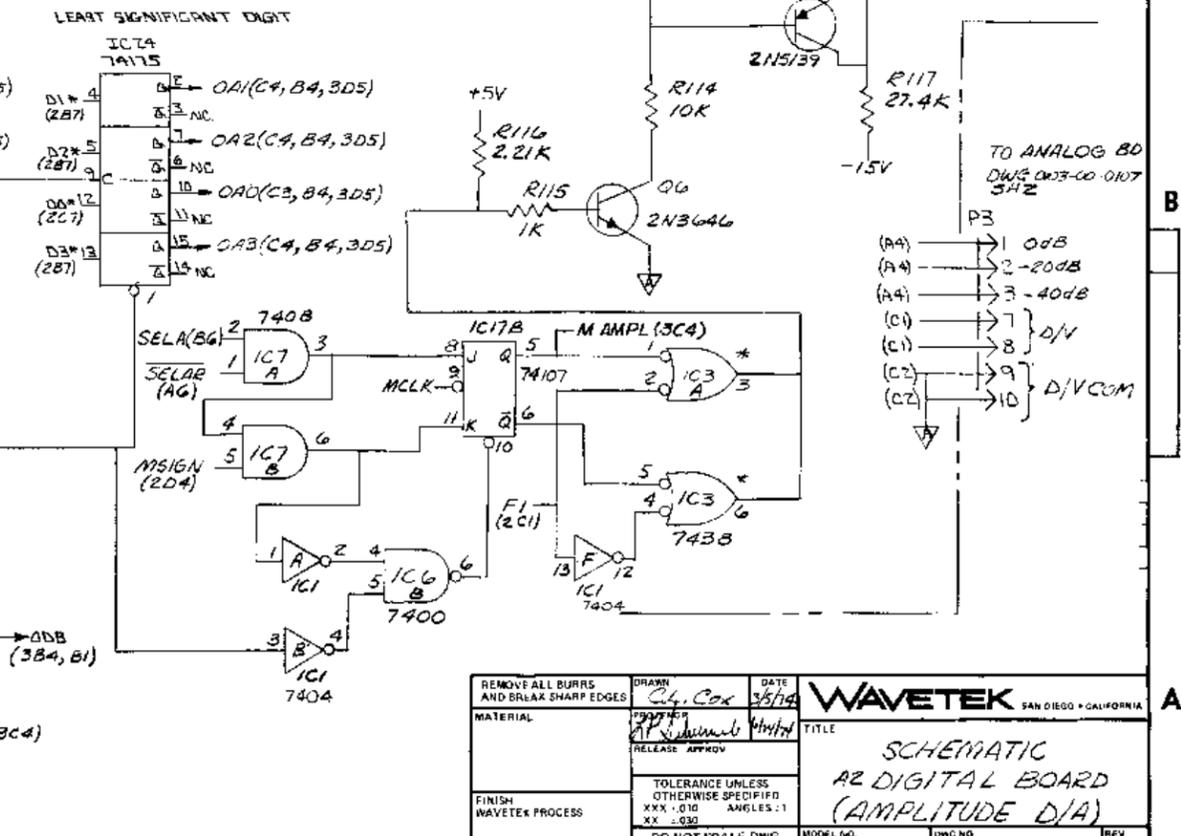
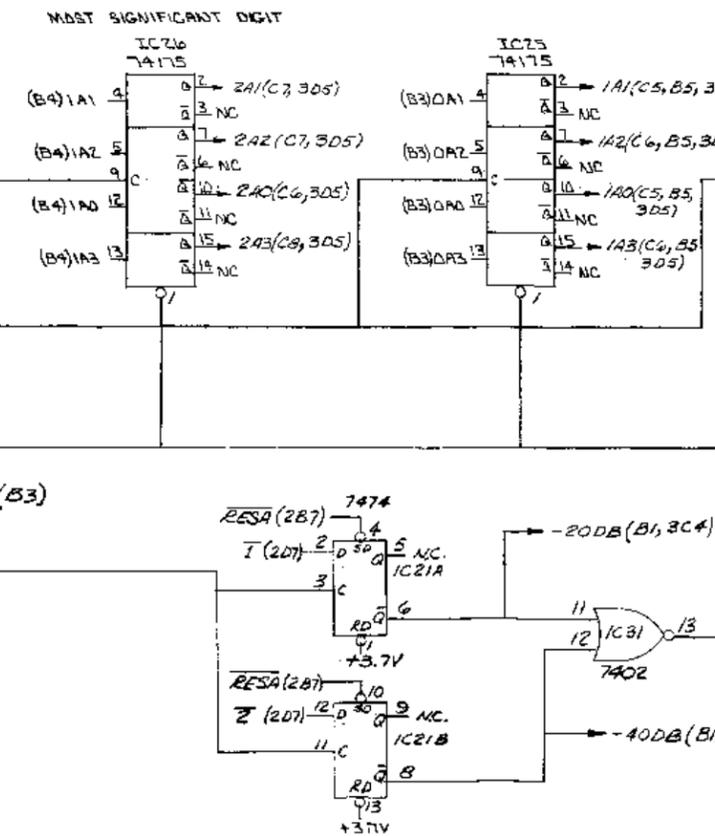
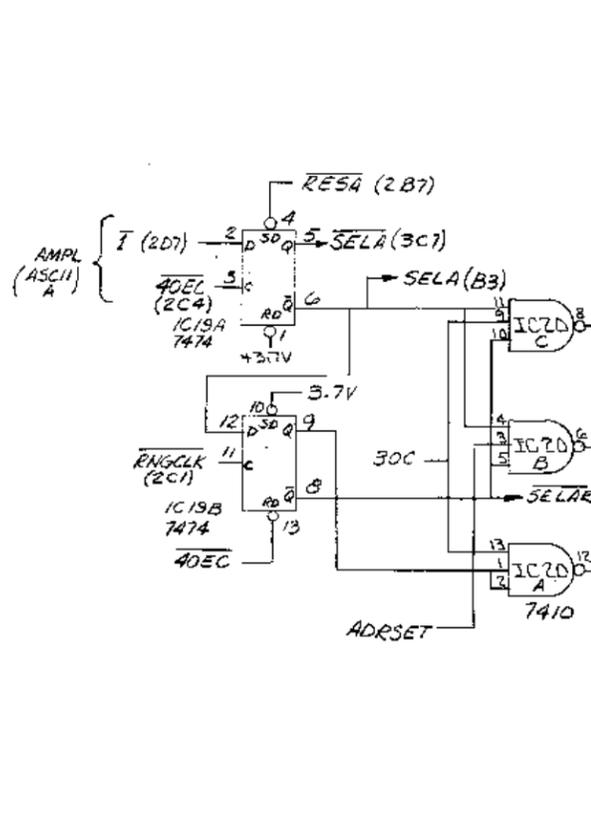
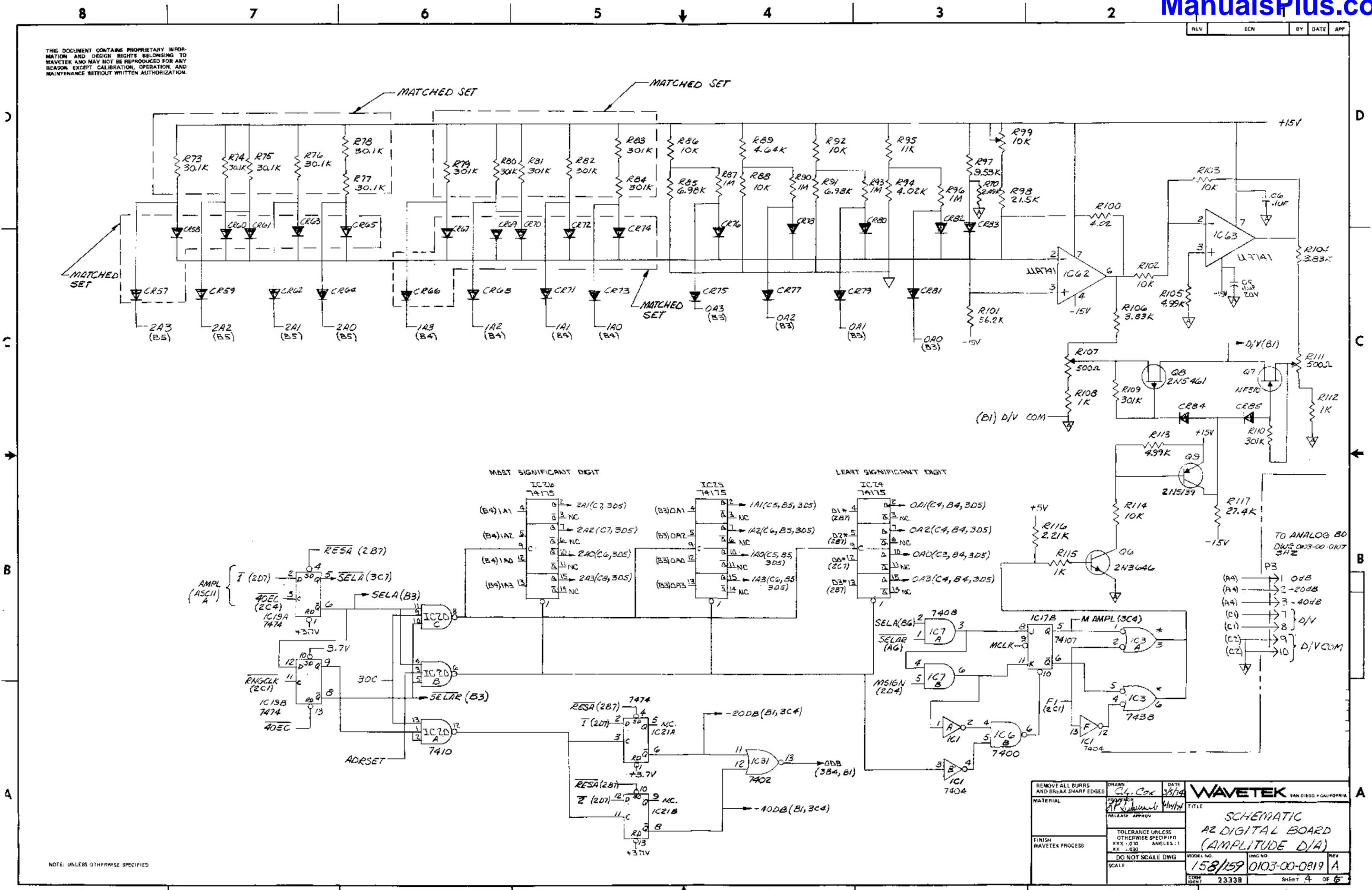


MINUS SIGN FOR AMPLITUDE OR OFFSET AND NO MINUS FOR OdB (x 10) AND FREQUENCY FUNCTION AND MODE AND UNIT SELECT MULTIPLEXING.

Table with 4 columns: REMOVE ALL BURRS AND BREAK SHARP EDGES, DRAWN BY, DATE, TITLE, FINISH WAVETEK PROCESS, RELEASE APPROV, TOLERANCE UNLESS OTHERWISE SPECIFIED, MODEL NO, SHEET 3 OF 6.

NOTE UNLESS OTHERWISE SPECIFIED

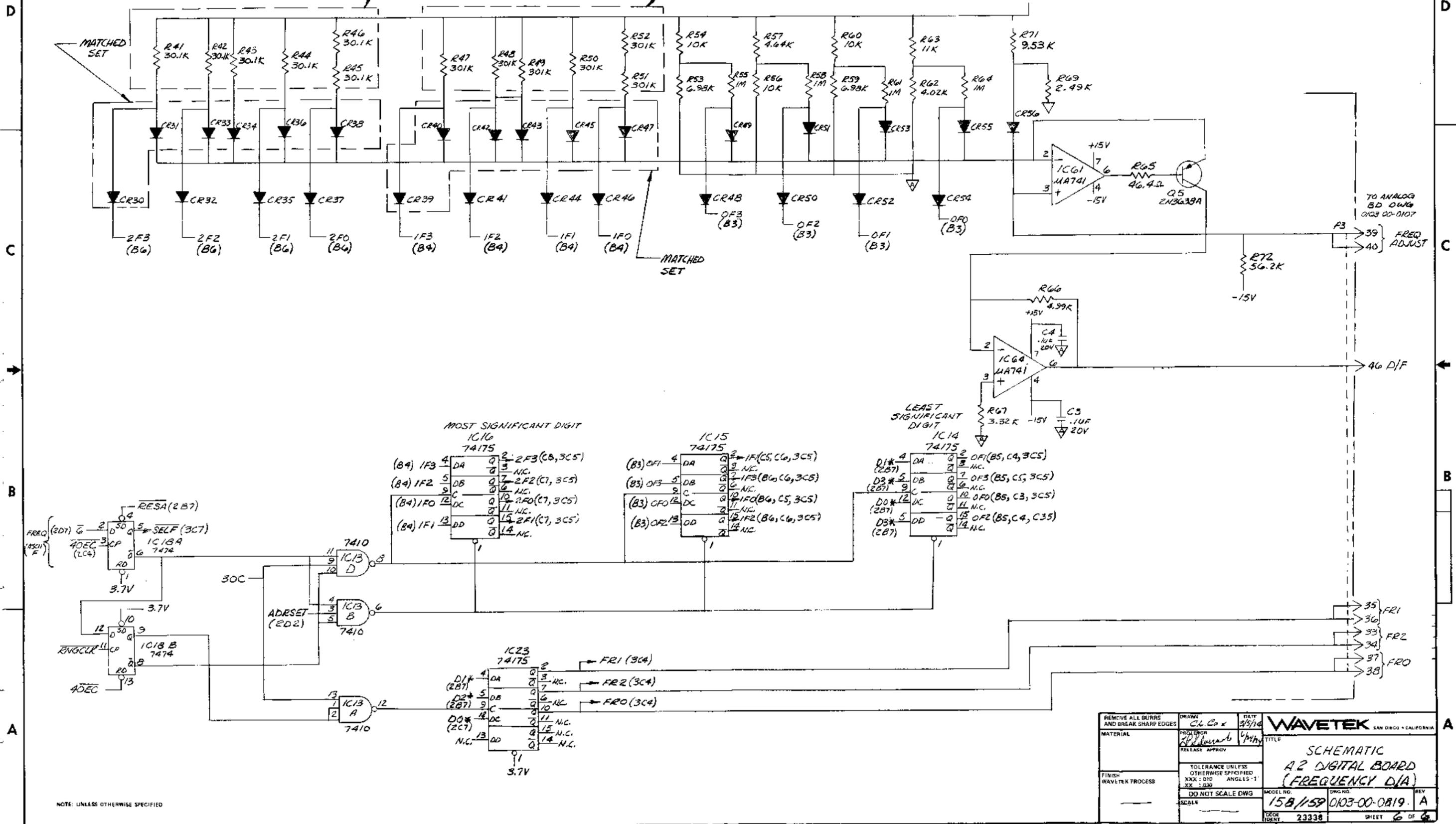
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



REMOVE ALL BURRS AND DEBRASS SHARP EDGES	DATE 3/5/74	
MATERIAL	DRIVER C. Cox	
FINISH WAVETEK PROCESS	RELEASE APPROV	TITLE
	TOLERANCE UNLESS OTHERWISE SPECIFIED	SCHEMATIC
	XXX .010 ANGLES .1	RZ DIGITAL BOARD
	XX .030	(AMPLITUDE D/A)
	DO NOT SCALE DWG	MODEL NO.
	SCALE	158/159
		DWG NO.
		0103-00-0819
		REV
		A
		CODE IDENT
		2333B
		SHEET 4 OF 6

NOTE: UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



MOST SIGNIFICANT DIGIT
IC10
7415

(B4) IF3	4	DA	0	2	2F3 (C6, 3C5)
			1	3	N.C.
(B4) IF2	5	DB	0	7	2F2 (C7, 3C5)
			1	8	N.C.
(B4) IF0	12	DC	0	10	2F0 (C7, 3C5)
			1	11	N.C.
(B4) IF1	13	DD	0	15	2F1 (C7, 3C5)
			1	14	N.C.

IC15
7415

(B3) OF1	4	DA	0	2	1F (C5, C6, 3C5)
			1	3	N.C.
(B3) OF3	5	DB	0	7	1F3 (B6, C6, 3C5)
			1	8	N.C.
(B3) OF0	12	DC	0	10	1F0 (B6, C5, 3C5)
			1	11	N.C.
(B3) OF2	13	DD	0	15	1F2 (B6, C6, 3C5)
			1	14	N.C.

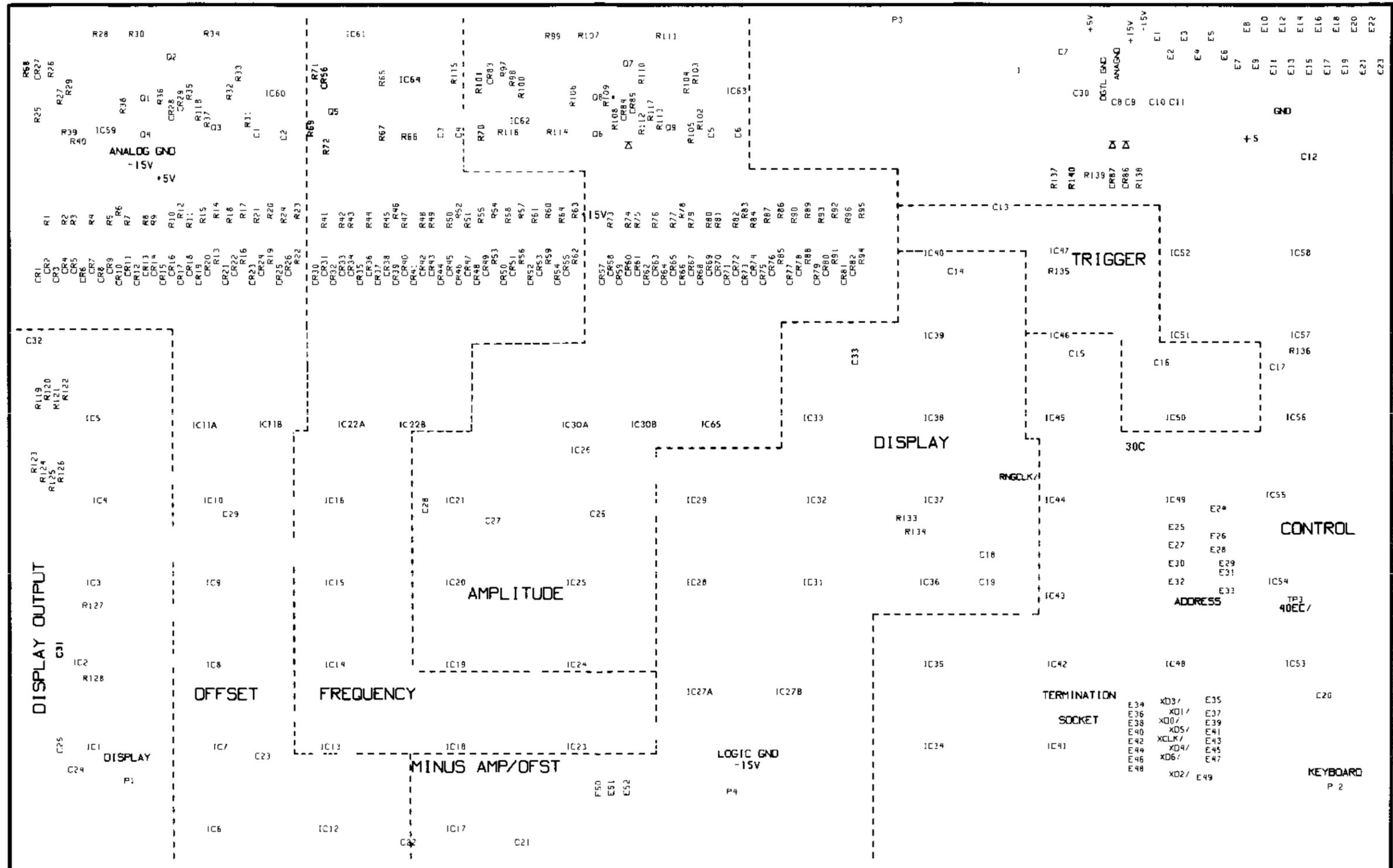
LEAST SIGNIFICANT DIGIT
IC14
7415

D1*	4	DA	0	2	OF1 (B5, C4, 3C5)
(2B7)			1	3	N.C.
D3*	5	DB	0	7	OF3 (B5, C5, 3C5)
(2B7)			1	8	N.C.
D0*	12	DC	0	10	OF0 (B5, C3, 3C5)
(2B7)			1	11	N.C.
D3*	5	DD	0	15	OF2 (B5, C4, 3C5)
(2B7)			1	14	N.C.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN C.L. Co x	DATE 3/5/74	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROFESSOR R. J. ...	RELEASE APPROV C. ...	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : DID ANGLES -1 XX : 0.030		TITLE SCHEMATIC A2 DIGITAL BOARD (FREQUENCY D/A)
SCALE	DO NOT SCALE DWG	MODEL NO. 15B/159	REV A
		DWG NO. 0103-00-0819	REV A
		SCALE	CODE IDENT 23338
			SHEET 6 OF 6

NOTE: UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	TITLE	
FINISH WAVETEK PROCESS	SCALE	PCA DIGITAL BD.
FORM 159	0101-00-0819	KEYBOARD P 2
23338	SHEET	OF

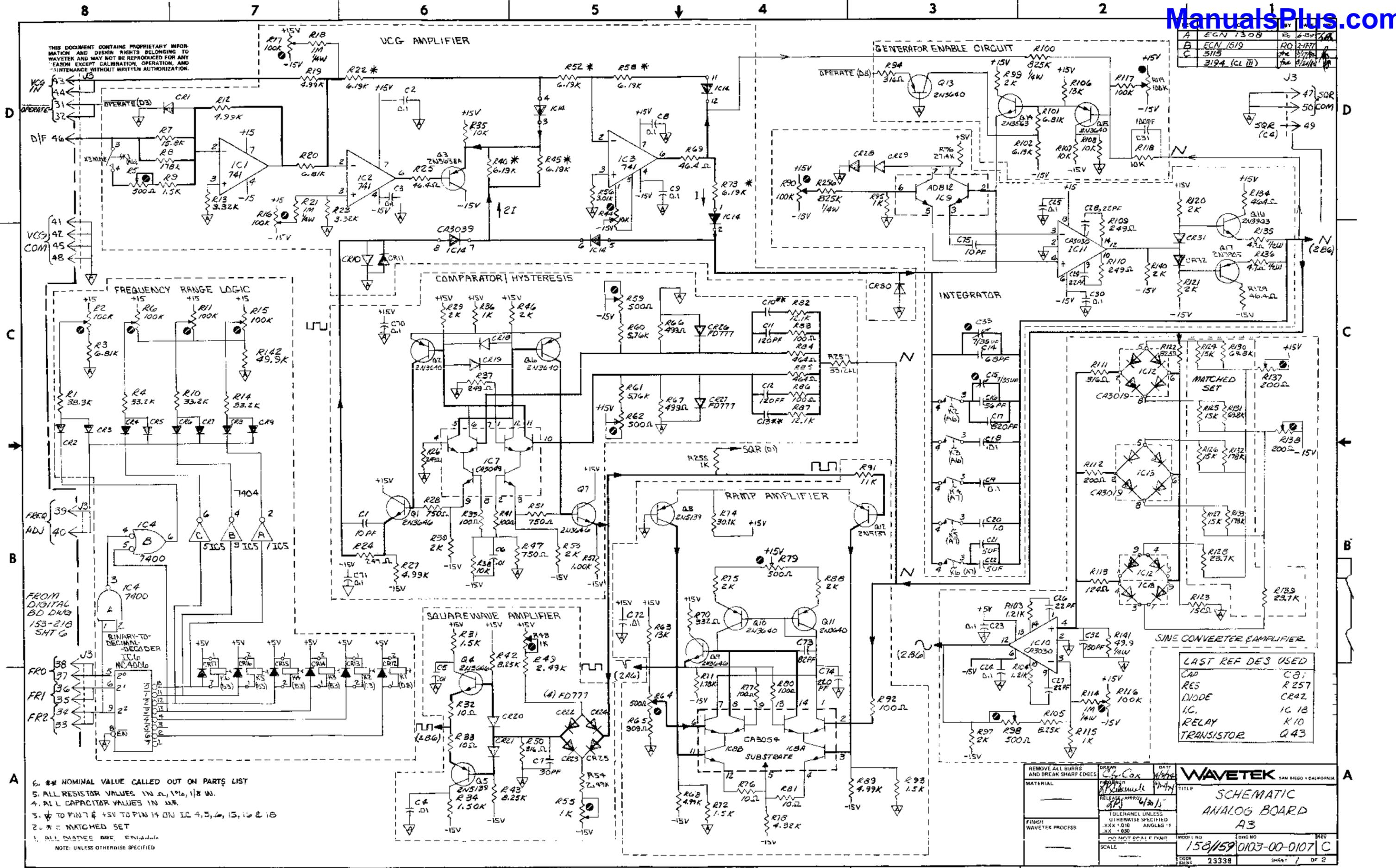
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

Table with 3 columns of parts lists. Each column includes headers for REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFR-PART-NO, MFR, WAVETEK NO., and QTY/PT. The first column lists components like ASSY DRWG, DIGITAL BD, CABLE ASSY, etc. The second column lists resistors (RES. MF, 1/8W, 1%, 21.5, etc.). The third column lists various integrated circuits (IC14, CR14, CR30, etc.).

Table with 3 columns of parts lists. Each column includes headers for REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFR-PART-NO, MFR, WAVETEK NO., and QTY/PT. The first column lists connectors (PIN, FEMALE; PIN, MALE; TRANSIAD), trimmers (PDT. TRIM, 1K), and diodes. The second column lists resistors (RES. MF, 1/8W, 1%, 6.98K, etc.) and diodes. The third column lists integrated circuits (IC9, IC12, IC18, etc.).

WAVETEK PARTS LIST form. Includes fields for DRAWN, DATE, PROJ ENGR, RELEASE APPROV, TOLERANCE UNLESS OTHERWISE SPECIFIED, DO NOT SCALE DWG, MODEL NO. 159, DWG NO. 1100-00-0819, and SHEET OF.

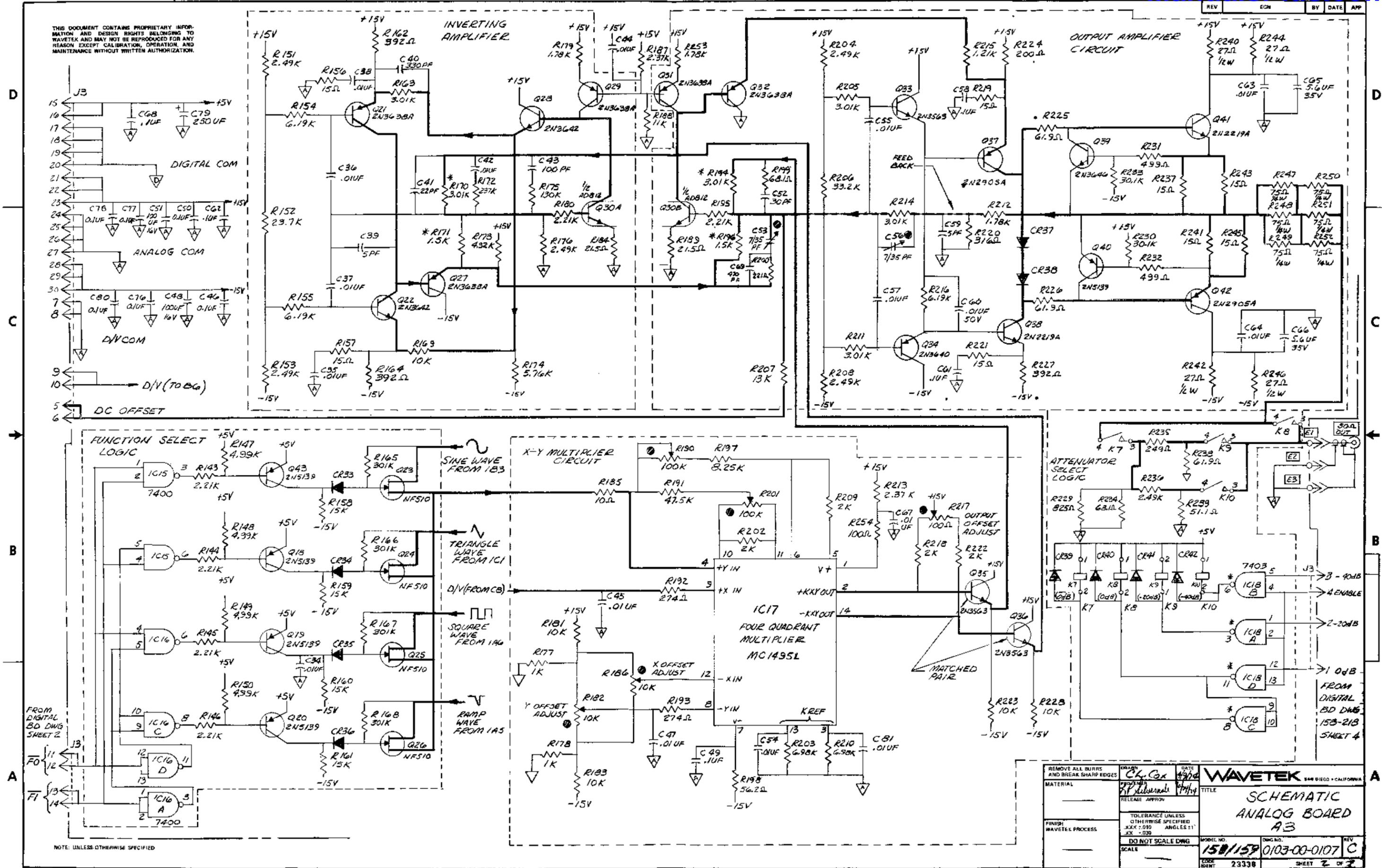
NOTE UNLESS OTHERWISE SPECIFIED



A	ECN 1308	REV	4-30-71
B	ECN 1519	REV	2-11-72
C	3115	REV	3-17-72
	3194 (CL III)	REV	8-24-71

WAVETEK	SAN DIEGO • CALIFORNIA
TITLE	
SCHEMATIC	
ANALOG BOARD	
A3	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



NOTE: UNLESS OTHERWISE SPECIFIED

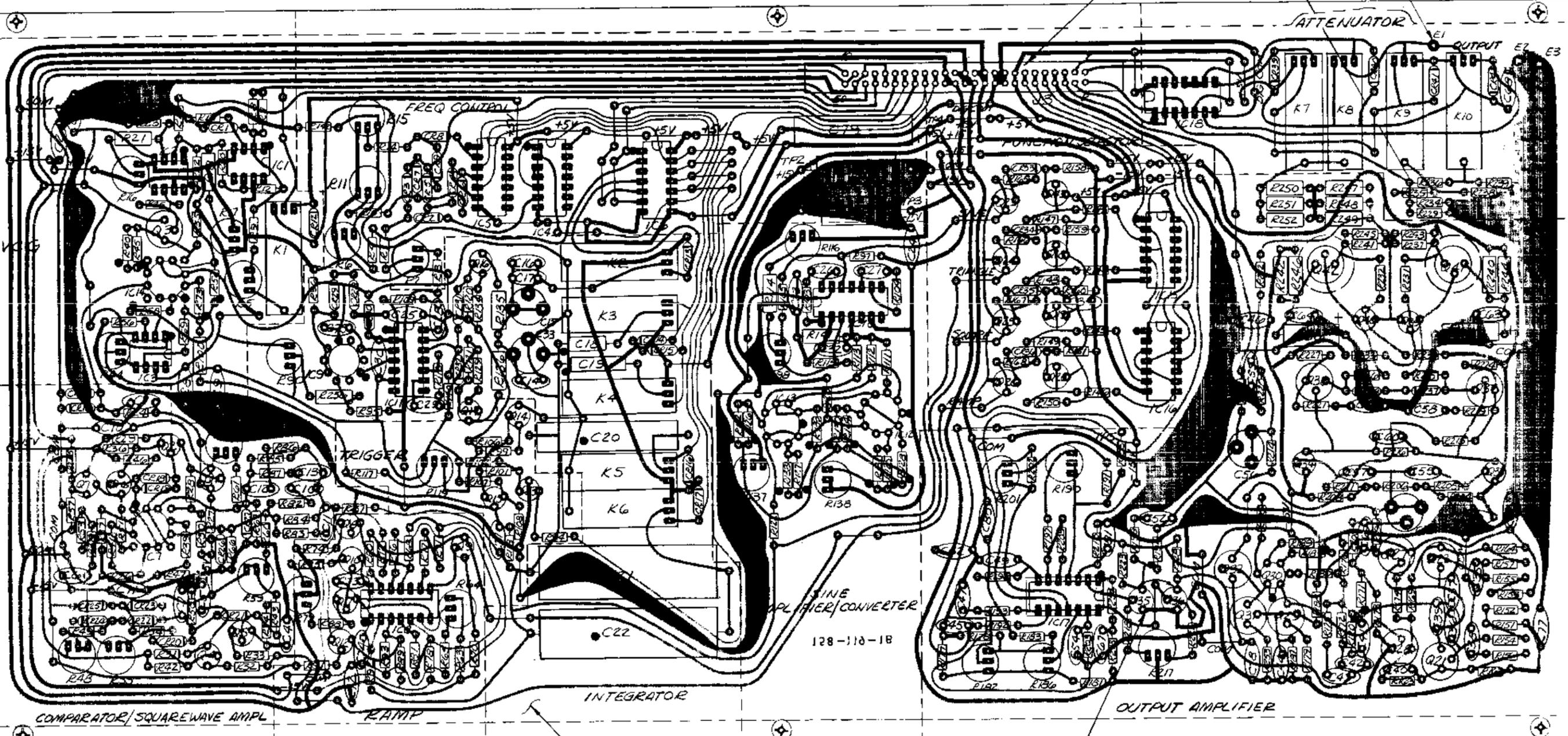
REMOVE ALL BURRS AND BREAK SHARP EDGES		DATE: 4/9/74	REV: 1
MATERIAL		DESIGNED BY: J. Edwards	RELEASE APPROV: [Signature]
FINISH: WAVETEK PROCESS		TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX - .010 ANGLES 1:1 XX - .030 DO NOT SCALE DWG	
SCALE		MODEL NO.: 150/157	DWG NO.: 0103-00-0107 C
SCALE IDENT: 23338		SHEET 2 OF 2	

WAVETEK 344 DIEGO • CALIFORNIA

TITLE: SCHEMATIC ANALOG BOARD A3

J	2644	LOU 5-5-81	RBG	C	ECN 1178	R	1-1-81	105
K	3115	JAN 4/17/82		D	ECN 1303	RO	6-10-81	108
	3167 (CLB)	JAN 5/20/82		E	ECN 1308	RO	6-8-81	108
				F	ECN 1519	RO	2-7-82	
				G	ECN 1754	RO	6-9-82	
				H	ECN 2153	UTE	5-4-84	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



1. * NOMINAL VALUE CALLED OUT ON PARTS LIST
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRW: CL Cox	DATE: 4/2/82	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJ: P. C. BOARD	REV: 4/15	
FINISH: WAVETEK PROCESS	RELEASE: APPROV: RB	SCALE: 2:1	MODEL NO: 158/159
			DWG NO: 0101-00-0107
			CODE: 23338
			SHEET 1 OF 1

0101-00-0107

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

Table with 3 columns: Reference Designators, Part Description, and Qty/Pt. Includes assembly info for Wavetek Parts List, Title Analog, and Assembly No. 1100-00-0107, Page 1.

Table with 3 columns: Reference Designators, Part Description, and Qty/Pt. Includes assembly info for Wavetek Parts List, Title Analog, and Assembly No. 1100-00-0107, Page 2.

WAVETEK SAN DIEGO CALIFORNIA PARTS LIST PCA ANALOG BD. Includes fields for DRAWN, DATE, PROJECT, RELEASE, APPROV, TOLERANCE, MODEL NO. 159, and SHEET 1 OF 2.

NOTE: UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATIONAL AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
R129 R134 R25 R69	RES. MF. 1/8W. 1%. 46. 4	RN55D-4684F	TRW	4701-03-4649	4
R191	RES. MF. 1/8W. 1%. 47. 3K	RN55D-4752F	TRW	4701-03-4752	1
R231 R232 R66 R67	RES. MF. 1/8. 1%. 499	RN55D-4990F	TRW	4701-03-4990	4
R12 R147 R145 R149 R130 R19 R27 R68 RB9	RES. MF. 1/8W. 1%. 4. 99K	RN55D-4991F	TRW	4701-03-4991	9
R142	RES. MF. 1/8W. 1%. 49. 9K	RN55D-4992F	TRW	4701-03-4992	1
R239	RES. MF. 1/8W. 1%. 51. 1	RN55D-5181F	TRW	4701-03-5119	1
R198	RES. MF. 1/8W. 1%. 56. 2	RN55D-5622F	TRW	4701-03-5629	1
R174 R60 R61	RES. MF. 1/8W. 1%. 5. 76K	RN55D-5761F	TRW	4701-03-5761	3
R102 R194 R155 R216	RES. MF. 1/8W. 1%. 6. 19K	RN55D-6191F	TRW	4701-03-6191	4
R225 R226 R238	RES. MF. 1/8W. 1%. 61. 9	RN55D-6199F	TRW	4701-03-6199	3
R131 R20 R2	RES. MF. 1/8W. 1%. 6. 81K	RN55D-6811F	TRW	4701-03-6811	3
R199 R234	RES. MF. 1/8W. 1%. 68. 1	RN55D-6881F	TRW	4701-03-6819	2
R203 R210	RES. MF. 1/8W. 1%. 6. 98K	RN55D-6981F	TRW	4701-03-6981	2
R28 R47 R51	RES. MF. 1/8W. 1%. 750	RN55D-7500F	TRW	4701-03-7500	3
R229	RES. MF. 1/8W. 1%. 825	RN55D-8250F	TRW	4701-03-8250	1
R103 R197 R42 R43	RES. MF. 1/8W. 1%. 8. 25K	RN55D-8251F	TRW	4701-03-8251	4
R122	RES. MF. 1/8W. 1%. 82. 5	RN55D-8285F	TRW	4701-03-8259	1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
R132 R133	RES. MF. MIXED SET RES. MF. 1/8W. 1%. 178K PART OF 4789-00-0032 QTY(2)			4789-00-0032	
CR22 CR23 CR24 CR25 CR26 CR27	DIODE	FD-777	FAIR	4807-02-0777	6
CR1 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR21 CR28 CR29 CR3 CR30 CR31 CR32 CR33 CR34 CR35 CR36 CR37 CR38 CR39 CR4 CR40 CR41 CR42 CR5 CR6 CR7 CR8 CR9	DIODE	FD-6666	FAIR	4807-02-6666	36
Q38 Q41	TRANS	2N2219A	NSC	4901-02-2191	2
Q37 Q42	TRANS	2N2905A	NSC	4901-02-9051	2
Q14 Q33	TRANS	2N3962	FAIR	4901-03-5630	2
Q21 Q27 Q29 Q3 Q31 Q32	TRANS	2N3638A	CARTR	4901-03-6381	6
Q10 Q11 Q13 Q15 Q2 Q34 Q6	TRANS	2N3640	FAIR	4901-03-6400	7
Q22 Q28	TRANS	2N3642	FAIR	4901-03-6420	2
Q1 Q39 Q4 Q7 Q9	TRANS	2N3646	NSC	4901-03-6460	5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
IC15 IC16 IC4	IC	7400	TI	8000-74-0000	3
IC18	IC	7403	TI	8000-74-0300	1
IC5	IC	7404	TI	8000-74-0400	1

WAVETEK PARTS LIST
TITLE ANALOG
ASSEMBLY NO. 1100-00-0107
PAGE: 7
REV L

WAVETEK PARTS LIST
TITLE ANALOG
ASSEMBLY NO. 1100-00-0107
PAGE: 9
REV L

WAVETEK PARTS LIST
TITLE ANALOG
ASSEMBLY NO. 1100-00-0107
PAGE: 11
REV L

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
R65	RES. MF. 1/8W. 1%. 909	RN55D-9090F	TRW	4701-03-9090	1
R114 R18 R21	RES. MF. 1/4W. 1%. 1K	RN60D-1004F	TRW	4701-13-1004	5
R141	RES. MF. 1/4W. 1%. 49. 9	RN60D-4999F	TRW	4701-13-4999	1
R247 R248 R249 R250 R251 R252	RES. MF. 1/4W. 1%. 75	RN60D-7500F	TRW	4701-13-7509	6
R100 R256	RES. MF. 1/4W. 1%. 825K	RN60D-8250F	TRW	4701-13-8250	2
R171 R196	RES. SET. 2-1. 5K. 1/8W QTY: 2: 4701-03-1501	158-501-95A	WVTK	4789-00-0008	1
R170 R194	RES. SET. 2-3. 01K. 1/8W QTY: 2: 4701-03-3041	157-501-26A	WVTK	4789-00-0012	1
R22 R40 R45 R52 R58 R73	RES. SET. 6-6. 19K. 1/8W QTY: 6: 4701-03-6191	130-501-3A	WVTK	4789-00-0016	1
	RES. MF. MIXED SET	130-501-5A	WVTK	4789-00-0032	1
R124 R125 R126 R127	RES. MF. 1/8W. 1%. 15K PART OF 4789-00-0032 QTY(4)				
R128 R139	RES. MF. 1/8W. 1%. 23. 7K PART OF 4789-00-0032 QTY(2)				
R130 R131	RES. MF. 1/8W. 1%. 69. 8K PART OF 4789-00-0032 QTY(2)				

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
Q16	TRANS	2N3903	NSC	4901-03-9030	1
Q17	TRANS	2N3905	ITT	4901-03-9050	1
Q12 Q18 Q19 Q20 Q40 Q42 Q5 Q8	TRANS	2N5139	FAIR	4901-05-1390	8
Q23 Q24 Q25 Q26	TRANS	NF-510	NSC	4902-00-5100	4
Q25 Q26	TRANS. M/P.R. 2N3563 QTY: 2: 4901-03-5630	142-501-52	WVTK	4998-00-0004	1
IC1 IC2 IC3	IC	MA-741	FAIR	7000-07-4100	3
IC9 Q30	IC	AD 812	ANDEV	7000-08-1200	2
IC17	IC	MC1495L	MDT	7000-14-9500	1
IC12 IC13	IC	CA-3019	FAIR	7000-30-1900	2
IC7	IC	CA-3049	RCA	7000-30-4900	1
IC8	IC	CA-3054	RCA	7000-30-5400	1
IC11	IC. CLASS I. CA-3030 QTY: 1: 7000-30-3000	130-501-15	WVTK	7200-00-0001	1
IC10	IC. CLASS II. CA-3030 QTY: 1: 7000-30-3000	130-501-16	WVTK	7200-00-0032	1
IC14	IC. CLASS I. CA-3039 QTY: 1: 7000-30-3900	130-501-18	WVTK	7200-00-0004	1
IC6	IC	4006	MDT	8000-40-0600	1

WAVETEK PARTS LIST
TITLE ANALOG
ASSEMBLY NO. 1100-00-0107
PAGE: 8
REV L

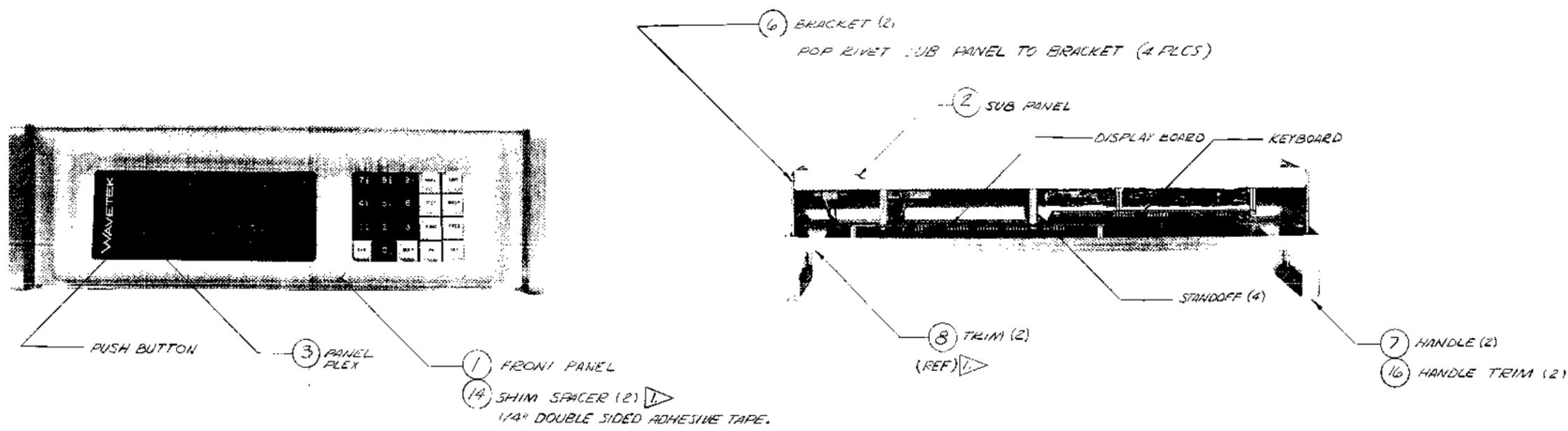
WAVETEK PARTS LIST
TITLE ANALOG
ASSEMBLY NO. 1100-00-0107
PAGE: 10
REV L

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	DESIGNER		
FINISH WAVETEK PROCESS	RELEASE APPROV		TITLE PARTS LIST PCA ANALOG BD
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES .1° XX ±.000		
	DRAWN SCALE UNLESS		
	SCALE		
	159	1100-00-0107	L
	CODE 23338	SHEET 2 OF 2	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

A	CHG DWG NO. FROM 159-001 ECN 1161	DATE 9/27	BY [Signature]
B	ECN 1160	DATE 11/20/88	BY [Signature]
C	ORD ASSY WAS 158-016 DELETED ITEM IS 154-331 ECN 1131	DATE 11/17	BY [Signature]
D	ECN 1288	DATE 6/25/88	BY [Signature]
E	ECN 1754	DATE 6/24/88	BY [Signature]



INSTALL SHIM SPACER BEHIND FRONT PANEL USING 1/4" DOUBLE SIDED TAPE, BEFORE ADDING TRIM.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CL Cox	DATE 3/2/88	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJ ENGR SP [Signature]	DATE 4/11/88	
FINISH WAVETEK PROCESS	RELEASE APPROVAL [Signature]	DATE 4/11/88	TITLE ASSEMBLY FRONT PANEL
	TDI FRANC JUNE 88 OTHERWISE SPECIFIED XXX - 010 ANGLES - 1 XX - 030	SCALE NONE	PART NO 159
	DO NOT SCALE DWG	SCALE	DWG NO 0102-00-0333
			SHEET / OF / CODE 23338

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
-----	-----	----	------	-----

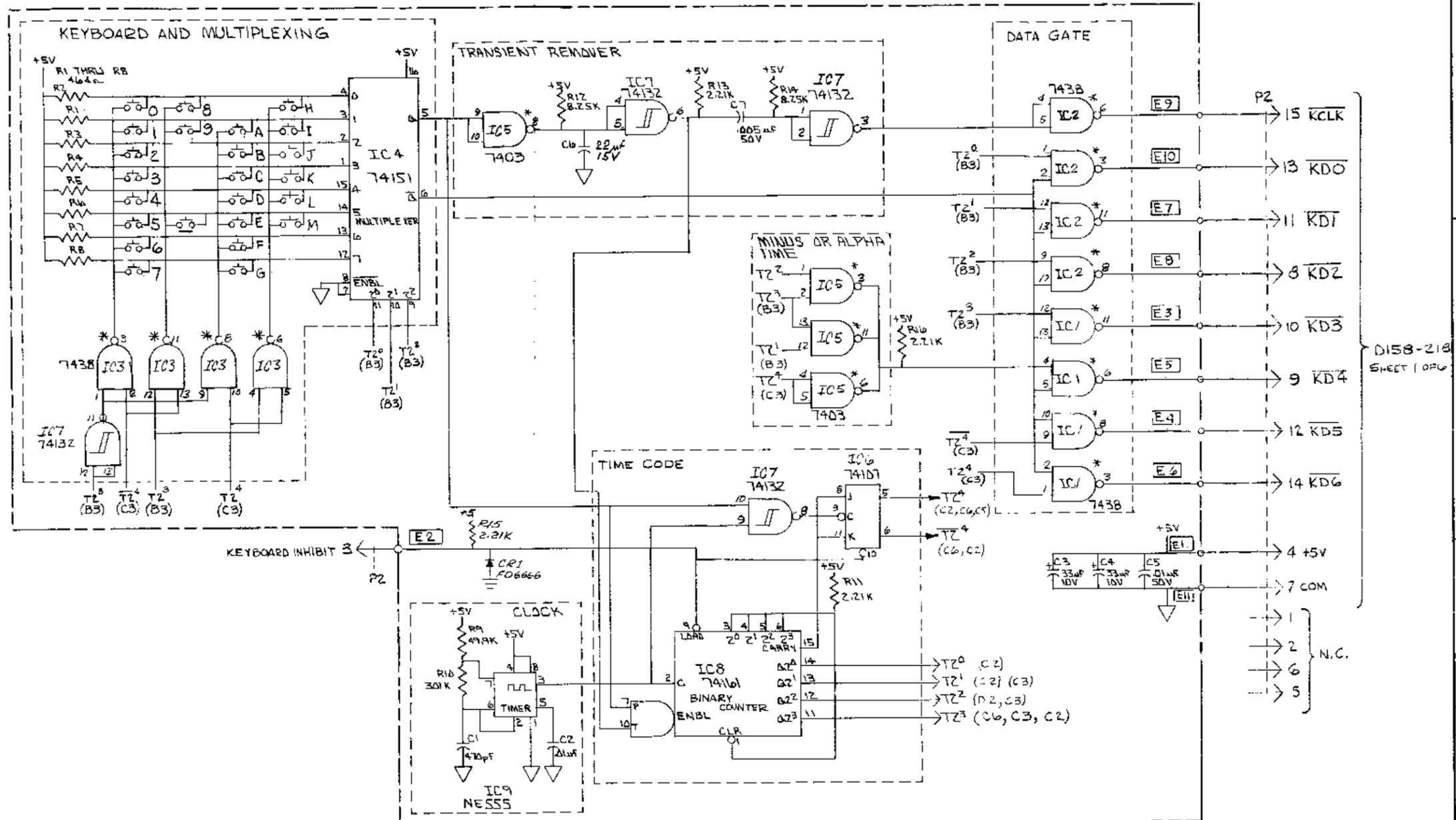
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGN-PART-NO	MFR	WAVETEK NO.	QTY/PT
NONE	ASSY DRNG. FRONT PNL	0102-00-0333	WVTK	0102-00-0333	1
1	PANEL FT REF:1300-03-0002	150-309	WVTK	1400-00-0660	1
3	PANEL P-1A	150-314	WVTK	1400-00-0690	1
2	PANEL SUB	150-323	WVTK	1400-00-0723	1
6	BKKT	150-324	WVTK	1400-00-0733	2
7	HANDLE, W/C FROM:1400-00-3501	147-364	WVTK	1400-00-3589	2
10	TRIM, HANDLE REF:1300-06-0000	147-365	WVTK	1400-00-3619	2
14	SHIM, SPACER	1400-00-7005	WVTK	1400-00-7005	2
8	TRIM REF:1300-06-0005	1400-00-7019	WVTK	1400-00-7019	2
NONE	SPACER	0221-A-0652	AMCOM	2000-02-0012	4

WAVETEK PARTS LIST	TITLE FT PANEL ASSY	ASSEMBLY NO. 1101-00-0075	REV E
	PAGE: 1		

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		
FINISH WAVETEK PROCESS	BELLASE APPROV	TITLE FRONT PANEL ASSY	
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES 1° XX ± .030		
DO NOT SCALE DWG	SCALE	MODEL NO. 150	DWG NO. 1101-00-0075
LOGE IDENT	23330	REV E	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



KEYBOARD ARRANGEMENT

1	8	9	G
4	5	6	A
7	3	0	B
-	2	E	H

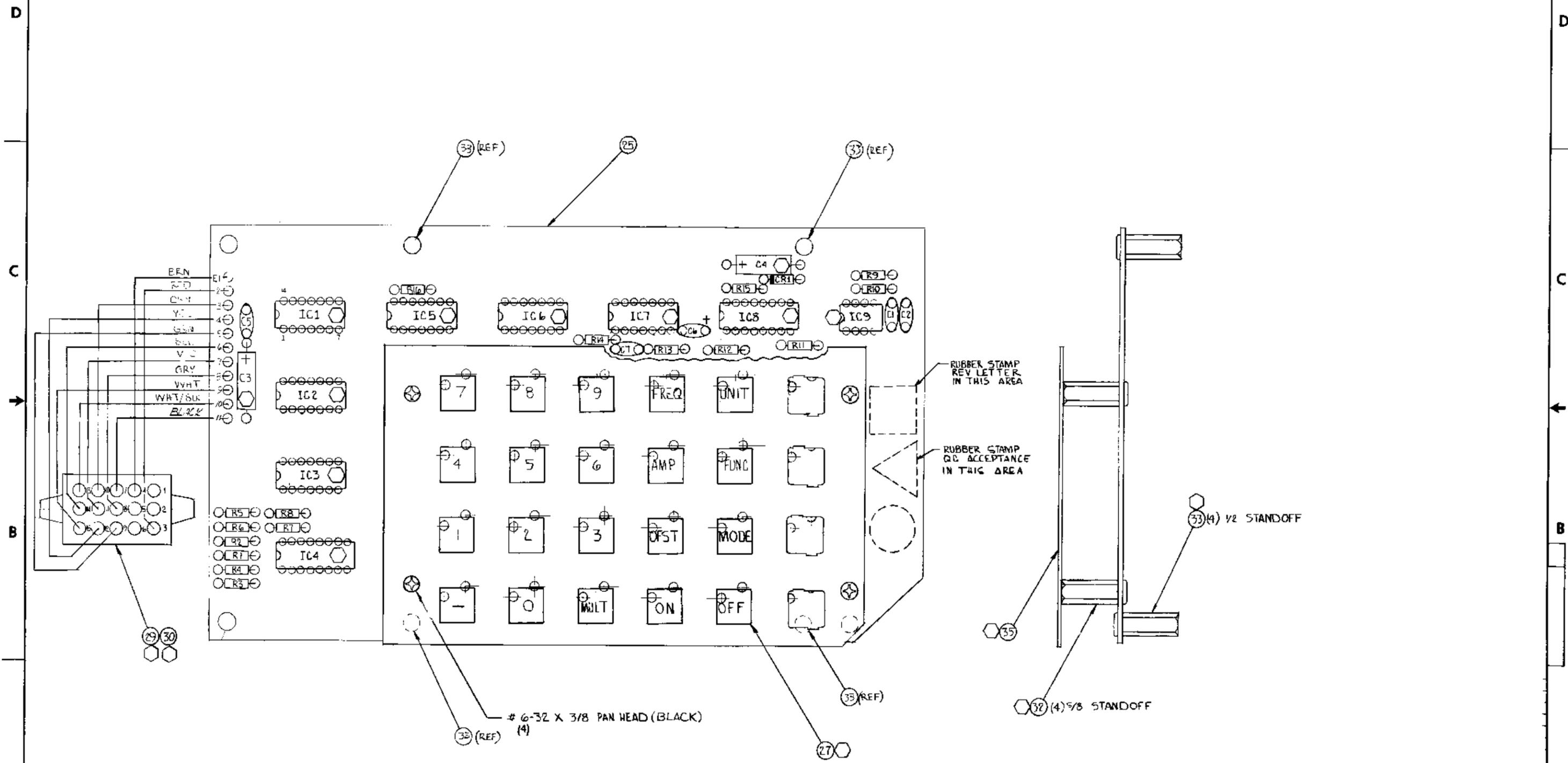
- A = AMPL
- B = MODE
- C = FUNC
- D = OFST
- E = MULT
- F = FREA
- G = UNIT
- H = ON
- I = OFF
- J = CHS

5. ○ DENOTES WIRE COLORS PER RESISTOR COLOR CODES.
 4. □ DENOTES ACTUAL LABELING.
 3. BAR OVER MNEMONIC DENOTES TRUE-WHEN-LOW.
 2. * DENOTES OPEN COLLECTOR.
 1. ALL RESISTORS ARE 1/4 W.
- NOTE: UNLESS OTHERWISE SPECIFIED.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE 1/19	
MATERIAL	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XX - .010 ANGLES 45° XX - .030	TITLE SCHEMATIC KEY BOARD A6
DO NOT SCALE DIMS	SCALE	MODEL NO. 159
		DATE 0103-00-0109
		CODE 23338
		SHEET OF 1

REV	ECN	BY	DATE	APP
A	ECN 1754	PO	6-2-78	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



1. (31) (REF) NUMBERS IN HEX AND CIRCLES INDICATE STATION LOCATION.
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. BARNETT	DATE 12/1/78	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	DESIGNED BY D. Barnett	DATE 1/7/78	TITLE PC ASSY - KEYBOARD	
FINISH WAVETER PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 0.10 ANGLES 1:1 XX ± 0.30	DO NOT SCALE DWG	MODEL NO. 159	REV A
SCALE 2/1	COM IDENT 2333B		SHEET 1 OF 1	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	OMIG-MFG#-PART-NO	MFG#	WAVETEK NO.	QTY/P1
NONE	ASSY UMRG, KEYBOARD	0101-00-0109	WVTR	0101-00-0109	1
NONE	SCHEMATIC, KEYBOARD	0103-00-0109	WVTR	0103-00-0109	1
35	CARRIER, KEY	150-344	WVTR	1400-00-0783	1
C2 C5	CAP, CEM., .01MF, 50V	CK-103	CKL	1500-01-0310	2
E1	CAP, CEM., 470PF, 1KV	DD-471	CKL	1500-04-7111	1
E7	CAP, CEM., .005MF, 50V	CK-502	CKL	1500-05-0210	1
E6	CAP, TANT, 22MF, 15V	196U226X9015K41	SPHAG	1500-72-2601	1
E5 E4	CAP, TANT, 33MF, 10V	1500336X901062	SPHAG	1500-73-3601	2
25	KEY BURHU	150-147	WVTR	1700-00-0109	1
30	PLUG, 15PIN	03-04-2151	MULEX	2100-02-0013	1
29	PIN, MALC	02-09-2118	MULEX	2100-05-0005	11
33	STANDOFF	15310-1/2-11	USECU	2800-02-0003	4
32	STANDOFF	15310-5/8	USECO	2800-02-0004	4
K11 K13 K15 K16	RES, MF, 1/8W, 1K, 2.21K	RV55D-2211F	TRW	4701-03-2211	4
K10	RES, MF, 1/8W, 1K, 301K	RV55D-3013F	TRW	4701-03-3013	1
K1 K2 K3 K4 K5 K6 K7 K8	RES, MF, 1/8W, 1K, 464	RV55D-4640F	TRW	4701-03-4640	8
K9	RES, MF, 1/8W, 1K, 49.9K	RV55D-4992F	TRW	4701-03-4992	1
WAVETEK PARTS LIST		TITLE KEY BOARD	ASSEMBLY NO. 1100-00-0109		REV A
			PAGE: 1		

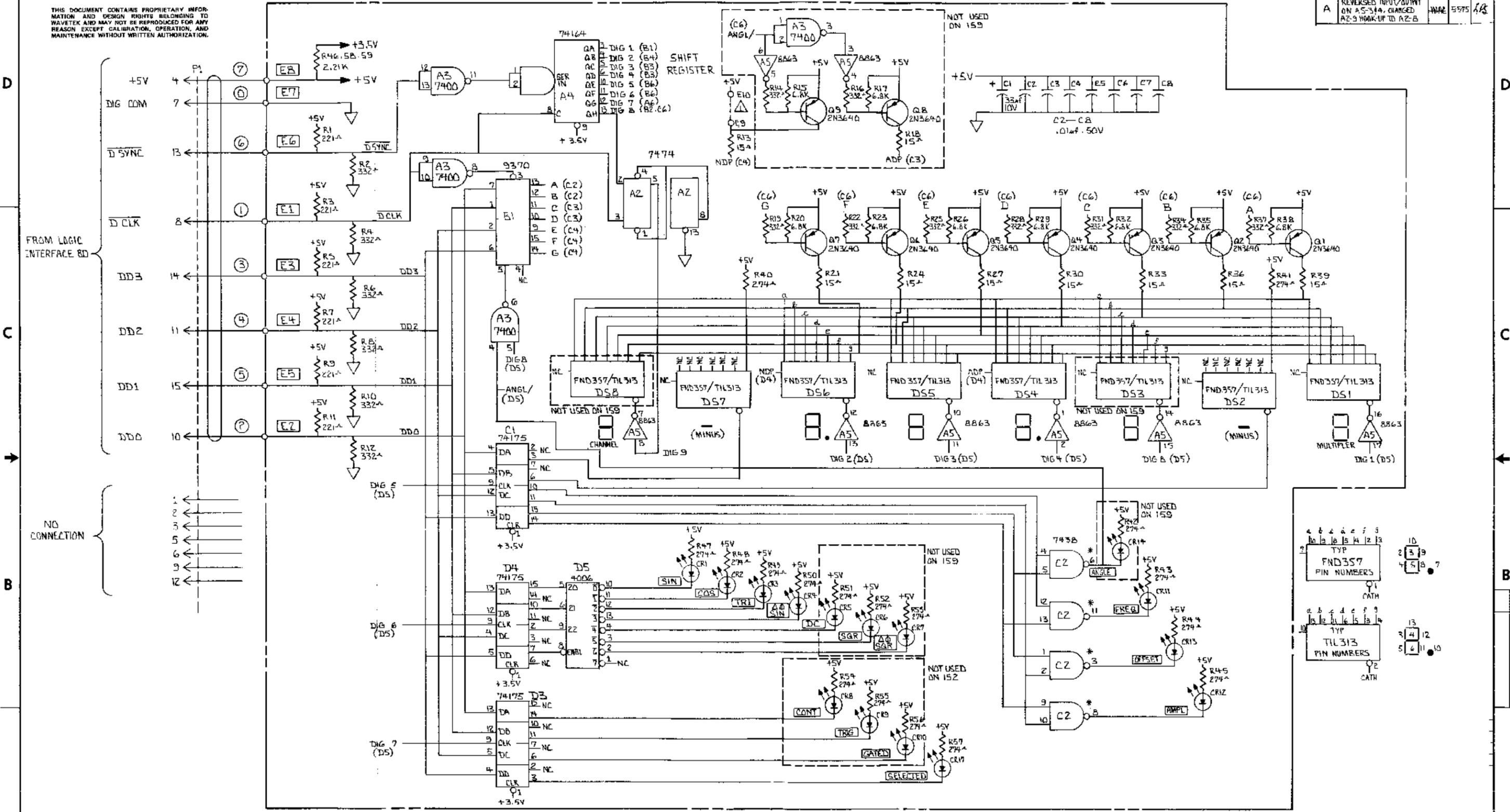
REFERENCE DESIGNATORS	PART DESCRIPTION	OMIG-MFG#-PART-NO	MFG#	WAVETEK NO.	QTY/P1
K12 K14	RES, MF, 1/8W, 1K, 6.25K	RV55D-6251F	TRW	4701-03-6251	2
C21	DIODE	FD-6666	FAIR	4807-02-6666	1
27	KEY & SWITCH ASSY	150-531	WVTR	4100-00-0301	1
IC9	IC	NE555V	816	7000-00-5500	1
IC5	IC	7403	TI	8000-74-0300	1
IC1 IC2 IC3	IC	7438	TI	8000-74-3800	3
IC6	IC	74107	TI	8007-41-0700	1
IC7	IC	74132	TI	8007-41-3200	1
IC4	IC	74151	TI	8007-41-5100	1
IC8	IC	74161	TI	8007-41-6100	1
WAVETEK PARTS LIST		TITLE KEY BOARD	ASSEMBLY NO. 1100-00-0109		REV A
			PAGE: 2		

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJ ENG		
FINISH WAVETEK PROCESS	RELEASE APPROV	TITLE	KEYBOARD
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 XX ±.000	SCALE	
DO NOT SCALE DIMS	SCALE	159	1100-00-0109
	SCALE		A
	DATE IDENT	23338	SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

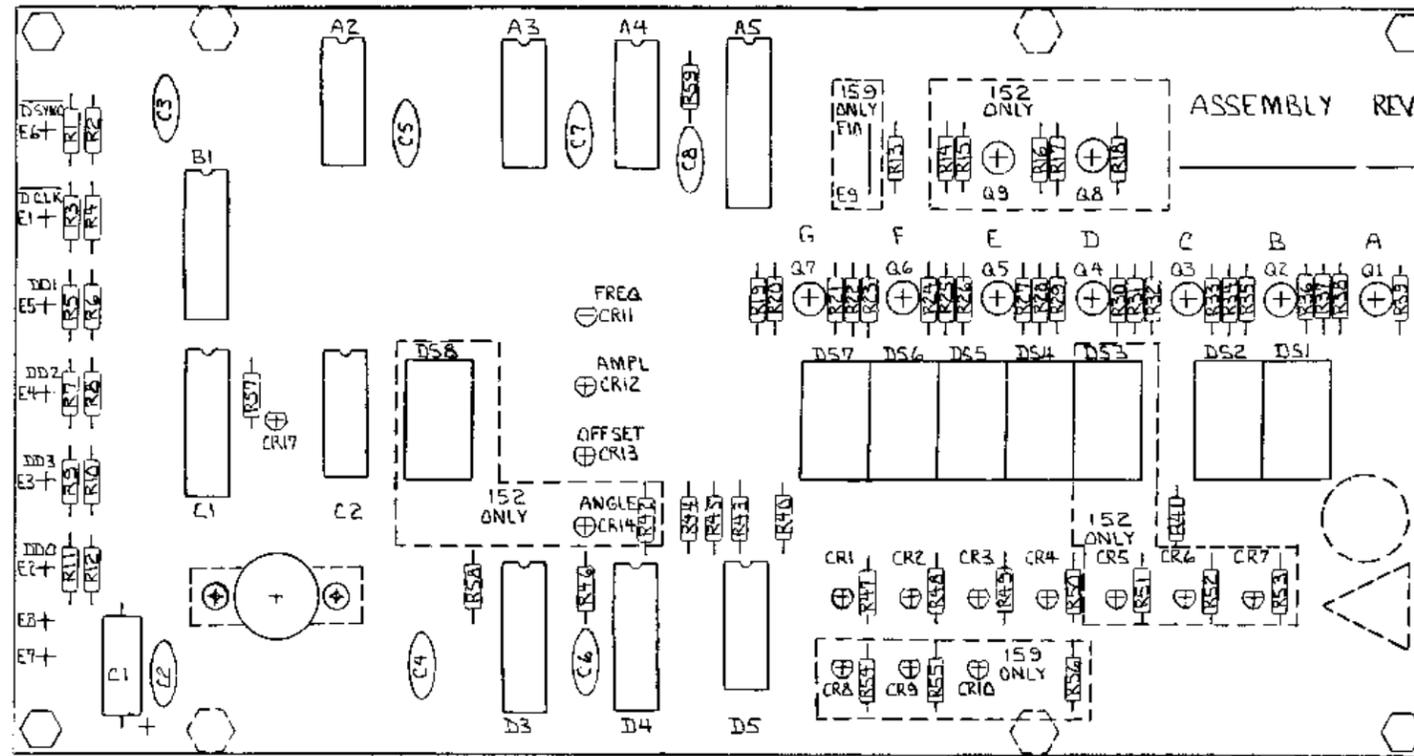
A	REVERSED INPUT/OUTPUT ON A5-314, CHANGED A2-5 HOOK-UP TO A2-8	MAE	5-75	1/8
---	---	-----	------	-----



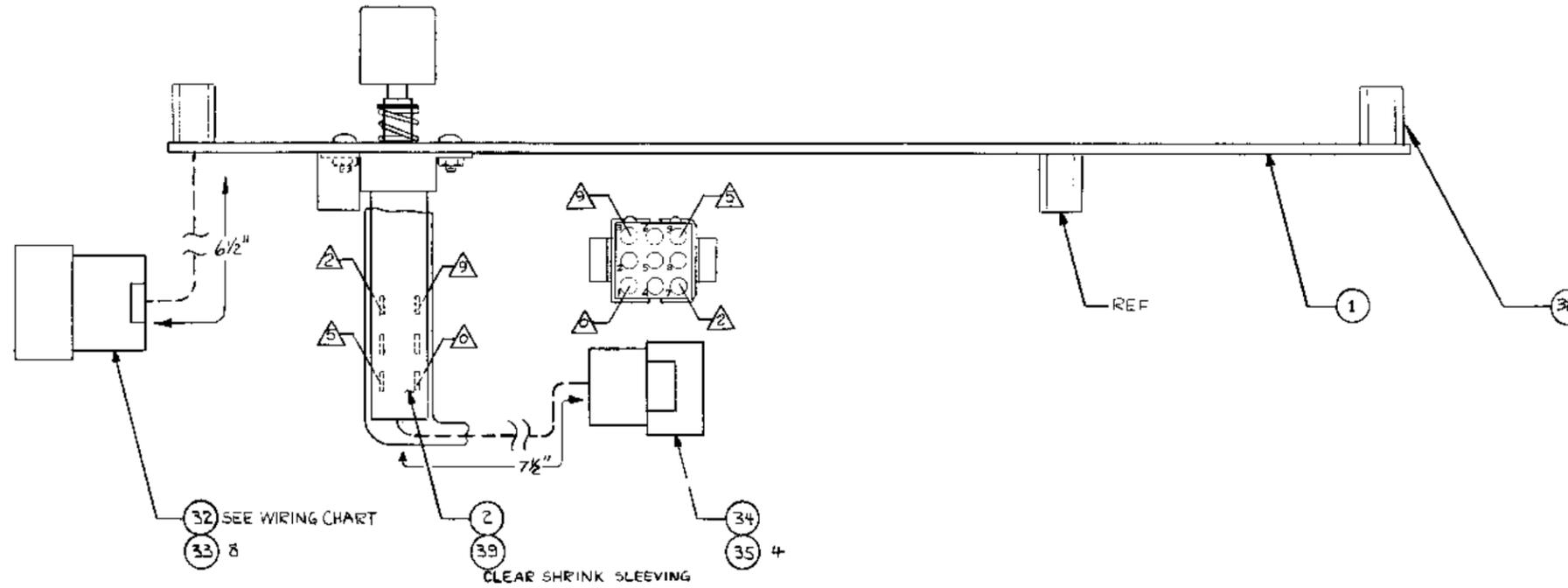
- 4. ○ DENOTES WIRE COLOR PER COLOR CODE.
 - 3. □ DENOTES LABELING ON BOARD OR DISPLAY PANEL.
 - 2. ALL RESISTORS ARE ±1% 1/8W.
 - 1. ADD JUMPER WHEN LOADING FOR MODEL 159.
- NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES		DATE: 4-2-75	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	DESIGNED BY: MAE	DATE: 4-2-75	TITLE: SCHEMATIC-DISPLAY BOARD	
FINISH: WAVETEK PROCESS	RELEASED BY: [Signature]	APPROVED BY: [Signature]	TOLERANCE UNLESS OTHERWISE SPECIFIED: XX .030 ANGLES: 1°	
DO NOT SCALE DWG		MODEL NO: 152/159	DWG NO: 0103-00-0105	REV: A
SCALE	CODE: 23338	SHEET 1 OF 1		

WIRING CHART		
BOARD LOCATION	COLORED WIRE COLOR	CONNECTOR PIN NUMBER
E1	1	8
E2	2	10
E3	3	14
E4	4	11
E5	5	15
E6	6	13
E7	0	7
E8	7	4



158-152 DISPLAY BOARD SILKSCREEN MASTER



NOTES: 1. Δ DENOTES WIRE COLOR PER COLOR CODE.

DATE		A		ECN 1314		20		6/28/75		BA	
DRAWN		JMAC		DATE		5-8-75		WAVETEK			
CHECKED		AP		DATE		7/2/75		TITLE			
RELEASE		JPA		DATE		8/28		SILKSCREEN ASSEMBLY DWG - DISPLAY BOARD			
SCALE		2/1		MODEL NO.		DWG NO.		REV			
						0101-00-0105		A			
CODE		23338		SHEET		1		OF		1	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGH	WAVETEK NO.	QTY/PKT
NONE	ASSY DRWG, DISPLAY	0101-00-0105	AVTK	0101-00-0105	1
NONE	SCHEMATIC, DISPLAY	0103-00-0105	AVTK	0103-00-0105	1
C2 C3 C4 C5 C6 C7 C8	CAP,CEM.,.01MF,.50V	CR-103 LONG LEAD	CHL	1500-01-0300	7
C1	CAP,TANT,.33MF,10V	1500330X901002	SPWAG	1500-73-3601	1
1	DISPLAY	156-151	AVTK	1700-00-0105	1
34	PLUG,PP1W	03-06-2091	MULEX	2100-02-0011	1
32	PLUG,15PIN	03-09-2151	MULEX	2100-02-0013	1
35	PIN,MALE	02-06-2103	MULEX	2100-05-0003	4
33	PIN,MALE	02-09-2116	MULEX	2100-05-0005	8
38	STANDOFF	6910-6-2C	LYNTR	2800-03-0002	4
R13 R21 R24 R27 R30 R33 R36 R39	RES,RF,1/8W,1%,15	RN55D-15H0F	TRW	4701-03-1504	4
R1 R11 R3 R5 R7 R9	RES,RF,1/8W,1%,221	RN55U-2210F	TRW	4701-03-2210	4
R40 R50 R53	RES,RF,1/8W,1%,2.21K	RN55U-2211F	TRW	4701-03-2211	3
R40 R41 R43 R44 R45 R47 R48 R49 R50 R54 R53 R56 R57	RES,RF,1/8W,1%,274	RN55U-2740F	TRW	4701-03-2740	13
R10 R12 R19 R2 R22 R25 R26 R31 R34 R37 R4 R6 R8	RES,RF,1/8W,1%,332	RN55D-3320F	TRW	4701-03-3320	13
WAVETEK PARTS LIST		TITLE DISPLAY	ASSEMBLY NO. 1100-00-0105 PAGE: 1		REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGH	WAVETEK NO.	QTY/PKT
R20 R23 R26 R29 R32 R35 R38	RES,RF,1/8W,1%,6.81K	RN55D-6811F	TRW	4701-03-6811	7
CH1 CH10 CH11 CH12 CH13 CH17 CH2 CR3 C4 C8 CH7	LED	41L-209A	LI	4899-01-0005	11
DS1 DS2 DS4 DS5 DS6 DS7	LED	5062-7740-C	PP	4899-00-0009	6
Q1 Q2 Q3 Q4 Q5 Q6 Q7	TRANS	2N5640	FAIR	4901-05-6400	7
2	SWITCH ASSY Pd	157-422	AVTK	5103-00-0011	1
39	BUTTON	6315 BLACK	CHL	5103-04-0001	1
IC05	IC	4006	MUT	8000-40-0600	1
IC43	IC	7400	TI	8000-74-0000	1
IC02	IC	7438	TI	8000-74-3800	1
IC42	IC	7474	TI	8000-74-7400	1
IC45	IC	DS8863	NSC	8000-68-6300	1
IC01	IC	9370DC	FAIR	8000-93-7000	1
IC44	IC	74164	TI	8007-41-6400	1
IC01 IC03 IC04	IC	74175	TI	8007-41-7500	5
WAVETEK PARTS LIST		TITLE DISPLAY	ASSEMBLY NO. 1100-00-0105 PAGE: 2		REV d

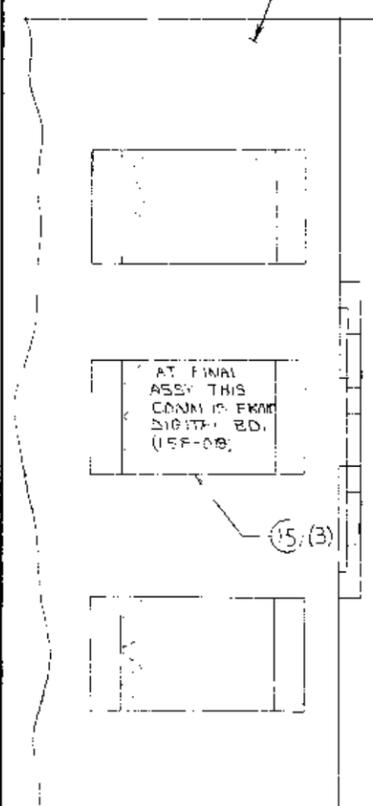
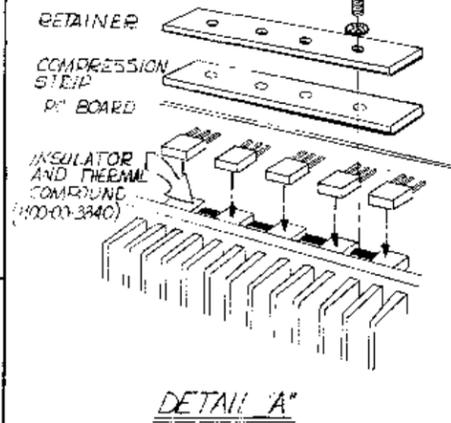
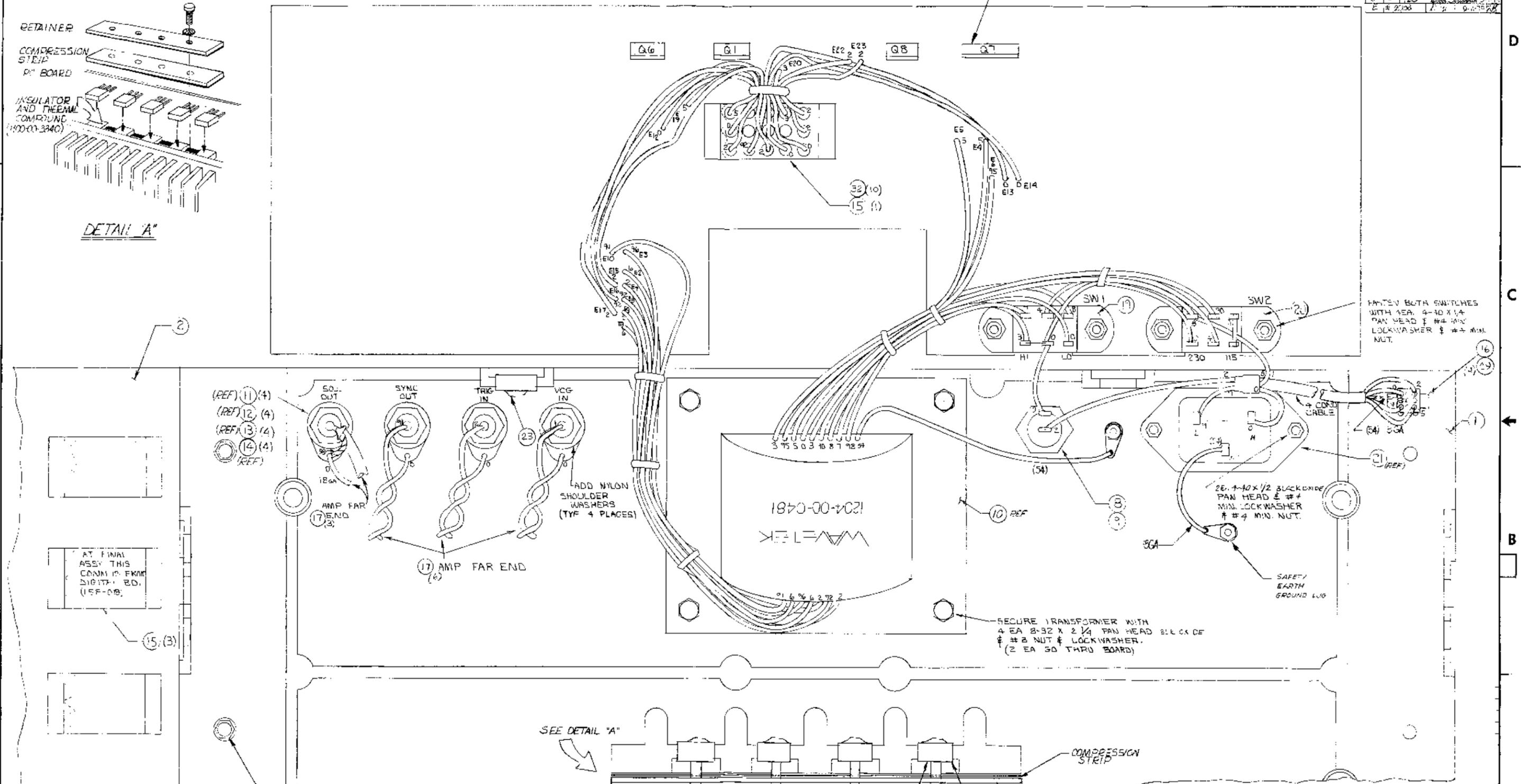
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJENGR	
FINISH WAVETEK PROCESS	RELEASE APPROV	TITLE DISPLAY
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES 1:1 XX ±.030	MODEL NO. 158/159
SCALE	DATE	ORD NO. 1100-00-0105
		REV B
	23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	ECN 1368	Ro	11/25/78	
B	ECN 1525	EO	3/1/77	
C	ECN 1754	Ro	6/1/77	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

SEE POWER SUPPLY (1100-00-0108) FOR INSTALLATION OF Q1, Q6, Q7 & Q8 (LEADS MUST BE FULL LENGTH)

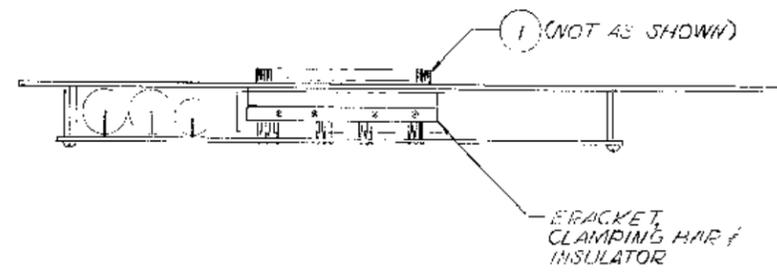
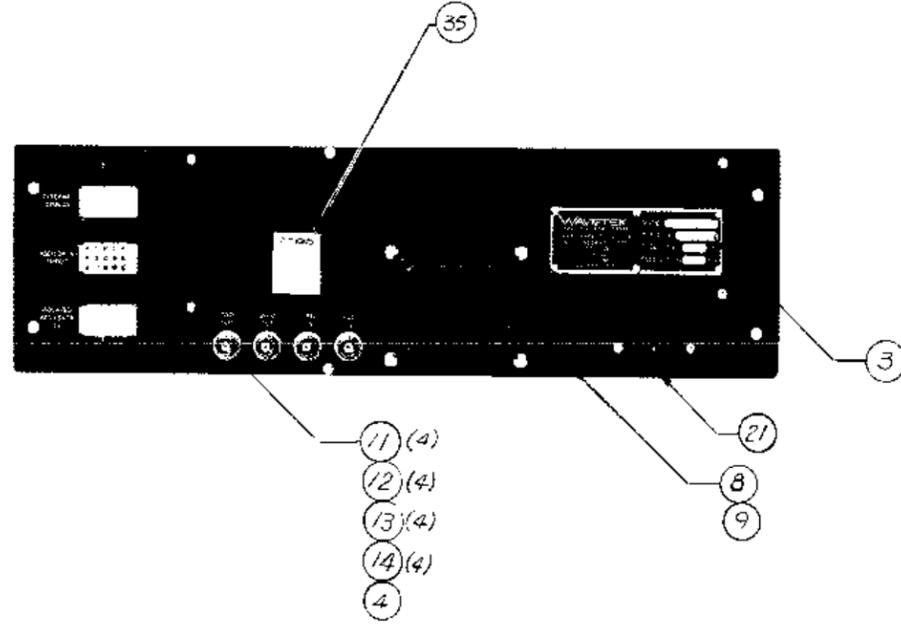
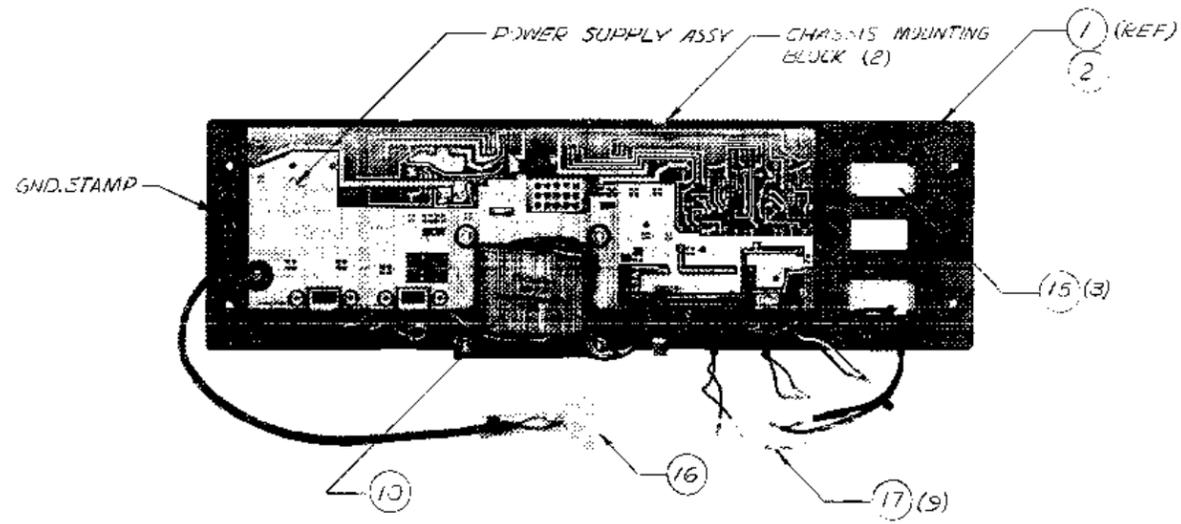


2 SLEEVE AS REQUIRED TYP
 NUMBERS INDICATE WIRE COLORS
 NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: REXINS	DATE: 3-21-78	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL:	PROBENGR	TITLE: ASSEMBLY POWER SUPPLY (REAR CASTING)	
FINISH: WAVETEK PROCESS	RELEASE APPROV:	TOLERANCE UNLESS OTHERWISE SPECIFIED: ANGLES -1 XX: 0.03	MODEL NO: 158/159
		DO NOT SCALE DWG	UNG NO: 0102-00-0332
		SCALE:	REV: E
			FORM IDENT: 23338 SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	DATE	BY	CHKD
A	DDC *1463	DC	PAW
SEE SHEET 1			



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN <i>Cl. Cox</i>	DATE <i>8/8/80</i>	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	PROJ. NO. <i>1000000</i>	DESIGNER <i>Y. H. Yip</i>	TITLE ASSEMBLY REAR PANEL	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - .010 ANGLES - 1 XX - .030	DO NOT SCALE DWG	MODEL NO. 158/159	ORIG. NO. 0102-00-0332
SCALE NONE	CODE 23338	REV. E	SHEET 2 OF 2	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP
-----	-----	----	------	-----

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. REAR PNL	0102-00-0332	WVTK	0102-00-0332	1
10	TRANSFORMER	158-500	WVTK	1204-00-0481	1
2	EXTENDER	158-022	WVTK	1400-00-0710	1
1	CAST, REAR FROM: 1400-00-3471	158-325	WVTA	1400-00-0759	1
30	INSULATOR	147-267	WVTK	1400-00-3700	1
22	BAR, CLAMP	147-379	WVTK	1400-00-0733	1
4	DECAL, BNC	162-209	WVTK	1400-00-3810	1
NONE	STRIP, COMP REF. 0200-08-0001	162-312	WVTK	1400-00-3840	1
NONE	LABEL, OPTION	1400-00-8880	WVTK	1400-00-8880	1
3	F.D. LABEL	1400-00-9110	WVTK	1400-00-9110	1
11	BNC CONN	KC-7946	KING	2100-01-0002	4
16	CONN, 9PIN	03-06-1091	MOLEX	2100-02-0010	1
15	CONN, 15PIN	03-09-1151	MOLEX	2100-02-0012	3
21	RECEP., POWER	EAC-301	SWCFT	2100-03-0008	1
14	SOLDER LUG	1497	SMITH	2100-04-0017	4
NONE	SOLDER LUG	1485-6	SMITH	2100-04-0025	2
29	PIN, FEMALE	02-06-1103	MOLEX	2100-05-0002	5

WAVETEK
PARTS LIST

TITLE
REAR PANEL ASSY

ASSEMBLY NO.
1101-00-0074

REV
G

PAGE: 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
17	CONN	60598-B	AMP	2100-05-0017	9
32	PIN, FEMALE	02-09-1118	MOLEX	2100-05-0026	10
8	FUSE, 3/4A, 250V, S-B	313-750	LITFU	2400-05-0011	1
9	FUSE HOLD	031.1682/021.1666	SCHUR	2400-05-0012	1
23	BREEDNUT, TYPE"U"	018050-632-4	TINN	2600-07-0002	6
12	WASHER, SHOULDER	266B	SMITH	2800-27-0004	4
13	NYLON FLAT WASHER	2264-N-385	AMTOM	2800-28-0005	4
19	SW ASSY SLIDE HI-LO	5W422-PT-HK	UTD	5105-00-0001	1
20	SWITCH ASSY SLIDE	4625A-LF	SWCFT	5105-00-3002	1
31	SOLDER GUARD	46256-LF-B0	SWCFT	5105-09-0001	2

WAVETEK
PARTS LIST

TITLE
REAR PANEL ASSY

ASSEMBLY NO.
1101-00-0074

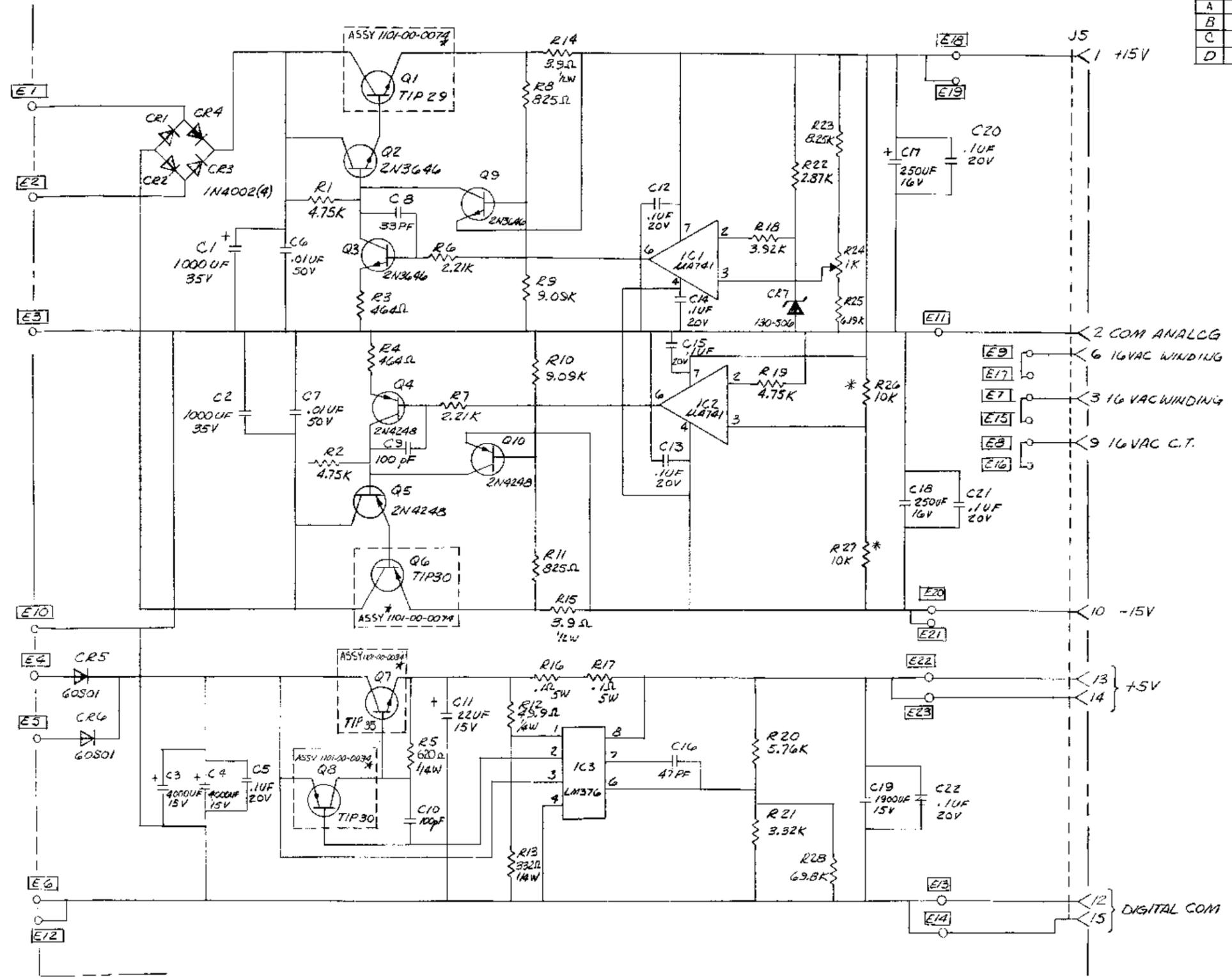
REV
G

PAGE: 2

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	DATE	
FINISH WAVETEK PROCESS	RELEASE APPROV		PARTS LIST REAR PANEL ASSY
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES: Y 3X ± .005			MODEL NO. 159
DO NOT SCALE DWG			
SCALE			REV G
CODE 23338			SHEET 1 OF 1

NOTE: UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



A	1069	EL	8/20/78
B	ECV 1754	RB	6/20/78
C	# 1920	Branch	2-24-79
D	3072	Am	3/5/79

3. * ATTACHED TO REAR PANEL HEATSINK BRACKET.
 2. * INDICATES MATCHED SET.
 1. ALL RESISTORS ARE 1/8W 1%.

NOTE: UNLESS OTHERWISE SPECIFIED

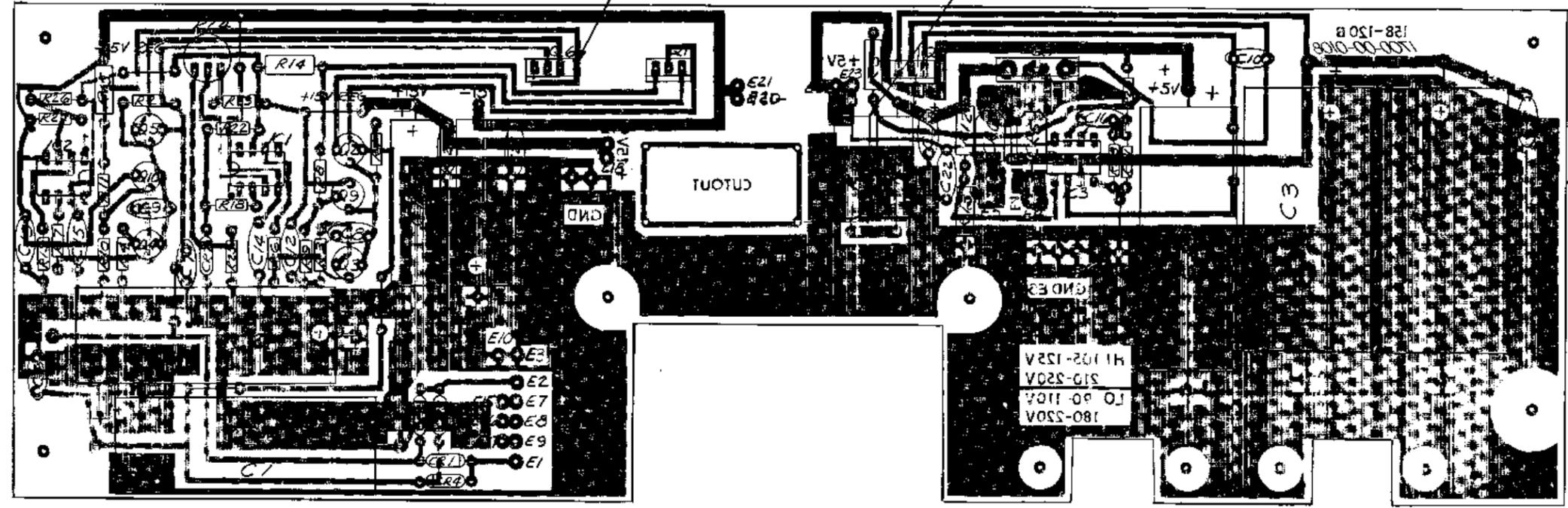
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CLC	DATE 8/25/78	WAVETEK SAN DIEGO • CALIFORNIA TITLE SCHEMATIC POWER SUPPLY A1
MATERIAL	APPROVED [Signature]	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES 1° .XX ±.020 DO NOT SCALE DWG		PART NO. 158/159 DWG NO. 0103-00-0108 REV. D
SCALE NONE	FORM IDENT 23338		SHEET 1 OF 1

REV	ECN	BY	DATE	APP
0	1069	180	01/20/82	
D	ECN 1303	RO	06-11-83	
E	ECN 1754	RO	06-20-83	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

INSTALL TRANSISTORS AFTER WAVESOLDER - DO NOT BEND LEADS. (TYP 4 PLACES) SEE DRWG 0102-00-0332 FOR FURTHER INFORMATION.

DO NOT STAND PARTS OFF BOARD



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRWEN: CC Cox	DATE: 4/15/82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	DESIGNED BY: R. Barandy	DATE: 4/15/82	
FINISH WAVETEK PROCESS	RELEASE APPROV:	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010 ANGLE ± .1° XX ± .030 DO NOT SCALE DWG SCALE: 2:1	TITLE: PC BOARD ASSY POWER SUPPLY BD
	MODEL NO: 158/159	DRG NO: 0101-00-0108	REV: E
	CODE: 23338	SHEET: 1	OF: 1

NOTE: UNLESS OTHERWISE SPECIFIED

BRUNING 40-520 15821

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. POWER	0101-00-0108	WVTK	0101-00-0108	1
NONE	SCHEMATIC. POWER	0103-00-0108	WVTK	0103-00-0108	1
C8 C9	CAP. CER. 100PF. 1KV	DD-101 LONG LEAD	CRL	1500-01-0101	2
C6 C7	CAP. CER. MIN. .01MF. 50V	CACDQZSU103Z100A	CDRNG	1500-01-0310	2
C12 C13 C14 C15 C20 C21 C22 C5	CAP. CER. MON. .1MF. 50V	CACDQZU104Z050A	CDRNG	1500-01-0405	8
C10	CAP. CER. 33PF. 1KV	DD-330	CRL	1500-03-3011	1
C16	CAP. CER. 47PF. 1KV	DD-470	ARCO	1500-04-7011	1
C1 C2	CAP. ELECT. 1000MF. 35V	39D10800350L6	SPRAG	1500-31-0212	2
C19	CAP. ELECT. 1900MF. 15V	39D19800150L4	SPRAG	1500-31-9201	1
C17 C18	CAP. ELECT. 250MF. 16V	50002576016DF7	SPRAG	1500-32-5101	2
C3 C4	CAP. ELECT. 4000MF. 15V	39D4080015JL4	SPRAG	1500-34-0201	2
C11	CAP. TANT. 22MF. 15V	1960226K9J15KA1	SPRAG	1500-72-2601	1
1	POWER	158-120	WVTK	1700-00-0108	1
R24	POT. TRIM. 1K	91AR1K	BECK	4400-01-0209	1
R14 R15	RES. C. 1/2W. 5%. 3.9	RC206F-3R9	STKPL	4700-25-0399	2
R5	RES. C. 1/2W. 5%. 620	RC206F-621	STKPL	4700-25-6200	1
R6 R7	RES. MF. 1/8W. 1%. 2.21K	RN55D-2211F	TRW	4701-03-2211	2

WAVETEK
PARTS LIST

TITLE
POWER

ASSEMBLY NO.
1100-00-0108
PAGE: 1

REV
C

REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
R22	RES. MF. 1/8W. 1%. 2.87K	RN55D-2871F	TRW	4701-03-2871	1
R21	RES. MF. 1/8W. 1%. 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R18	RES. MF. 1/8W. 1%. 3.92K	RN55D-3921F	TRW	4701-03-3921	1
R3 R4	RES. MF. 1/8W. 1%. 464	RN55D-4640F	TRW	4701-03-4640	2
R1 R19 R2	RES. MF. 1/8W. 1%. 4.75K	RN55D-4751F	TRW	4701-03-4751	3
R20	RES. MF. 1/8W. 1%. 5.76K	RN55D-5761F	TRW	4701-03-5761	1
R25	RES. MF. 1/8W. 1%. 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R26	RES. MF. 1/8W. 1%. 69.8K	RN55D-6982F	TRW	4701-03-6982	1
R11 R8	RES. MF. 1/8W. 1%. 825	RN55D-8250F	TRW	4701-03-8250	2
R23	RES. MF. 1/8W. 1%. 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R10 R9	RES. MF. 1/8W. 1%. 9.09K	RN55D-9091F	TRW	4701-03-9091	2
R13	RES. MF. 1/4W. 1%. 332	RN60D-3320F	TRW	4701-13-3320	1
R12	RES. MF. 1/4W. 1%. 49.9	RN60D-4992F	TRW	4701-13-4992	1
R16 R17	RES. MW. 5W. 10%. .1	CP-5	DALE	4702-66-0019	2
R26 R27	RES. SET. 2-10K. 1/8W QTY: 2: 4701-03-1002	142-501-64A	WVTK	4789-00-0019	1
CR7	DIODE	1N4581	MICRU	4801-01-4581	1
CR1 CR2 CR3 CR4	DIODE	SCE-1	SEHT	4801-02-0001	4

WAVETEK
PARTS LIST

TITLE
POWER

ASSEMBLY NO.
1100-00-0108
PAGE: 2

REV
G

REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
CR5 CR6	DIODE	6061	IR	4806-02-0060	2
Q2 Q3 Q9	TRANS	2N3646	NSC	4901-03-6460	3
Q10 Q4 Q5	TRANS	2N4248	FAIR	4901-04-2480	3
Q1	TRANS	TIP-29	TI	4902-00-0290	1
Q6 Q8	TRANS	TIP-30	TI	4902-00-0300	2
Q7	TRANS	TIP-35	TI	4902-00-0350	1
IC3	IC	LM376	NSC	7000-03-7600	1
IC1 IC2	IC	MA-741	FAIR	7000-07-4100	2

WAVETEK
PARTS LIST

TITLE
POWER

ASSEMBLY NO.
1100-00-0108
PAGE: 3

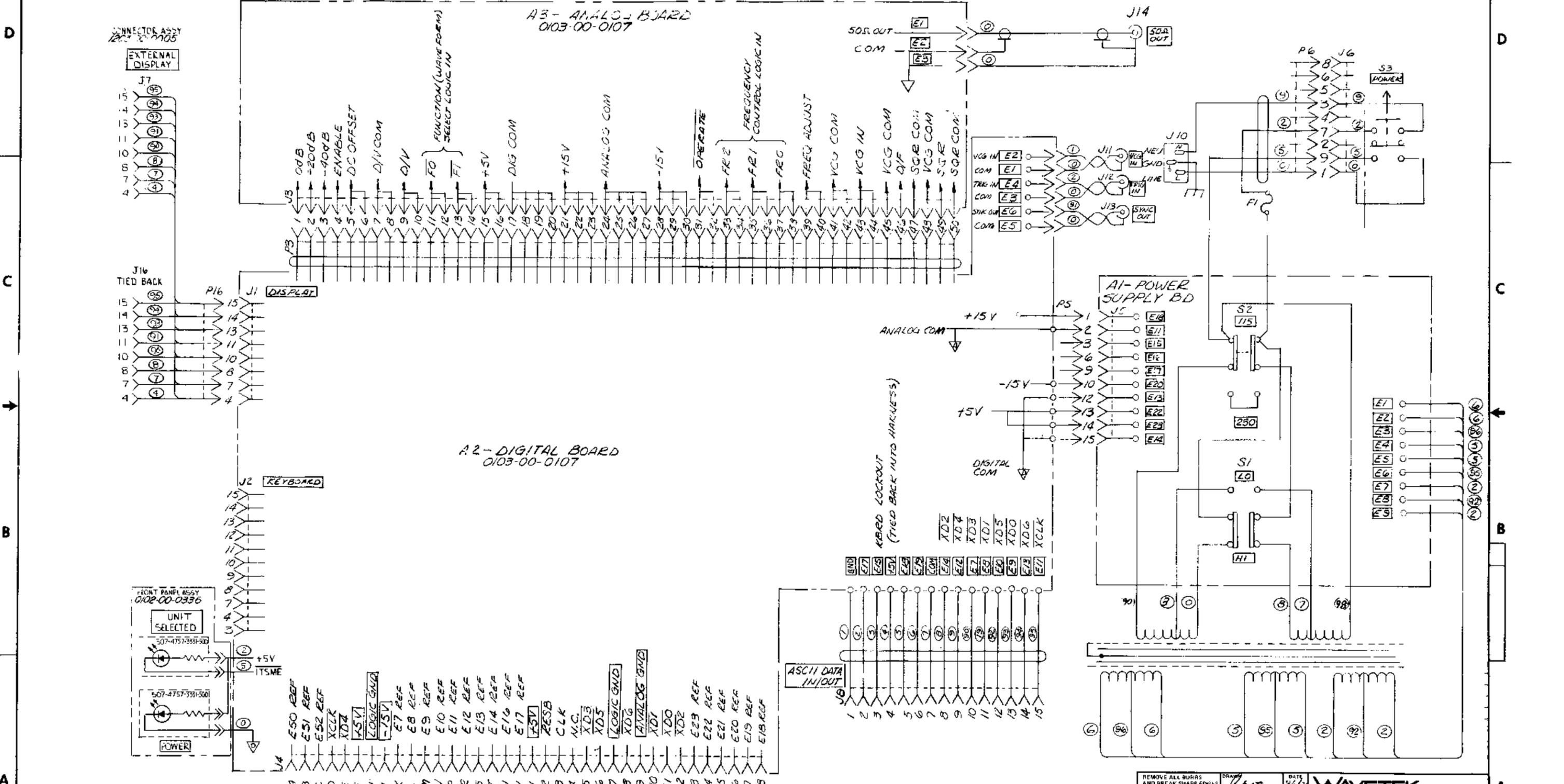
REV
G

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	 WAVETEK SAN DIEGO • CALIFORNIA TITLE PARTS LIST POWER SUPPLY
MATERIAL	PROF ENGR	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES .1° XX ±.030		
SCALE	DO NOT SCALE DWG	MODEL NO	
SCALE	SCALE	DWG NO.	REV.
CODE	23338	159	1100-00-0108 G
SHEET	23338	SHEET	1 OF 1

NOTE: UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

A	ECW	3/28	Ro	11/17
---	-----	------	----	-------

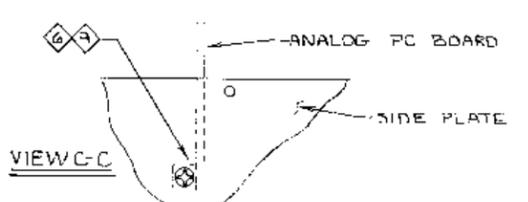
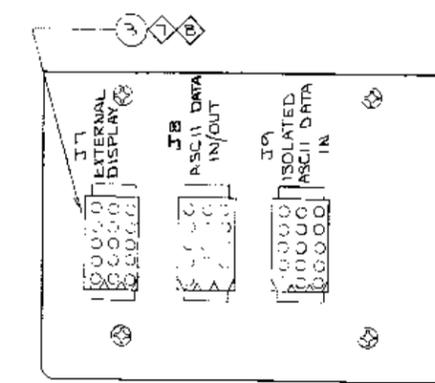
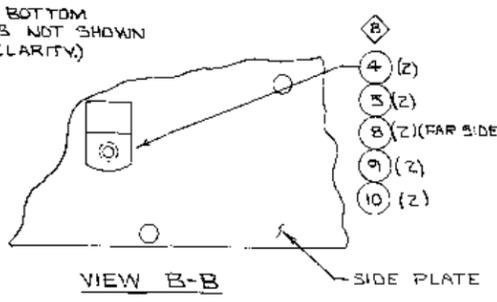
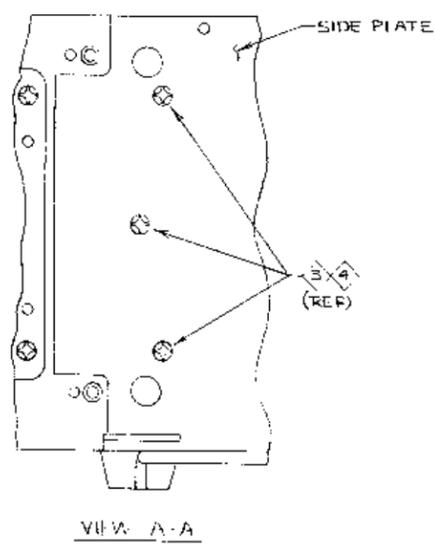
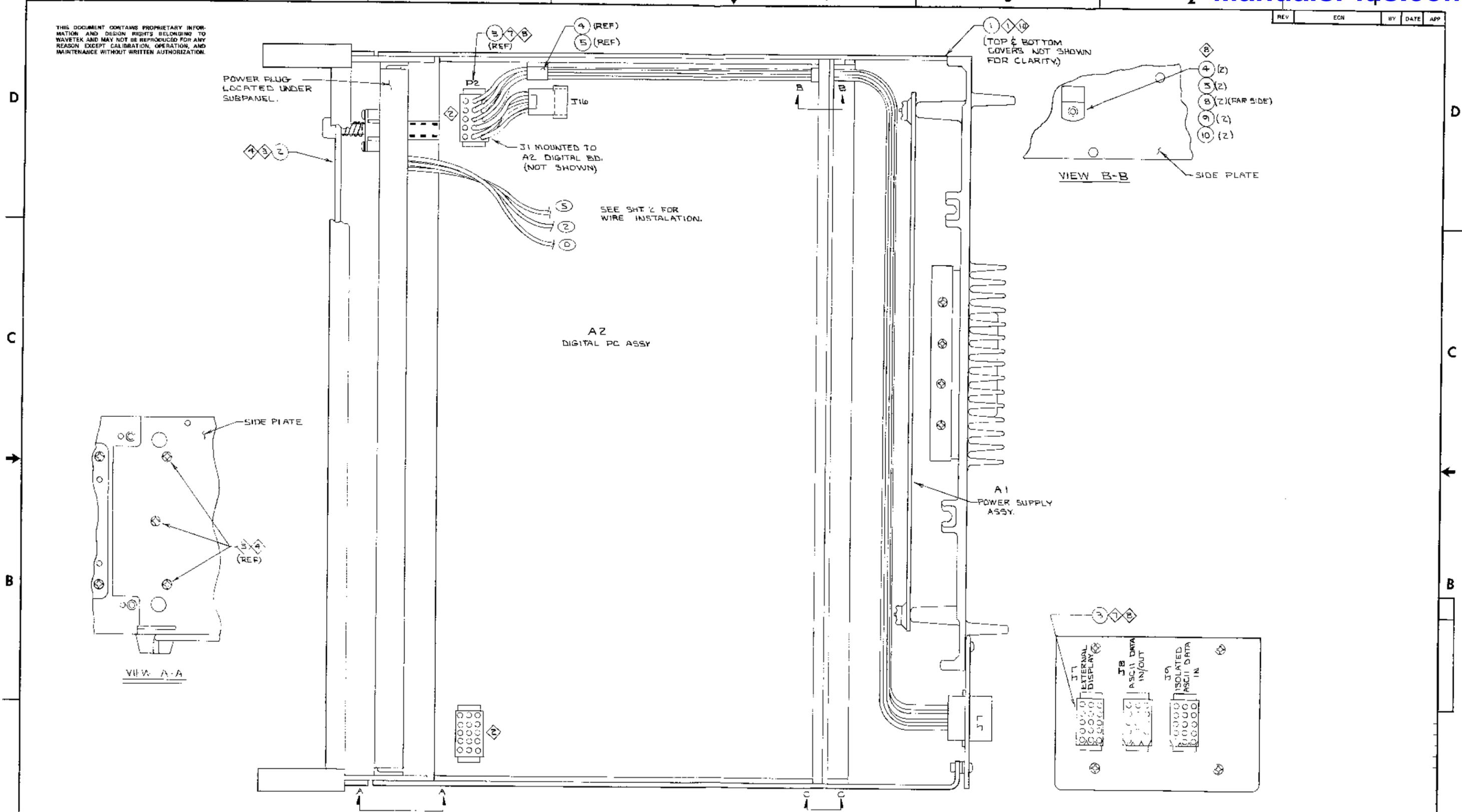


- NOTES:
- 3. ○ DENOTES WIRE COLOR PER RESISTOR CODE
 - 2. BAR OVER MNEMONIC DENOTES TRUE WHEN LOW
 - 1. □ DENOTES ACTUAL LABELING ON UNIT

REMOVE ALL BURRS AND BREAK SHARP EDGES		DATE: 11/14	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	DRIVER: [Signature]	DATE: 11/14	TITLE: INTERCONNECT DIAGRAM	
FINISH: WAVETEK PROCESS	RELEASE APPROV: [Signature]	SCALE: DO NOT SCALE DWG	MODEL NO: 158/159	
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX - 010 ANGLES - 1:1 XX - 030		DWG NO: 0004000081	
			REV: A	
			CODE IDENT: 23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

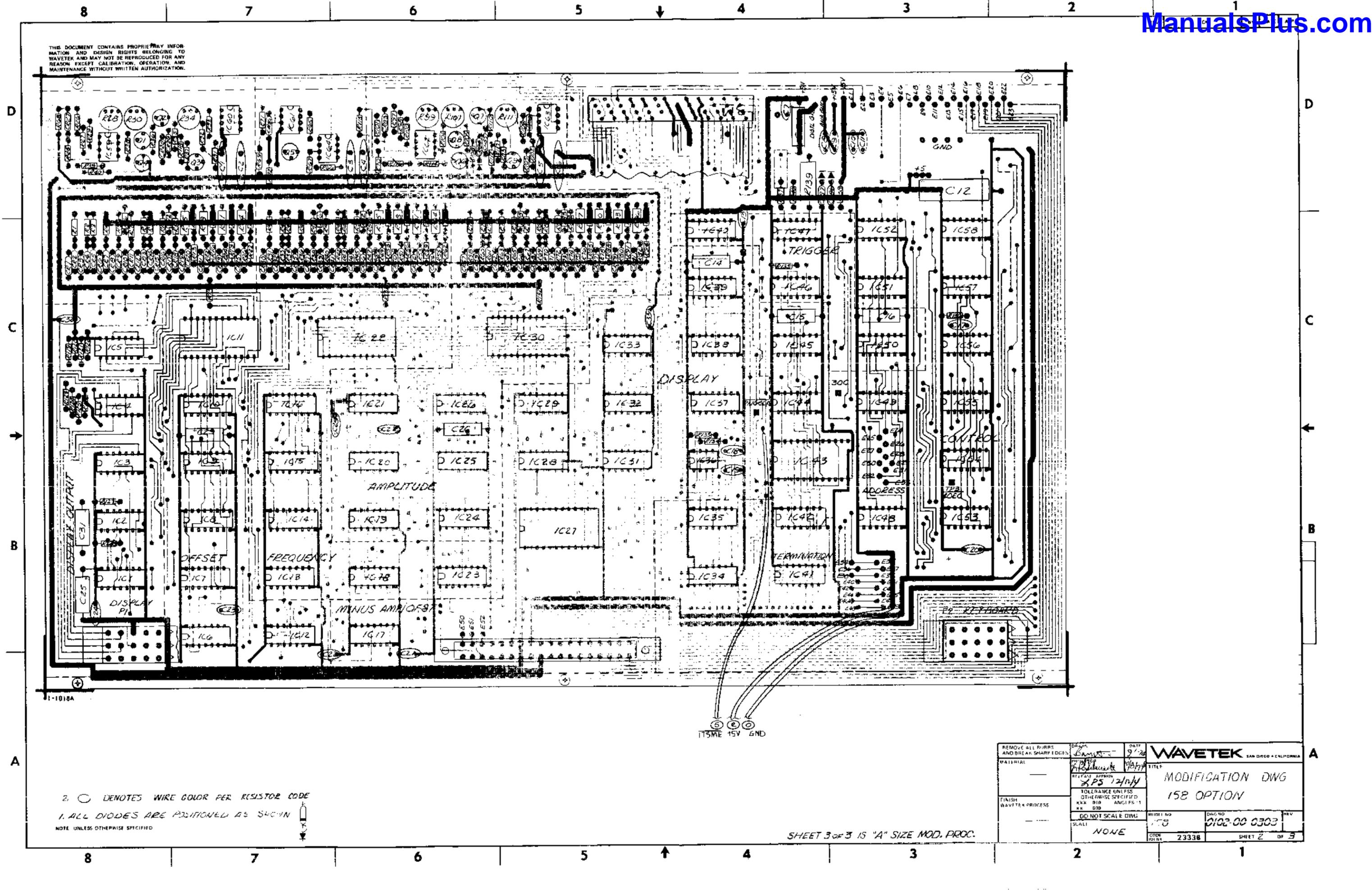


- ▲ FULL HARDWARE FOR FIELD INSTALLATION ONLY.
- 2. ◊ DENOTES LINE NUMBER FOR MODIFICATION PROCEDURE.
- DENOTES WIRE COLOR PER RESISTOR CODE.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN ADKINS	DATE 10-27-74	WAVETEK OAK BROOK, CALIFORNIA
MATERIAL	DESIGNED BY	10/27/74	
FINISH WAVETEK PROCESS	RELEASE APPROV. JPS 10/1/74	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.020 X ±.050	TITLE MODIFICATION DWG 158 OPTION
SCALE	DO NOT SCALE DWG	MODEL NO. 158	DWG NO. 010200-0303
		CURT IDENT 23338	SHEET 1 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON, EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



1-1018A

ITSME 15V GND

2. \bigcirc DENOTES WIRE COLOR PER RESISTOR CODE
1. ALL DIODES ARE POSITIONED AS SHOWN
NOTE: UNLESS OTHERWISE SPECIFIED

SHEET 3 OF 3 IS "A" SIZE MOD. PROC.

REMOVE ALL BURRS AND BREAK SHARP EDGES.		DATE: 9/26		WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL:		DRAWN: [Signature]		TITLE: MODIFICATION DWG	
FINISH: WAVETEK PROCESS		CHECKED: [Signature]		158 OPTION	
DO NOT SCALE DWG		MATERIAL NO: 158		DWG NO: 0102-00 0303	
SCALE: NONE		CAGE CODE: 23338		SHEET 2 OF 3	

MODIFICATION PROCEDURE

1. REMOVE TOP AND BOTTOM COVERS.
2. DISCONNECT POWER PLUG P6, DISPLAY PLUG P1 AND KEYBOARD PLUG P2.
3. REMOVE FRONT PANEL ASSY1100-00-0075 AND RETURN TO STOCK.
4. INSTALL FRONT PANEL ASSY1101-00-0078 AS SHOWN.
5. CONNECT POWER PLUG P6, TO NEW FRONT PANEL ASSY.
6. REMOVE SCREWS AND RAISE ANALOG BOARD TO FACILITATE INSTALLATION OF WIRES TO DIGITAL BOARD.
7. REMOVE BLANK MOLEX CONNECTOR FROM THE EXTERNAL DISPLAY LOCATION ON REAR PANEL AND RETURN TO STOCK.
8. INSTALL CONNECTOR ASSY1203-00-0005. CONNECT P16 TO J1 ON THE A2 DIGITAL PC ASSY. INSTALL MOLEX TO EXTERNAL DISPLAY LOCATED ON THE REAR EXTENDER AS SHOWN.
9. LOWER ANALOG PC ASSY AND INSTALL SCREWS.
10. INSTALL TOP AND BOTTOM COVERS.

SH 3 of 3

DWG NO. 0102-00-0303	REV
-------------------------	-----

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATIONS	PART DESCRIPTION	DWG-MFGN-PART-NO	MFGM	WAVETEK NO.	QTY/PKT
NONE	ASSY DRWG, 158 MOD	0102-00-0303	AVIK	0102-00-0303	1
3	CABLE ASSY	158-039	AVIA	1205-00-0005	1
NOVE	CABLE CLAMP	035	SMITH	2800-00-0010	2
NONE	RETAINING SPRING	U-191	HEKSH	2800-09-0007	2

	TITLE MODIFICATION KIT	ASSEMBLY NO. 1101-00-0044	REV A
	PAGE: 1		<input type="checkbox"/>

SEE PART DRAWING FOR DIMENSIONS

NOTE: UNLESS OTHERWISE SPECIFIED

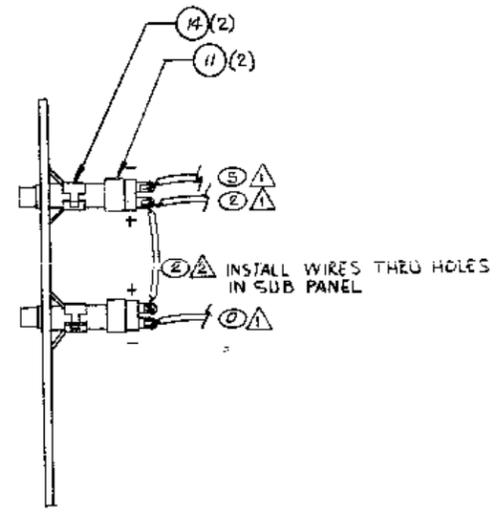
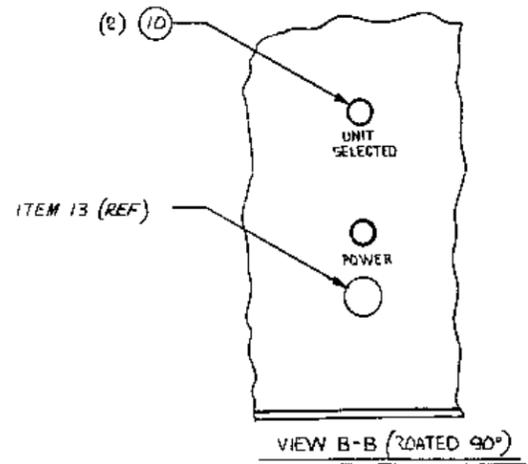
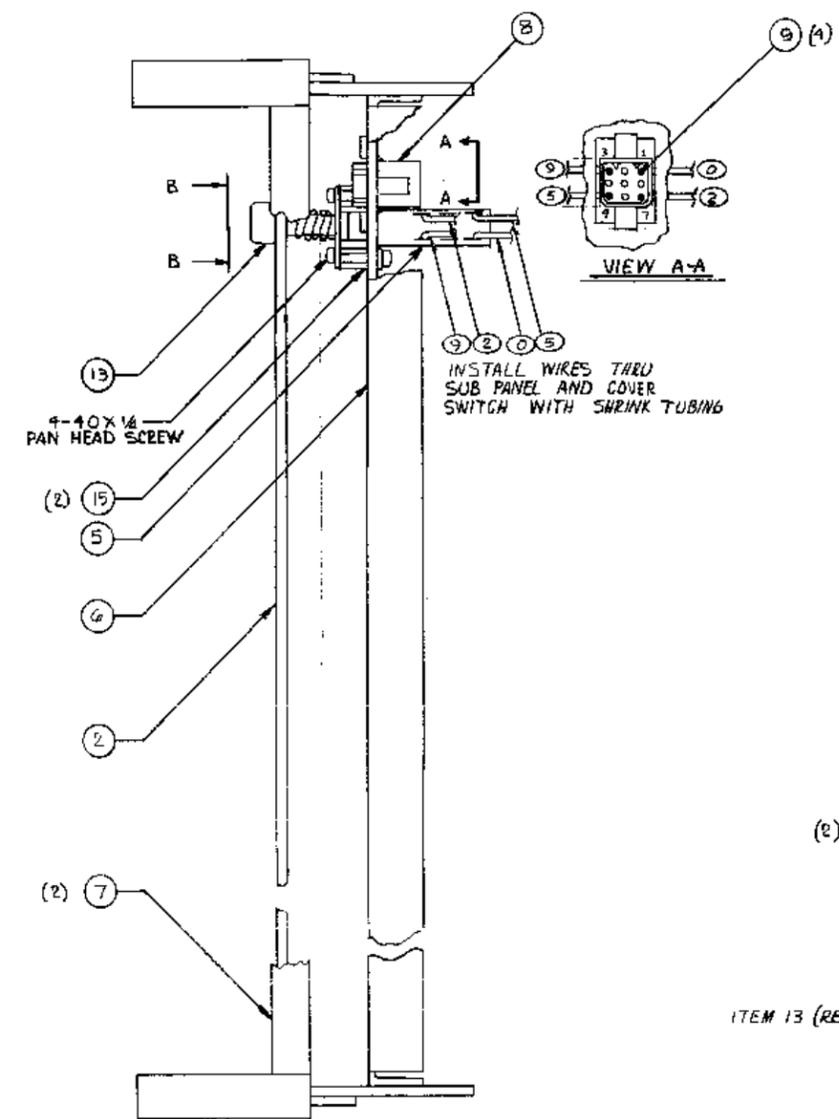
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE		
MATERIAL	PROJ ENGR		TITLE MODIFICATION,	
	RELEASE APPROV		158	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - .010 ANGLES : F XX - .030		MODEL NO 158	DWG NO 1101-00-0044
	DO NOT SCALE DWG		REV A	
SCALE			CODE IDENT 23338	SHEET 1 OF 1

REV	LOG	BY	DATE	APP
A	ECN 1160	Ed	1/16/82	
B	ECN 1315	BA	6/20/85	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

D
C
B
A

D
C
B
A



- 3. ○ DENOTES WIRE COLOR PER RESISTOR CODE
 - △ CUT WIRE TO A LENGTH OF 3"
 - ▲ CUT WIRES TO A LENGTH OF 16" AND STRIP ENDS
- NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: BARNETT	DATE: 9/6	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROCESSED BY: [Signature]	DATE: 10/14	TITLE: FRONT PANEL ASSY-158 OPTION	
FINISH: WAVETEK PROCESS	RELEASE APPROV: [Signature]	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± 0.10 ANGLES: 2° XX ± 0.30	MODEL NO: 159	DWG NO: 0102-00-0336
	SCALE: FULL	DO NOT SCALE DWG	REV: B	
			CODE IDENT: 23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG=FIG#-PART-NO	MGR	WAVETEK NO.	QTY/PT
1000	ASSY DRWS, F1 PVL	0102-00-0330	WVTK	0102-00-0330	1
6	PANEL, BUS	158-323	WVTK	1400-00-0723	1
1 14	GRN	158-324	WVTK	1400-00-0723	2
15 15A	STANDOFF	013-003-2	WVTK	1400-00-2513	2
3 3A	HANDLE, H/A FROM 1440-00-15A1	147-304	WVTK	1400-00-3504	2
4 4A	TRIP, HANDLE REF: 13200-06-0006	147-345	WVTK	1400-00-3019	2
2	HANDLE, FT	158-326	WVTK	1400-00-5570	1
7	TRIP REF: 13200-06-0005	1400-00-7019	WVTK	1400-00-7019	2
8	PLUS, SPIN	03-26-2091	MCLX	2100-02-0311	1
11 11A	CONV, LAMP	515-0074	UILLG	2100-03-0024	2
1000	MIN, MALL	02-06-2193	MCLX	2100-05-1003	4
1000	LAMP, CANI-1001	507-4757-3551-500	UILLG	2400-02-0010	2
14 14A	LIFT	515-0051	UILLG	2800-06-0003	2
5	SWITCH, VOST P5	157-422	WVTK	5103-00-0011	1
13	BUTTON	J-52305-PLACN	CNC	5103-04-0003	1

WAVETEK
PARTS LIST

TITLE
FRONT PANEL ASSY

ASSEMBLY NO
1101-00-0078

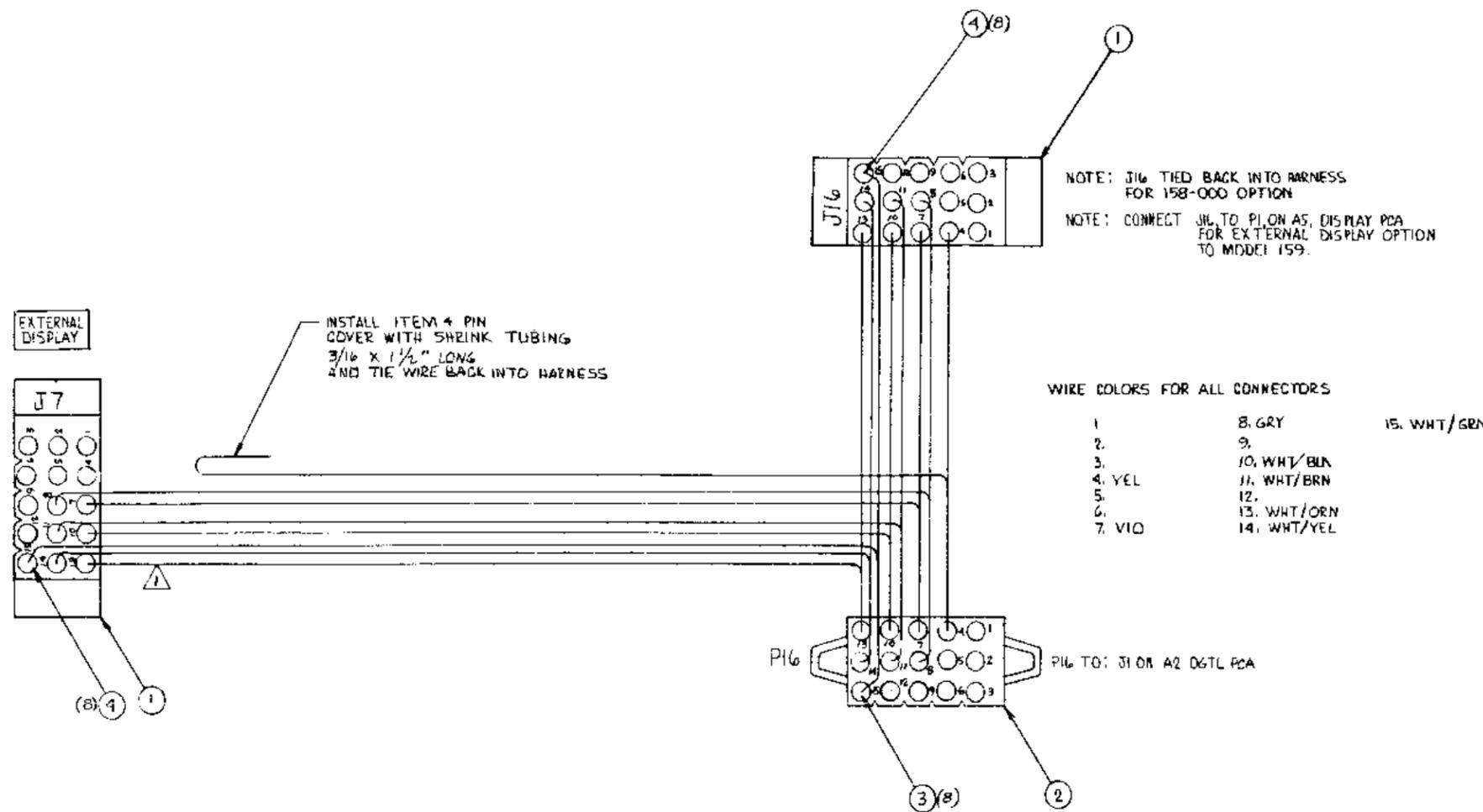
REV
B

PAGE: 1

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PRD. #	TITLE	
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES: 1° XX ± .030	FRONT PANEL ASSY
	DO NOT SCALE DWG	SCALE	
	MODEL NO	DWG NO	REV
	158	1101-00-0078	B
	CODE IDENT	23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



3. TIE WIRES USING SMALL CABLE TIE 23M AS REQ.

⚠ CUT WIRES TO A LENGTH OF 3.0 INCHES

⚠ CUT WIRES TO A LENGTH OF 28.5 INCHES

NDG: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE: 9/2	
MATERIAL	PROV. ENGR: [Signature]	
FINISH: WAVETEK PROCESS	RELEASE APPROV: [Signature]	TITLE: CONNECTOR ASSY - EXT. DISPLAY
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ± .010 ANGLES -1 XX ± .020	MODEL NO: 158
	DO NOT SCALE DWG	DWG NO: 120-00-0005
	SCALE	CODE IDENT: 23338
		SHEET 2 OF 2

APPENDIX A GPIB OPTION 005

A.1 MODEL 159 GPIB

Option 159-005 (General Purpose Interface Bus) is compatible with IEEE Standard 488-1975 and 1978 (for Model 159 purposes, the IEEE 488-1975 and 1978 standards are the same). Previous names, including IEC and HP-IB, always refer to the GPIB.

The GPIB Option 159-005 implements Acceptor Handshake (AH), Listen (L), Remote Enable (REN) and Go To Local (GTL). Group Execute Trigger (GET) is not implemented. No provisions for Service Request or Polling have been made. (The SRQ and EOI lines are not used.)

A.1.1 REN Function

The GPIB equipped generator will be in a Remote Only condition if the GPIB option card is addressed to Listen while the REN line is set. (Remote Only implies that the generator's keyboard will be disabled). Either a Go To Local (GTL) command or resetting the REN line will enable the generator's keyboard.

A.1.2 GPIB Listen Address

The GPIB listen address is independent of the generator unit address. The GPIB card provides the controller-to-instrument transfer of data when ever the GPIB addressed data and instrument GPIB address agree. The GPIB card, when addressed, translates the GPIB data into Wavetek synchronous bus - data (figure A-1). The Wavetek bus then distributes data both to the rear panel for other possible units and also to the main board of this generator. The instrument unit address (not GPIB address) is hardware jumpered to be from 1 through 9. An incoming unit address, ASCII code of G1 through G9, selects the particular 159 instrument to receive new programming information.

Unless otherwise specified, GPIB options are delivered with an address of "(quote mark) for the HP9830 controller (device 02 for the HP9825 and Tektronix 4051 controllers and 34 for the Commodore PET controller. See appendix A for possible addresses). This address can be changed by the switches of component U12A on the GPIB option card.

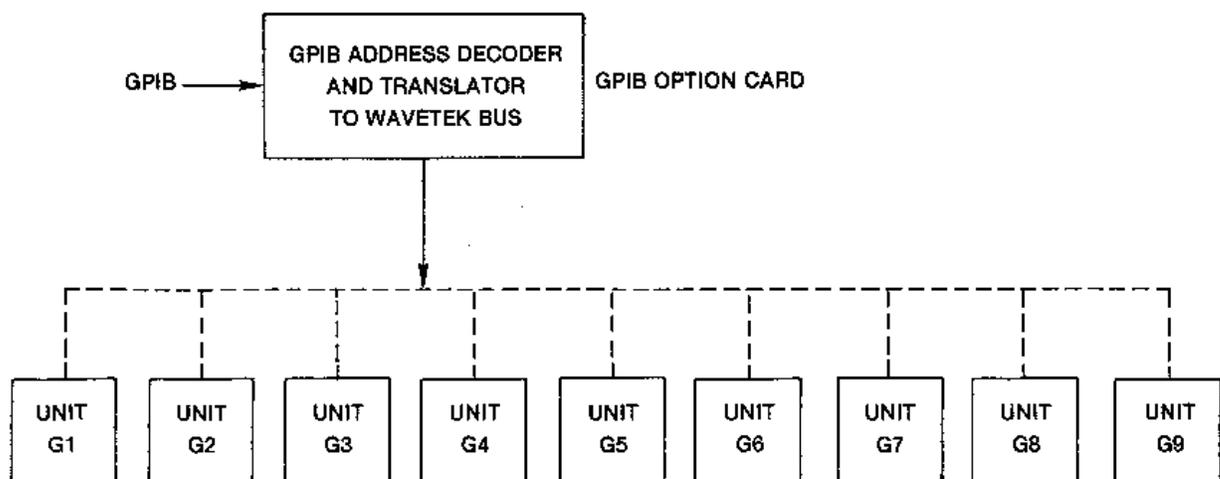


Figure A-1. Wavetek Generators with Unit Address

A.1.3. Changing GPIB Address

Remove the top cover of the 159 and locate the vertically mounted option card at the front of the generator. It is not really necessary to remove the card to make visual inspections or changes to the GPIB address selector, component U12A. A dextrous hand and an insulated narrow tool (e.g., an orange stick or tuning wand) is all that is necessary for changing the GPIB address. However, if you desire greater access, remove the screws at both ends of the mounting bar and remove the card.

The five switches of S1 (figure A-2) correspond to the lower five data I/O lines of the GPIB: switch 1 = DIO1, switch 2 = DIO2, etc. All legal listen addresses are listed in table A-1. Set the switches to 0 or 1 as indicated for the desired addresses.

A.1.4 Unit Address

Unless otherwise specified, the Model 159 is delivered with a unit address of 1 (this is not the GPIB address). The merely inspect for the proper unit address, the frontpanel keyboard and display may be used. By pressing UNIT followed by a number entry of 0 through 9, ventually the UNIT SELECTED LED will light. This indicated that this particular instrument, unit (figure A-1), is selected for programming. Once a unit is selected, all programming that reaches the Wavetek ASCII bus is for that unit; the unit designator need not be repeated unless a different unit is desired. The unit address may similarly be determined via remote programming and the ASCII G code.

The unit address may be changed by repositioning the unit address jumper on the digital board of the generator.

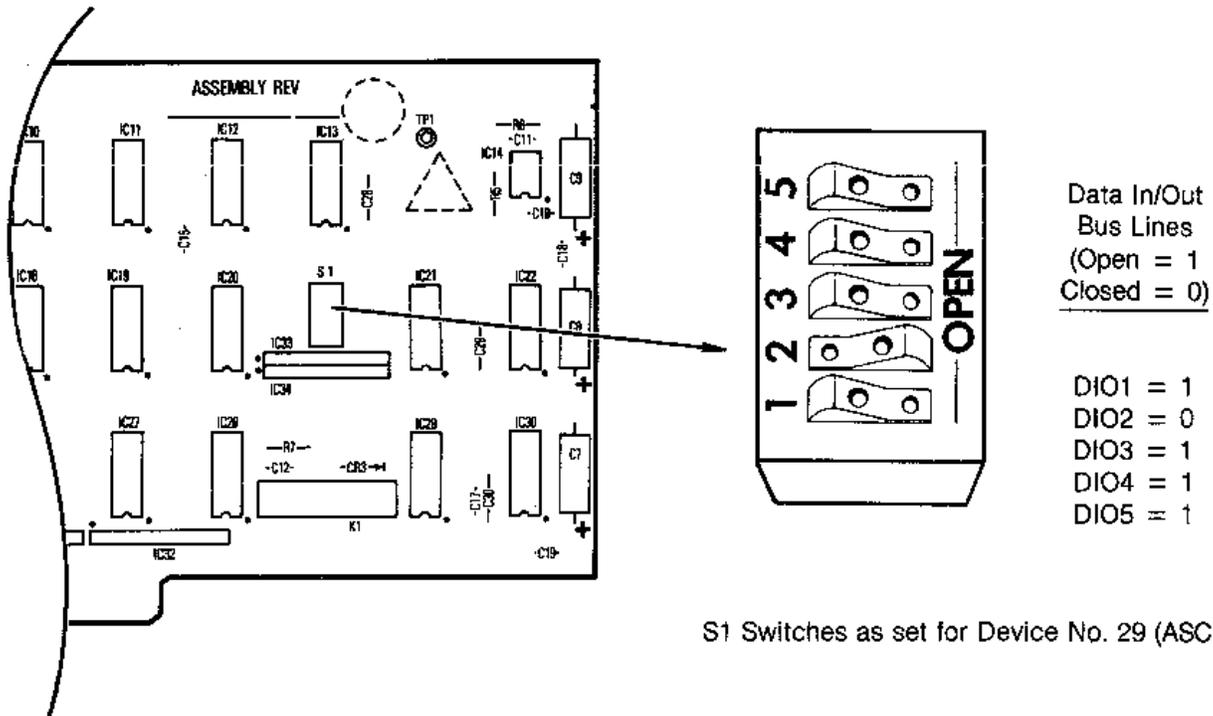


Figure A-2. GPIB Address Selector on the GPIB Option Card.

A.1.5 Changing Unit Address

Remove top and bottom covers of generator. Remove screws from both ends of the analog board front mounting bar (top horizontal board). Rotate and secure analog board in an UP position. Locate address pads E24 through E33. (See figure A-3.) A soldering iron is required to move the jumper on the digital board.

- Jumper E29 to E24 for unit address of 1.
- Jumper E29 to E25 for unit address of 2.
- Jumper E29 to E26 for unit address of 3.
- Jumper E29 to E27 for unit address of 4.
- Jumper E29 to E28 for unit address of 5.
- Jumper E29 to E30 for unit address of 6.
- Jumper E29 to E31 for unit address of 7.
- Jumper E29 to E32 for unit address of 8.
- Jumper E29 to E33 for unit address of 9.

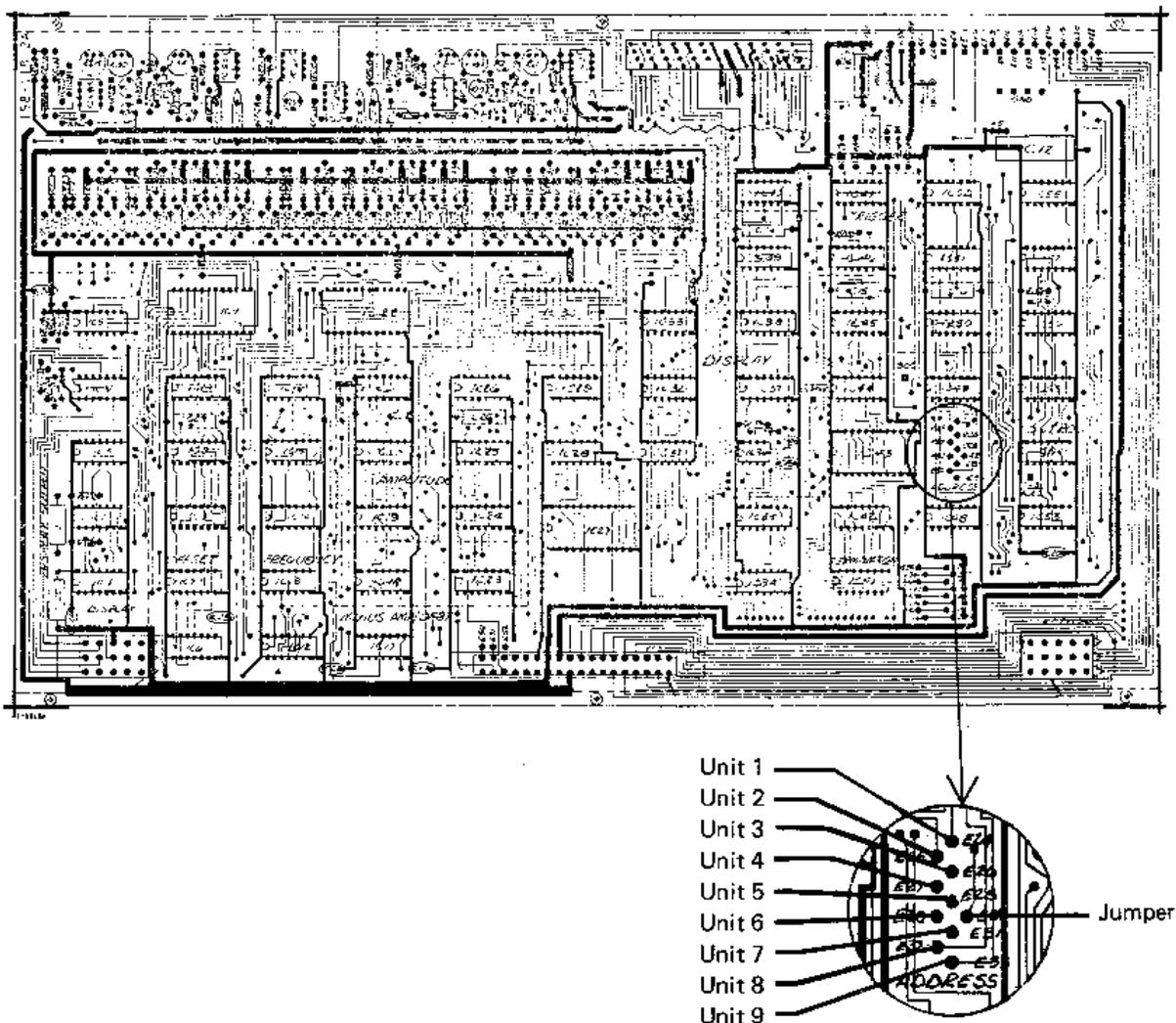


Figure A-3. Model 158/159 Digital Board (Top View)

Table A-1. General Purpose Interface Bus Address

HP9825 TEK4051	HP9830	Primary Listen Address							
		Decimal Value	DIO Bus						
			8	7	6	5	4	3	2
Device 0	SP	32	0	0	1	0	0	0	0
Device 1	!	33	0	0	1	0	0	0	1
Device 2	"	34	0	0	1	0	0	0	1
Device 3	#	35	0	0	1	0	0	0	1
Device 4	\$	36	0	0	1	0	0	1	0
Device 5	%	37	0	0	1	0	0	1	0
Device 6	&	38	0	0	1	0	0	1	1
Device 7	'	39	0	0	1	0	0	1	1
Device 8	(40	0	0	1	0	1	0	0
Device 9)	41	0	0	1	0	1	0	0
Device 10	*	42	0	0	1	0	1	0	1
Device 11	+	43	0	0	1	0	1	0	1
Device 12	,	44	0	0	1	0	1	1	0
Device 13	-	45	0	0	1	0	1	1	0
Device 14	.	46	0	0	1	0	1	1	1
Device 15	/	47	0	0	1	0	1	1	1
Device 16	0	48	0	0	1	1	0	0	0
Device 17	1	49	0	0	1	1	0	0	0
Device 18	2	50	0	0	1	1	0	0	1
Device 19	3	51	0	0	1	1	0	0	1
Device 20	4	52	0	0	1	1	0	1	0
Device 21	5	53	0	0	1	1	0	1	0
Device 22	6	54	0	0	1	1	0	1	1
Device 23	7	55	0	0	1	1	0	1	1
Device 24	8	56	0	0	1	1	1	0	0
Device 25	9	57	0	0	1	1	1	0	0
Device 26	:	58	0	0	1	1	1	0	1
Device 27	;	59	0	0	1	1	1	0	1
Device 28	<	60	0	0	1	1	1	1	0
Device 29	=	61	0	0	1	1	1	1	0
Device 30	>	62	0	0	1	1	1	1	0
Unlisten	?	63	0	0	1	1	1	1	1

NOTE: Unlisten (?) cannot be used as an address.

5	4	3	2	1
Switch Sections				

A.2 PROGRAM EXAMPLE USING COMMODORE PET CONTROLLER

This program demonstrates the Model 159 only. Other instruments may be left (with power on) connected to the bus provided none of them have the GPIB address on "1". The controller is the Commodore PET with 8K memory.

Display the 159 output on an oscilloscope triggering externally from the 159 SYNC OUT.

Run the program as outlined in the following steps:

1. Turn the PET on (power switch is at the left rear of the PET).
2. Insert the tape cartridge into the tape drive.
3. Type:

```
LOAD "DEMO 159"
```

Press RETURN.

4. The PET will instruct you to press PLAY on the tape drive. The tape will advance and load the program.
5. When "READY" and flashing "BASIC" appear, type:

```
RUN
```

Press RETURN.

6. The program is now running. The flashing "BASIC" indicates that the program is finished. The program will normally terminate (exit) itself upon its conclusion.

NOTES: 1. To terminate a program immediately, press STOP. To restart a program, type:

```
RUN
```

Press RETURN.

2. In loading (searching) for a particular program, the tape will only advance forward. You must re-wind the tape to load a program that has been passed.
3. The PET is much slower than the Model 159.

```
10 PRINT"159 DEMO"
20 REM 28 JAN '80
30 REM 159 ADDRESS SET TO 1
40 OPEN 2,33
50 REM UNIT NUMBER IS ONE
60 PRINT#2,"G1"
70 REM INITIALIZE
80 PRINT#2,"F100E3A999E0D0B0C0H"
90 TIS="000000"
95 IFTI<60GOTO95
100 FORC=0TO3
110 PRINT#2"C",C
120 TIS="000000"
125 IFTI<60GOTO125
130 NEXTC
140 PRINT#2,"C0"
150 REM FREQUENCY***
160 FORF=100TO950STEP25
```

```

170 PRINT#2,"F",F
180 TIS="000000"
185 IFTI<10GOTO185
190 NEXTF
200 FORF=950TO100STEP-25
210 PRINT#2,"F",F
220 TIS="000000"
225 IFTI<10GOTO225
230 NEXTF
240 REM AMPLITUDE ***
250 FORA=999TO-951STEP-50
260 REM 3 DIGITS FOR AMPLITUDE
270 IFABS(A)<10THENPRINT#2,"A00",A
280 IFABS(A)>=10ANDABS(A)<100THENPRINT#
2,"A0",A
290 IFABS(A)>=100THENPRINT#2,"A",A
300 TIS="000000"
305 IFTI<10GOTO305
310 NEXTA
320 FORA=-951TO499STEP50
330 IFABS(A)<10THENPRINT#2,"A00",A
340 IFABS(A)>=10ANDABS(A)<100THENPRINT#
2,"A0",A
350 IFABS(A)>=100THENPRINT#2,"A",A
360 TIS="000000"
365 IFTI<10GOTO365
370 NEXTA
380 REM D C OFFSET **
390 FORD=0TO250STEP25
400 REM 3 DIGITS FOR AMPLITUDE
410 REM A SUBROUTINE USED THIS EXAMPLE
420 GOSUB440
430 GOTO500
440 REM 3 DIGIT ROUTINE
450 IFABS(D)<10THENPRINT#2,"D00",D
460 IFABS(D)>=10ANDABS(D)<100THENPRINT#
2,"D0",D
470 IFABS(D)>=100THENPRINT#2,"D",D
480 TIS="000000"
485 IFTI<10GOTO485
490 RETURN
500 NEXTD
510 FORD=250TO-250STEP-25
520 REM 3 DIGIT ROUTINE
530 GOSUB440
580 NEXTD
590 REM TRIGGERED MODE W/TRIG'S **
600 FORI=1TO1000
610 PRINT#2,"B1"
620 NEXTI
630 PRINT#2,"F100E3A999E0D0B0C0H"

```

A.3 PROGRAMMING EXAMPLE USING HP 9830 CONTROLLER

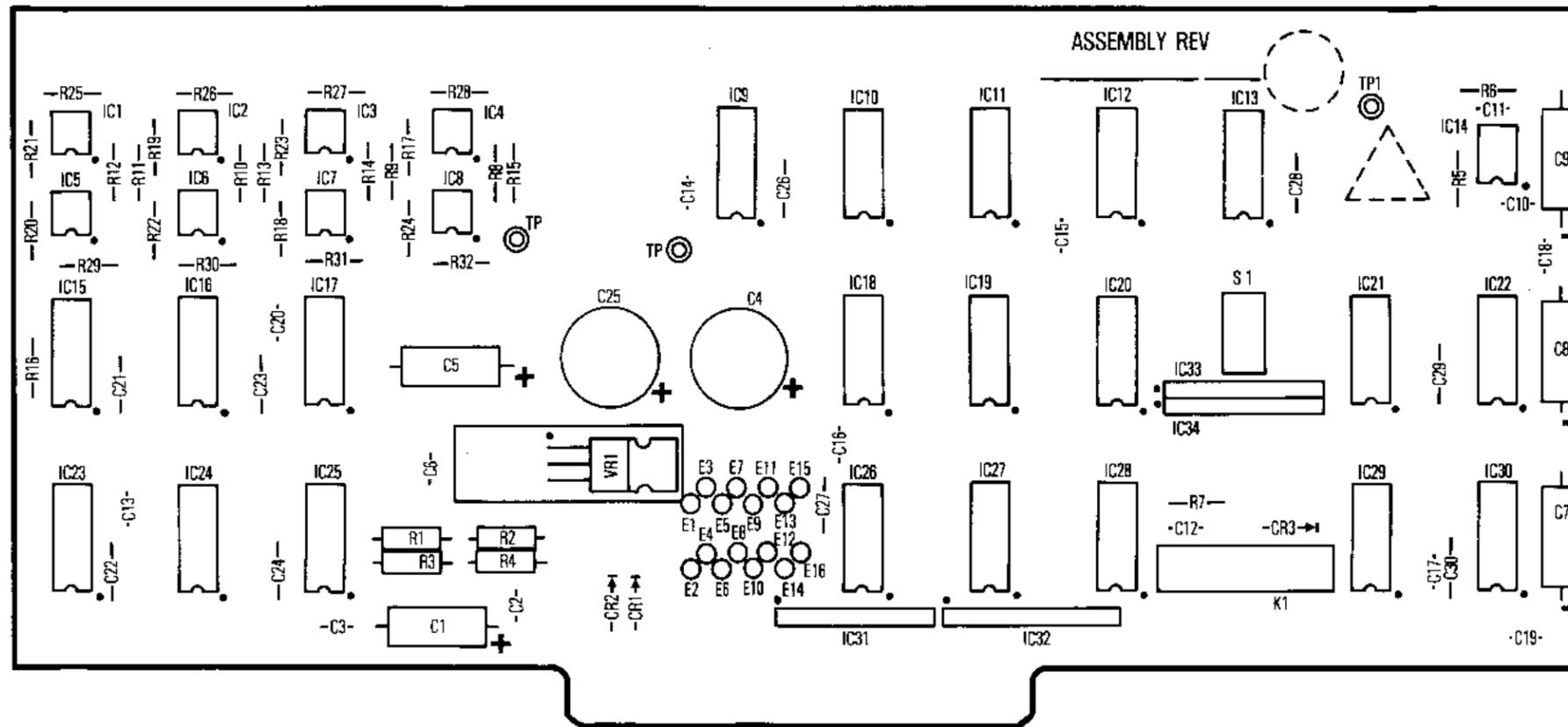
```

100 REM PROGRAM DEMONSTRATES USE OF WAVETEK MODEL 158-159 GENERATOR
110 REM ASSUMES MODEL 30 CALCULATOR WITH EXTENDED I/O
120 REM 9820 AND 21 CALCULATORS USE FORMAT B AND WBYTE CMD COMMANDS
130 REM
140 REM UNIT IS ADDRESSED BY A CMD "?U>" "G1"
150 CMD "?U>" "G1"
160 REM WHERE THE FIRST GROUP SELECTS H/P BUS (UNIT 13) UNLISTENS (?),
170 REM THEN SELECTS CALCULATOR TO BE TALKER, > IS ADDRESSED AS A LISTENER
180 REM SECOND GROUP SELECTS UNIT 1 ATN IS SET FOR FIRST GROUP, RESET FOR SECOND
190 REM A1 IS THE UNIT NUMBER; 13 FOR H-P INTERFACE BUS
200 A1=13
210 REM
220 REM AMPLITUDE MAY BE DRIVEN BY;
230 A=5
240 OUTPUT (A1,250)A;
250 FORMAT "A",E9.2
260 REM SEMICOLON INHIBITS CR, LF.
270 REM
280 REM FREQUENCY MAY BE DRIVEN BY;
290 F=1234567
300 OUTPUT (A1,310)F;
305 REM USE OF 1000 FORMAT SPECIFICATION DELETES LEADING BLANKS
310 FORMAT "F",E1000.2
320 REM
330 REM OFFSET MAY BE DRIVEN BY;
340 O=1
350 OUTPUT (A1,360)O;
360 FORMAT "D",F6.2
370 REM NOTE THAT OFFSET DOES NOT HAVE A MULTIPLIER DIGIT
380 REM
390 REM FUNCTION AND MODE ARE DRIVEN BY;
400 OUTPUT (A1,*)"B0 C0";
410 REM WOULD SELECT MODE (B) 0, CONTINUOUS, FUNCTION (C) 0 SIN. .
420 REM LEGAL MODE VALUES ARE 0,1,2; FUNCTION INCLUDES 0,1,2,3. .
430 REM OUTPUT IS ENABLED BY;
440 OUTPUT (A1,*)"H"
450 REM WHERE H ENABLES OUTPUT OF GENERATOR TO CONNECTOR. . .
460 REM SENDING AN "I" WILL DISCONNECT GENERATOR OUTPUT.
470 REM
480 REM SPECIAL CHARACTERS CONTROL H-P INTERFACE BUS. . .
490 REM ATN IS ENABLED BY OUTPUT (13,500)256;
500 FORMAT B
510 REM ATN IS RESET BY OUTPUT (13,500)512;
520 REM THESE COMMANDS MAY BE CONCATENATED TO GENERATE UNIVERSAL COMMANDS
530 OUTPUT (A1,500)256.1.512;
540 REM WILL SET ATN, OUTPUT A GO TO LOCAL CHARACTER 'GTL=01', THEN TURN ATN OFF
550 REM
560 OUTPUT (A1,500)768;
570 REM WILL ASSERT THE REN LINE TO ENABLE INSTRUMENTS IN THE REMOTE MODE
580 REM ****NOTE INSTRUMENT WILL NOT GO REMOTE UNTIL ADDRESSED. .
590 REM UNIT WILL STAY REMOTE UNTIL A 'GTL' OR REN IS RESET. .
600 REM UNLISTEN ALL DEVICES
610 CMD "? "
620 REM REN IS RESET BY;
630 OUTPUT (A1,500)1024;
640 DISP "END TEST";
650 STOP
660 REM
670 REM *****
680 REM
690 REM SAMPLE PROGRAM
700 A=0
710 F=123456
720 O=M=U=0
730 REM MODE=FUNCTION=0=CONTINUOUS, SIN WAVE. . .
740 REM ADDRESSES THE UNIT ON THE H-P INTERFACE BUS WITH REN ENABLED
750 OUTPUT (13,500)768
760 CMD "?U>"
770 OUTPUT (13,780)A,F,O,U,M;
780 FORMAT "G1A",E9.2,"F",E9.2,"D",F6.2,"B",F4.0,"C",F4.0,"HA"
790 REM LAST A DISPLAYS AMPLITUDE ON MODEL 159 DISPLAY. . .
800 FOR L=1 TO 100
810 OUTPUT (13,820)A;
820 FORMAT "A",E1000.2
830 A=9.99*RND(5)
840 DISP L
850 NEXT L
860 REM SENDS GTL TO ADDRESSED UNIT ONLY TO ENABLE KEYBOARD. . .

```

```
870 OUTPUT (13,500)256,1,512;  
880 REM REN IS STILL ASSERTED.  
890 DISP "STOP ** CONT-EXE TO REPEAT";  
900 CMD "?"  
910 STOP  
920 GOTO 700  
930 REM NOTE STOP BUTTON WILL ISSUE EOP-ICL INTRFC CLEAR WHICH WILL SEND  
940 REM 159 TO LOCAL MODE. . . .  
950 REM  
960 REM *****  
970 REM  
980 END
```


THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJECT NO.		FILE	
	RELEASE APPROV.		PCA GPIB INTERFACE BD. OPT. 005	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - DIM ANGLES - 1 XX - 30	DO NOT SCALE DWG	MODEL NO.	DWG NO.
SCALE			159	0101-00-0972
	CODE IDENT	23338	SHEET	06

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, IEC INTERFACE	0101-00-0972	WVTK	0101-00-0972	1
NONE	SCHEMATIC, IEC INTERFACE	0103-00-0972	WVTK	0103-00-0972	1
C11	CAP, CER, MN, .01MF, 50V	CAC0225U103Z100A	CORND	1500-01-0210	1
C12 C14 C15 C16 C18 C2 C21 C22 C23 C24 C26 C27 C28 C29 C30 C6	CAP, CER, NON, .1MF, 50V	CAC032U104Z050A	CORND	1500-01-0405	16
C10	CAP, CER, 470PF, 1KV	DD-471	ARCO	1500-04-7111	1
C25 C4	CAP, ELECT, 1000NF/35V RADIAL LEAD	CRE-SERIES-1000/35	CAPAR	1500-31-0202	2
C19	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	1
C3	CAP, TANT, 27MF, 35V	196D276X0035FB	SPRAG	1500-72-7602	1
C1 C5 C7 C8 C9	CAP, TANT, 33MF, 10V	150D336X9010B2	SPRAG	1500-73-3601	5
NONE	IEC INTERFACE	1700-00-0972	WVTK	1700-00-0972	1
NONE	PIN, MALE	611B2-2	AMP	2100-05-0020	3
NONE	STANDOFF, SWAGE .125 H., .250 DIA 4-40, .062 MAT'L	95316-0440-3A	AMTOM	2800-03-0004	2
NONE	HEAT SINK	2800-11-0002	WVTK	2800-11-0002	1
NONE	WASHER, SHOULDER	2661	SMITH	2800-27-0002	2

WAVETEK
PARTS LIST

TITLE
PCA, IEC INTERFACE

ASSEMBLY NO.
1100-00-0972
PAGE: 1

REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
K1	RELAY, REED, FORM-A	RA3019-1051	ETROL	4500-00-0007	1
R1 R2 R3 R4	RES, C, 1/2W, 5%, 10	RC209F-106	BTMPL	4700-25-0100	4
R10 R11 R12 R13 R14 R15 R8 R9	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	8
R17 R18 R19 R20 R21 R22 R23 R24	RES, MF, 1/8W, 1%, 20, 5K	RN55D-2052F	TRW	4701-03-2052	8
R16	RES, MF, 1/8W, 1%, 2, 21K	RN55D-2211F	TRW	4701-03-2211	1
R6	RES, MF, 1/8W, 1%, 30, 1K	RN55D-3012F	TRW	4701-03-3012	1
R5	RES, MF, 1/8W, 1%, 4, 99K	RN55D-4991F	TRW	4701-03-4991	1
R7	RES, MF, 1/8W, 1%, 61, 9	RN55D-6199F	TRW	4701-03-6199	1
R25 R26 R27 R28 R29 R30 R31 R32	RES, MF, 1/8W, 1%, 75, 7K	RN55D-7872F	TRW	4701-03-7872	8
IC31 IC32 IC33 IC34	RESISTOR MOD	159-520	WVTK	4770-00-0005	4
CR1 CR2	DIODE	5CE-1	GEHT	4801-02-0001	2
CR3	DIODE	FD-6666	FAIR	4807-02-6666	1
S1	SWITCH PC	500-105	DUNCN	5199-00-0001	1
IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8	OPTO-COUPLER	4N26	SPECT	7000-04-2600	8
IC14	IC	NE555V	SIG	7000-05-5500	1

WAVETEK
PARTS LIST

TITLE
PCA, IEC INTERFACE

ASSEMBLY NO.
1100-00-0972
PAGE: 2

REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
IC19 IC23 IC24	IC	7400	TI	8000-74-0000	3
IC26 IC27	IC	7404	TI	8000-74-0400	2
IC18 IC20	IC	7405	TI	8000-74-0500	2
IC30	IC	7408	TI	8000-74-0800	1
IC21	IC	7410	TI	8000-74-1000	1
IC11	IC	7430	TI	8000-74-3000	1
IC10 IC17 IC25 IC29 IC9	IC	7438	TI	8000-74-3800	5
IC28	IC	7474	TI	8000-74-7400	1
VR1	VOLTAGE REGULATOR	7805393	FAIR	8000-78-0500	1
IC12 IC13	IC	8242	SIG	8000-82-4200	2
IC22	IC	74107	TI	8007-41-0700	1
IC15 IC16	IC	74132	TI	8007-41-3200	2

WAVETEK
PARTS LIST

TITLE
PCA, IEC INTERFACE

ASSEMBLY NO.
1100-00-0972
PAGE: 3

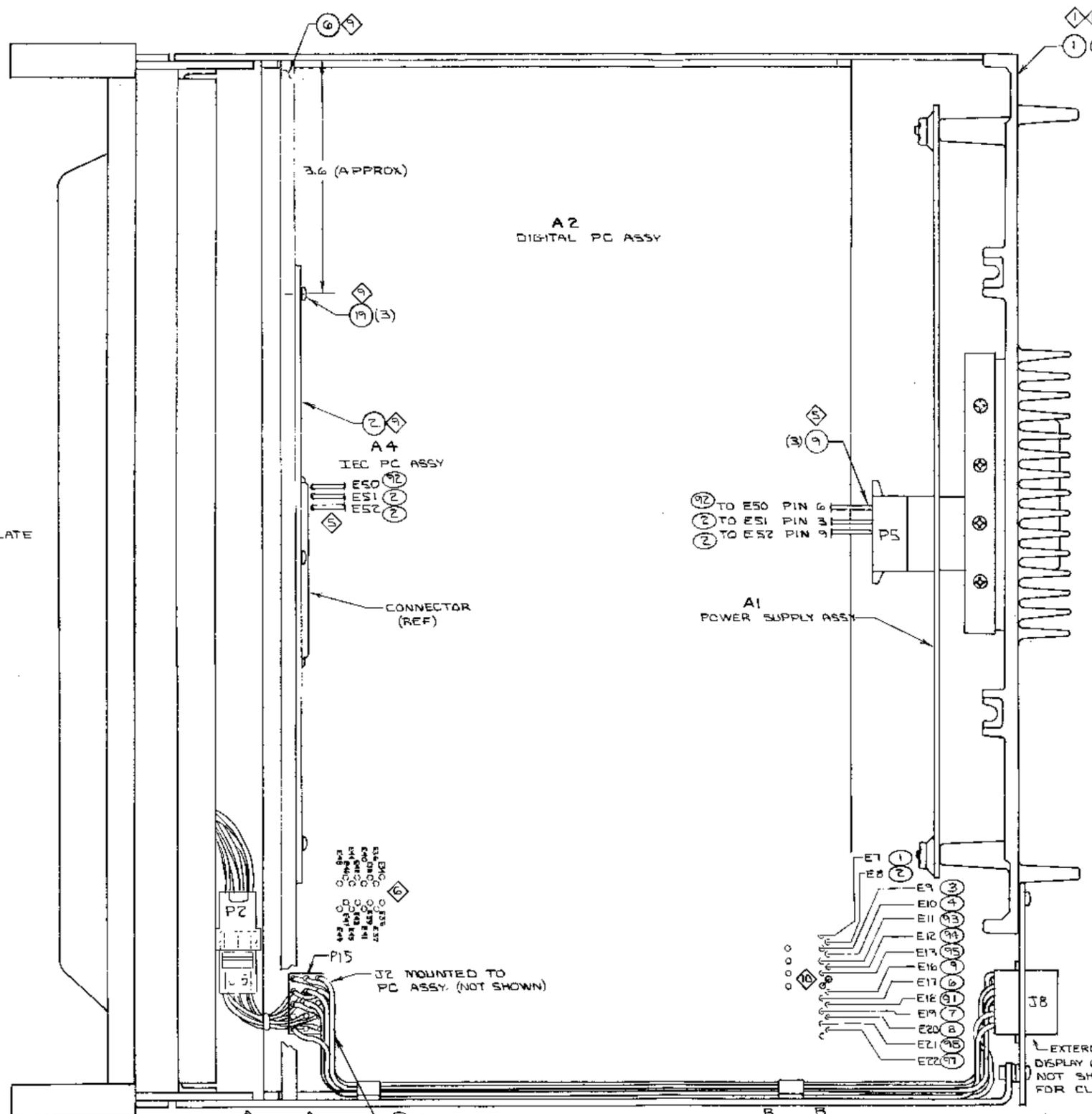
REV

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	<p>WAVETEK SAN DIEGO • CALIFORNIA</p> <p>TITLE PARTS LIST PCA IEC (GPIB) INTERFACE</p>
MATERIAL	PROJECTOR	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX-.919 ANGLES .1° XX-.000		
SCALE	DO NOT SCALE DWG	MODEL NO.	
		159	1100-00-0972
		EDGE IDENT 23338	SHEET 1 OF 1

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



1 (TOP & BOTTOM COVERS & ANALOG PC ASSY NOT SHOWN FOR CLARITY)

A2 DIGITAL PC ASSY

A4 IEC PC ASSY

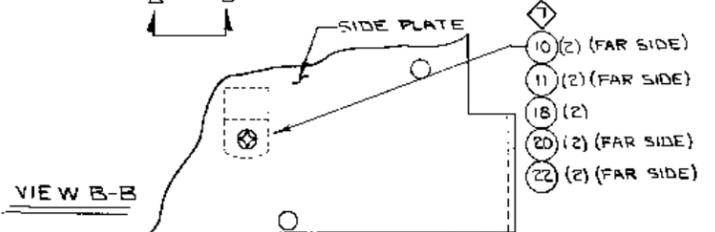
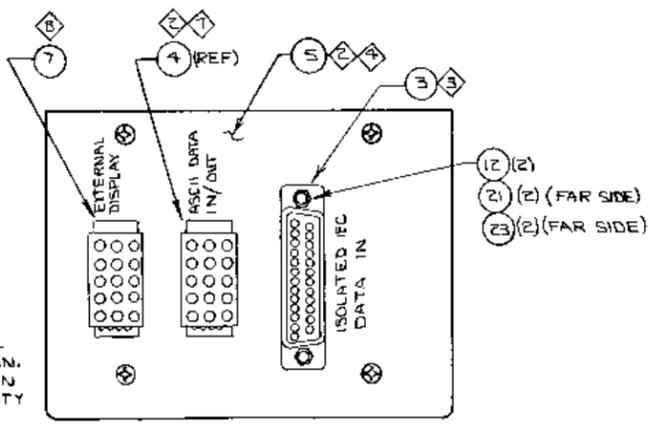
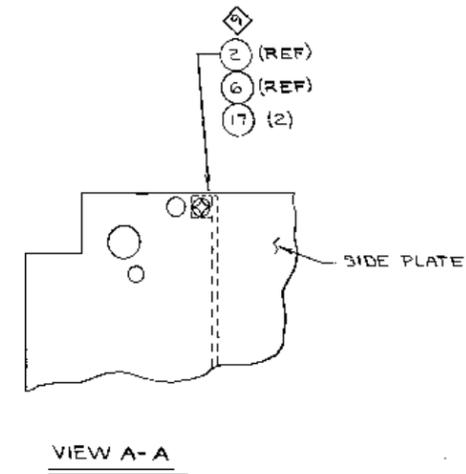
A1 POWER SUPPLY ASSY

CONNECTOR (REF)

ES0
ES1
ES2
ES3
ES4
ES5
ES6
ES7
ES8
ES9
ES10
ES11
ES12
ES13
ES14
ES15
ES16
ES17
ES18
ES19
ES20
ES21
ES22
ES23
ES24
ES25
ES26
ES27
ES28
ES29
ES30
ES31
ES32
ES33
ES34
ES35
ES36
ES37
ES38
ES39
ES40
ES41
ES42
ES43
ES44
ES45
ES46
ES47
ES48
ES49
ES50
ES51
ES52
ES53
ES54
ES55
ES56
ES57
ES58
ES59
ES60
ES61
ES62
ES63
ES64
ES65
ES66
ES67
ES68
ES69
ES70
ES71
ES72
ES73
ES74
ES75
ES76
ES77
ES78
ES79
ES80
ES81
ES82
ES83
ES84
ES85
ES86
ES87
ES88
ES89
ES90
ES91
ES92
ES93
ES94
ES95
ES96
ES97
ES98
ES99
ES100

J2 MOUNTED TO PC ASSY. (NOT SHOWN)

EXTERNAL DISPLAY CONN. NOT SHOWN FOR CLARITY



- ▲ PULL HARDWARE FOR FIELD INSTALLATION ONLY.
- 3.◇ DENOTES LINE NUMBER FOR MODIFICATION PROCEDURE. (SEE SHT 2)
- ▲ PROGRAMMING MATING CONNECTORS: IDENTIFY PARTS BY BAG AND TAG AND SHIP WITH INSTRUMENT.
- DENOTES WIRE COLOR PER RESISTOR CODE.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES MATERIAL	DRAWN ADKINS	DATE 7-27-79	WAVETEK SAN DIEGO - CALIFORNIA TITLE MODIFICATION DWG IEC OPTION
FINISH WAVETEK PROCESS	PROF ENGR [Signature]	19/1/79	
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 0.10 ANGLES 1:1 XX ± 0.20	DO NOT SCALE DWG	MODEL NO. 159
	SCALE 1/1		OWN NO. 0102-00-0351
			REV
			CODE IDENT 23338
			SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

MODIFICATION PROCEDURE
IEC OPTION

- 1 REMOVE TOP AND BOTTOM COVERS.
- 2 REMOVE ASCII DATA IN/OUT MOLEX CONNECTOR J9 FROM EXISTING REAR PANEL EXTENDER P/N 400-00-070. REMOVE REAR PANEL EXTENDER AND RETURN TO STOCK. UNSOLDER ALL WIRES THAT GO TO THE A2 DIGITAL PC ASSY, FROM ASCII DATA IN/OUT CONNECTOR J9, AND RETURN THE CONNECTOR ASSY TO STOCK.
- 3 INSTALL THE IEC CABLE ASSY, P/N 203-00-0002 AND CONNECT WIRES AS SHOWN (REF INTERCONNECT 158-230 J9)
- 4 INSTALL EXTENDER REAR CASTING P/N 400-00-5590 AS SHOWN.
- 5 DISCONNECT THE MOLEX CONNECTOR, P5, FROM THE POWER SUPPLY PC ASSY A1. ATTACH MOLEX PINS P/N 200-05-0026, QTY (3), TO THE ENDS OF THREE WIRES. TWO OF THE WIRES TO BE, 22 AWG, RED, 13.5 INCHES LONG, AND ONE WIRE TO BE 22 AWG, WHI/RED, 13.5 INCHES LONG. INSTALL THE MOLEX PINS AND WIRES INTO P5 AS SHOWN AND SOLDER THE OTHER ENDS TO E50, E51, AND E52. (REF INTERCONNECT 158-30 P5)
- 6 REMOVE JUMPERS FROM PADS E34 THRU E49 ON A2 DIGITAL PC ASSY.
- 7 DISCONNECT KEYBOARD MOLEX P2 FROM J2 AND INSTALL CONNECTOR ASSY, ASCII DATA IN/OUT, P/N 203-00-0003 TO J2. CONNECT THE OTHER END TO THE KEYBOARD MOLEX P2. CONNECT THE OTHER END TO THE KEYBOARD MOLEX P2. INSTALL MOLEX J8, TO ASCII DATA

DWG NO 0102-00-0351 REV 5H2

IN/OUT, LOCATED ON THE REAR PANEL EXTENDER AS SHOWN.

- 8 INSTALL EMPTY MOLEX CONNECTOR P/N 200-02-0012, IN THE EXTERNAL DISPLAY LOCATION ON THE EXTENDER REAR CASTING P/N 400-00-5590.
- 9 INSTALL MTG BAR (OPTION CARD) P/N 400-00-5382, TO PC ASSY IEC, P/N 100-00-0142, AS SHOWN AND PLUG INTO CONNECTOR ON A2 DIGITAL PC BOARD.
NOTE: IF PHOTO ISOLATION IS NOT REQUIRED INSTALL JUMPERS TO PADS E1 AND E2, E3 AND E4, E5 AND E6, E7 AND E8, E9 AND E10, E11 AND E12, E13 AND E14, E15 AND E16 AS SHOWN ON THE IEC PC ASSY.
- 10 INSTALL A JUMPER FROM E14 TO E15, ON THE A2 DIGITAL PC ASSY AS SHOWN.
- 11 INSTALL TOP AND BOTTOM COVERS.

DWG NO 0102-00-0351 REV 5H3

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES		DATE 6-10-92	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR	RELEASE APPROV	TITLE MODIFICATION IEC OPTION	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XX .010 ANGLES 11 XX .030		MODEL NO 159	DWG NO 0102-00-0351
DO NOT SCALE DWG		SCALE	CODE 23338	REV
			SHEET 2 OF 2	

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV ECN BY DATE APP

REFERENCE DESIGNATORS	PART DESCRIPTION	UNLESS OTHERWISE SPECIFIED	PLCY	WAVETEK NO.	QTY/PI
NONE	ASST DRWG, IEC MOD	1102-00-0351	WVTK	2102-00-0351	1
3	CABLE ASSY	150-035	WVTK	1207-00-0034	1
4	CABLE ASSY	150-035	WVTK	1207-00-0035	1
6	BAR,SUPP	150-530	WVTK	1400-00-5565	1
9	EAF,CASTING	150-533	WVTK	1400-00-5540	1
7	CONN,15PIN	03-09-1151	WVLEK	2100-02-0012	1
8	PLUG,15PIN	03-09-2151	WVLEK	2100-02-0013	1
NONE	PIN,MALE	02-09-2116	WVLEK	2100-05-0005	10
10	CABLE LAMP	855	SMITH	2200-00-0010	2
11 11A	METALREIN,SPRING	0-191	HEKOP	2800-04-0007	2
12 12A	JACK SCREW	438-146475	AMFN	2800-25-0000	2

WAVETEK
PARTS LIST

TITLE
MODIFICATION KIT

ASSEMBLY NO.
1101-00-0229
PAGE: 1

REV
B

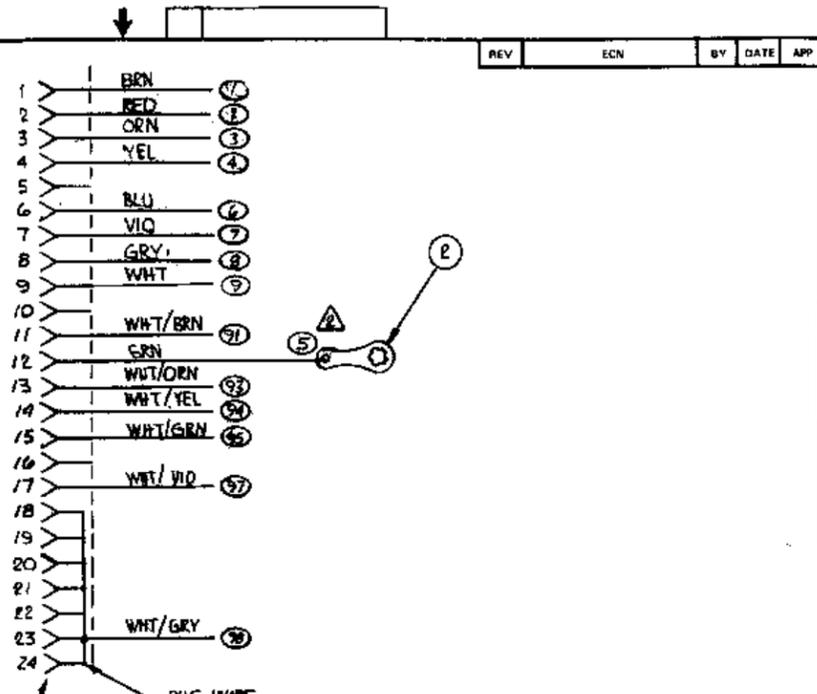
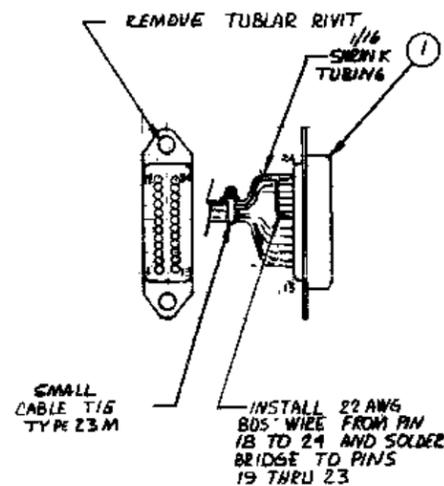
LAWSON GRAPHICS PRINTING CO. INC. 1984

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJ ENGR		
FINISH WAVETEK PROCESS	RELEASE APPROV		TITLE PARTS LIST MODIFICATION, IEC (GP13) OPTION
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XX ± .010 ANGLES : F .XX : .030		
DO NOT SCALE DWG	MODL NO	DWG NO	REV
SCALE	159	1101-00-0229	B
	CODE IDENT	23338	SHEET (OF 1

NOTE: UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



4. SOLDER WIRES TO CONNECTOR AS SHOWN IN DIAGRAM.
3. CUT WIRES TO A LENGTH OF 5.00.
2. CUT WIRE TO A LENGTH OF 3.50 AND SOLDER TO LUG
1. O DENOTES WIRE COLOR PER RESISTOR COLOR CODE

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN BARNETT	DATE 7-24	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJECT <i>APC</i>	RELEASE APPROV <i>APC</i>	TITLE CABLE ASSY- IEC OPTION	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES 1:1 XX ±.030		MODEL NO. 159-005	DWG NO. 1203-00-0002
SCALE FULL	DO NOT SCALE DWG	CODE IDENT 23338	REV	SHEET 2 OF 2

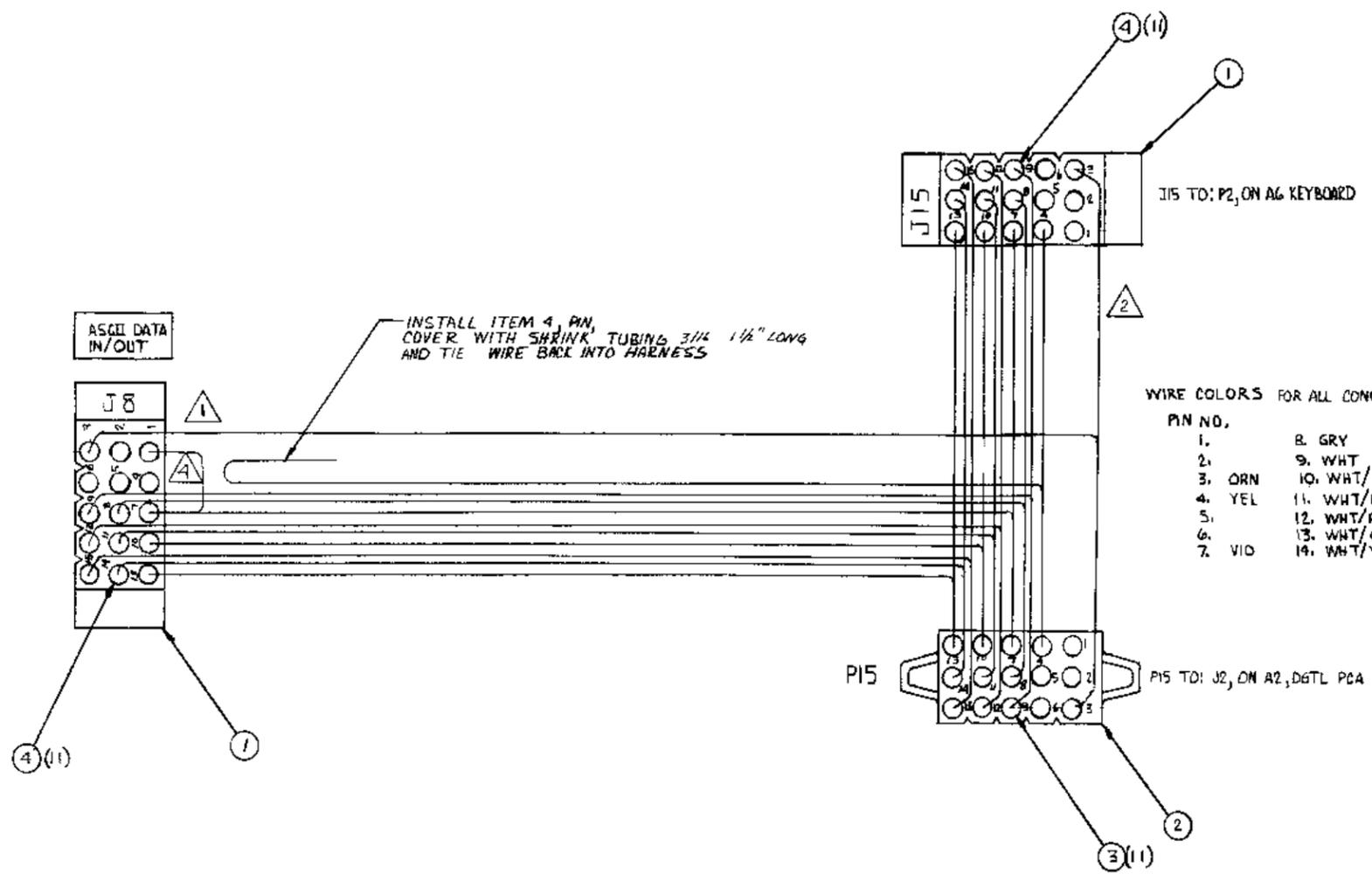
REFERENCE DESIGNATORS	PART DESCRIPTION	DNIG-MFGK-PART-NU	MFGN	WAVETEK NO.	QTY/PT
1	CONN	57-20240	AMP	2100-02-0060	1
2	TERM, LUG LUG	1410-6	SMITH	2100-04-0009	1

WAVETEK PARTS LIST	TITLE CABLE ASSY	ASSEMBLY NO. 1207-00-0004	REV
		Page 1	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJECT	RELEASE APPROV	TITLE CABLE ASSY IEC (GP13) OPTION	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES 1:1 XX ±.030		MODEL NO. 159-005	DWG NO. 1207-00-0004
SCALE FULL	DO NOT SCALE DWG	CODE IDENT 23338	REV	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



REFERENCE DESIGNATOR	PART DESCRIPTION	QTY	UNIT	REV	
L 1A	LONG, 15PIN	03-07-0101	MULEX	2300-02-0010	2
E	PLUG, 15PIN	03-07-0101	MULEX	2300-02-0010	1
NOTE	PIN, MALE	02-09-0110	MULEX	2300-03-0005	11
NOTE	PIN, FEMALE	02-09-0110	MULEX	2300-03-0020	22

WAVETEK PARTS LIST

TITLE: CABLE ASSY

ASSEMBLY NO.: 1203-00-0005

REV: PAGE 1

- ⚠ WIRE COLOR TO BE VID CUT WIRE TO A LENGTH OF 1.00
 - 3. TIE WIRES USING SMALL CABLE TIE 23M AS REQ.
 - ⚠ CUT WIRES TO A LENGTH OF 3.00
 - ⚠ CUT WIRES TO A LENGTH OF 16.50
- NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE: 12/14/91	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	RELEASE APPROV: [Signature]	TITLE: CONNECTOR ASSY ASCII DATA IN/OUT
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: .XX ± .010 ANGLES: 11° XX ± .030	MODEL NO: 158/159
SCALE: NONE	DO NOT SCALE DWG	DWG NO: 1203-00-0003
	CODE IDENT: 23338	REV: SHEET 2 OF 2