

INSTRUCTION MANUAL

Model 191
20 MHz Pulse/Function
Generator

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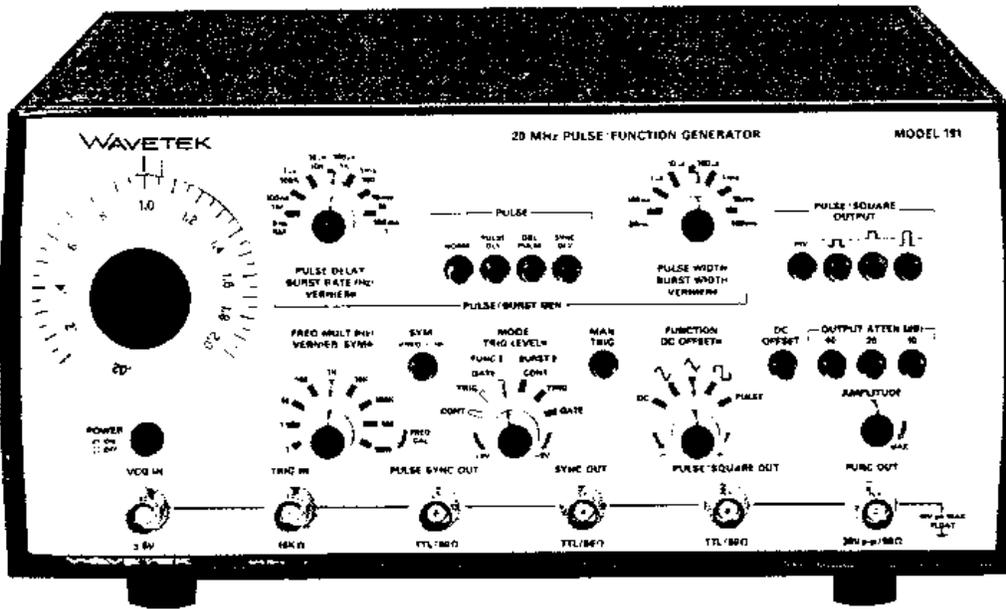
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SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with \oplus or \triangle).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.



Model 191, 20 MHz Pulse/Function Generator

1.1 THE MODEL 191

Wavetek Model 191, a 20 MHz Pulse/Function Generator, is a precision source of sine, triangle, square and pulse waveforms plus dc voltage. All waveforms are variable from 0.002 Hz to 20 MHz and can be externally modulated. Outputs can be continuous or can be triggered or gated by external signal or front panel switch. Variable width and delay, single or double pulses can be inverted or normal. Pulse and square wave fixed baseline selectable may be varied from fixed baseline to 15 Vp-p (7.5 Vp-p into 50 Ω). An internal burst generator gates main generator and operates in continuous, triggered and gated modes. Amplitude of the waveforms is variable from 30 Vp-p (15 Vp-p into 50 Ω) down to 1.5 mVp-p. DC reference of the waveform can be offset positively or negatively. Maximum 150 mA peak current can be continuously varied over an 80 dB range. A sync output provides a TTL level into 50 Ω .

1.2 SPECIFICATIONS

1.2.1 Main Generator

Waveforms

Selectable sine \sim , triangle \wedge , square \square , pulses, double pulses and dc.

Symmetry

With SYM on, waveforms may be varied to produce sawtooth \nearrow and variable duty cycle pulse \square from 1:19 to 19:1.

NOTE

SYMMETRY and VERNIER controls affect frequency calibration. Maximum possible asymmetry is a function of frequency setting.

When SYM control is used, indicated frequency is divided by approximately 10.

Operational Modes

Function

Continuous: Generator oscillates continuously at selected frequency.

Triggered: Generator is quiescent until triggered by external signal or manual trigger, then generates one cycle at selected frequency.

Gated: As triggered mode, except generator oscillates for the duration of gate signal plus time to complete the last cycle.

Burst

Internal burst generator gates main generator and operates in continuous, triggered and gated modes.

Burst Rate: 1 Hz to 5 MHz in 7 ranges.

Burst Width: 20 ns to 100 ms in 7 ranges.

Frequency Range

0.002 Hz to 20 MHz in 9 overlapping decade ranges with approximately 1% of full scale vernier.

Function Output

\sim , \wedge , \square and pulse selectable and variable to 30 Vp-p (15 Vp-p into 50 Ω). Pulse and \square fixed baseline selectable (\nearrow , \searrow , \square) and can be inverted. \square , \nearrow can be varied from fixed baseline to 15 Vp-p (7.5 Vp-p into 50 Ω). All waveforms and dc may be attenuated in 10 db steps to 70 dB with 10 dB vernier for overall attenuation of 80 dB. 50 Ω source impedance.

DC Output and DC Offset

Selectable thru function output BNC. Controlled by front panel control with separate on-off switch. Adjustable between ± 15 Vdc (± 7.5 Vdc into 50 Ω) with signal peak plus offset limit to ± 15 Vdc (± 7.5 Vdc into 50 Ω). DC offset and output waveform attenuated proportionately by 0 to 70 dB output attenuator.

Sync Output

A TTL level square wave synchronized to the main generator. Duty cycle varies with symmetry control. 50 Ω source impedance.

Pulse/Square Output

A TTL level pulse or square wave whose transitions are simultaneous with function output (square and pulse only). 50 Ω source impedance.

VCG—Voltage Controlled Generator

Up to 1000:1 frequency change with external 0 to $\pm 5V$ signal. Upper frequency limited to maximum of selected range.

Slew Rate: 2% of range per μs .

Linearity: $\pm 0.5\%$ thru $\times 100K$ range. $\pm 5\%$ on $\times 1M$ and $\times 10M$ range.

Impedance: 10 k Ω .

Trigger (and Gate) Input

Input Range: 1 Vp-p to $\pm 10V$.

Trigger Level Adj: $-5V$ to $+5V$.

Impedance: 1.5 k Ω shunted by 1.5 pF.

Pulse Width: 25 ns minimum.

Repetition Rate:	Input	Max Rep Rate
	$\pm 1V$	1 MHz
	$\pm 2.5V$	10 MHz

1.2.2 Pulse Generator**Pulse Modes**

Normal Pulse: Adjustable width pulse in phase with pulse sync output. Repetition rate is set by frequency of main generator.

Pulse Delay: Pulse delayed with respect to pulse sync output. Pulse delay and pulse width adjustable.

Double Pulse: Two pulses for every period. Time between pulses and pulse width adjustable.

Sync Delay: Pulse sync output delayed with respect to pulse output. Delay is adjustable.

NOTE

The preceding Pulse Modes operate as defined when the Function Mode is Continuous, Triggered or Gated. However, Pulse Modes are not applicable in Burst Mode.

Pulse Period Range

50 ns to 500 sec in 9 decade ranges.

Pulse Width

20 ns to 100 ms in 7 ranges.

Pulse or Sync Delay

0 ns to 100 ms in 7 ranges.

Duty Cycle

Up to: 75% for pulse widths > 100 ns; 50% for pulse widths of 20 to 100 ns.

Pulse/Burst Sync Output

A TTL level pulse when terminated with 50 Ω . Reference for pulses and bursts at function output BNC and TTL pulse BNC.

In pulse function mode (normal pulse) and burst mode, sync output is coincident with leading edge of pulse/burst output and has width of 20 to 60% of maximum selected pulse/burst width, except on the 20 to 100 ns range which will have a sync pulse width between 10 and 30 ns.

NOTE

Also see Pulse Modes.

1.2.3 Frequency Precision**Dial Accuracy**

$\pm 3\%$ of full scale from $\times 0.1$ Hz to $\times 1$ MHz.
 $\pm 5\%$ of full scale on $\times 10M$ range.

1.2.4 Amplitude Precision**Amplitude Change with Frequency**

Sine variation with frequency:
 $< \pm 0.2$ dB on all ranges thru $\times 100K$.
 $< \pm 0.5$ dB on $\times 1M$ range.
 $< \pm 1.0$ dB on $\times 10M$ range.

Step Attenuator Accuracy

± 0.3 dB with 10, 20 and 40 dB.
 ± 0.6 dB with 30, 50 and 60 dB.
 ± 0.9 dB with 70 dB setting.

1.2.5 Waveform Characteristics**Sine Distortion**

$< 0.5\%$ on $\times 100$, $\times 1K$ and $\times 10K$.
 $< 1.0\%$ on $\times 0.1$ to $\times 100$ ranges.

All harmonics 30 dB below fundamental on $\times 100K$, $\times 1M$ range, and 25 dB below on $\times 10M$ range.

Square Wave and Pulse

Rise/Fall Time at Function Output BNC:
 < 15 ns (10% to 90%).

Total Aberrations:
 $\pm 5\%$ of full amplitude.

Time Symmetry

Square wave variation from 0.1 to 2 on dial:
< $\pm 1\%$ to 200 kHz.
< $\pm 10\%$ to 20 MHz.

Triangle Linearity

> 99% for 0.002 Hz to 200 kHz.

1.2.6 General

Stability

Main generator amplitude, frequency and dc offset.
After 2 hour warm-up:
 $\pm 0.05\%$ for 10 minutes.
 $\pm 0.25\%$ for 24 hours.

Environmental

Specifications apply at $25^{\circ}\text{C} \pm 5^{\circ}$. Instrument operates 0°C to $+50^{\circ}$.

Dimensions

28.6 cm (11 ¼ in.) wide; 13.3 cm (5 ¼ in.) high; 28.6 cm (11 ¼ in.) deep.

Weight

4.6 kg (10 lb) net; 6.4 kg (14 lb) shipping.

Power

100/120/220/240V (+ 5%, - 10%), 48 Hz to 66 Hz,
 ≤ 95 VA.

NOTE

All specifications apply from 0.1 to 2.0 on frequency dial, when FUNC OUT amplitude is maximum and 50 Ω terminated, and with SYM control OFF.

SECTION 2

INITIAL PREPARATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground path can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a $\frac{3}{8}$ amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

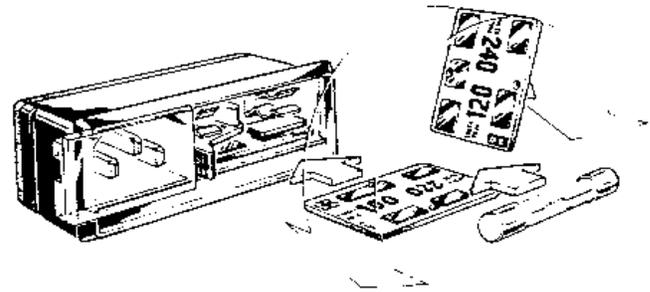


Figure 2-1. Voltage Selector and Fuse

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.
2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.
3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

Card Position	Input Vac	Fuse
100	90 to 105	$\frac{3}{4}$ amp
120	108 to 126	$\frac{3}{4}$ amp
220	198 to 231	$\frac{3}{8}$ amp
240	216 to 252	$\frac{3}{8}$ amp

2.2.2 Signal Connections

Use RG58U 50 Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

2.3 ELECTRICAL ACCEPTANCE CHECKOUT

This checkout procedure verifies the generator operation. If a malfunction is found, refer to the Warranty in the front of this manual. A dual trace, 150 MHz bandwidth oscilloscope with X 10 time base magnification, a 50 Ω load, a coaxial tee and three 50 Ω cables are required to perform this checkout.

Set up as in figure 2-2 and preset the generator front panel controls as follows. Perform the steps in table 2-1.

Control	Position
Dial	1.0
FREQ MULT	1K
VERNIER/SYM	FREQ CAL (cw)
SYM	Off(extended)
MODE	CONT (FUNC)
TRIG LEVEL	10 o'clock
FUNCTION	~
DC OFFSET (On/Off)	OFF(Extended)
DC OFFSET (Variable Control)	ccw
OUTPUT ATTN 40, 20, 10	All Extended
AMPLITUDE	MAX (cw)
PULSE DELAY (Range)	10 μ s to 100 μ s
PULSE DELAY (Vernier)	ccw
PULSE (Pushbuttons)	NORM (Pressed)
PULSE WIDTH (Range)	10 μ s to 100 μ s
PULSE WIDTH (Vernier)	cw

PULSE/SQUARE OUTPUT
 INV Normal (Extended)
 POWER ON

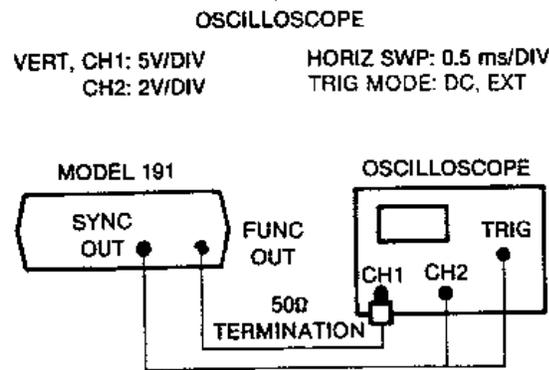


Figure 2-2. Initial Checkout Setup

Table 2-1. Checkout Procedure

Step	Control	Position/Operation	Observation
1	Oscilloscope	Trig level and slope, both positive.	CH2: Square wave that begins on positive going edge. CH1: 15 Vp-p sine wave.
2	Dial and VERNIER/SYM	Rotate dial full cw, vernier full ccw. Then the opposite. Return dial to 1.0, vernier to CAL.	CH2: Square wave remains in sync for all dial positions. Range is greater than from 2 Hz to 2000 Hz (1000:1).
3	FREQ MULT	Rotate to all positions. Return to 1K position.	Frequency is 1 x each range position.
4	AMPLITUDE	Set to 6 Vp-p on scope.	CH1: Amplitude decreases to approximately 6 Vp-p.
5	DC OFFSET	Depress DC OFFSET switch, then rotate DC OFFSET Control CW. Release DC OFFSET to extended (off) position at completion of this step.	Full CCW gives negative offset. Clipping occurs when the offset plus waveform peak amplitude exceeds approximately $\pm 7.5V$ into 50 Ω . Initially the negative peak is clipped, but as the DC offset is rotated cw the clipping of the negative peak disappears and eventually the positive peak begins to clip.
6	AMPLITUDE	Rotate cw.	Waveform returns to 15 Vp-p.
7	OUTPUT ATTN 10, 20, 40	Depress buttons in various combinations. Then release all buttons.	Output level varies from 15 Vp-p (0 dB) to 4.7 mV (70 dB).
8	FUNCTION	Rotate ccw. Select DC ~, ~, ~. Reset to ~.	Observe 0 Vdc level; ~, ~ and ~ are 15 Vp-p. Note phase relationships; ~ in phase with ~ and ~.

Table 2-1. Checkout Procedure (Cont)

Step	Control	Position/Operation	Observation
9	SYM, VERNIER/SYM.	Depress SYM switch and rotate VERNIER/SYM control ccw. Extend SYM, return VERNIER/SYM to CAL.	Frequency decreases to approximately 100 Hz. CCW of the 12 o'clock position gives 1:19; CW gives 19:1 (a skewed sinewave and variable duty cycle pulses can be observed for \sim and \square .)
10	MODE and FUNCTION	Select GATE. Select \sim , \square , \square . Return to \sim .	A dc level near zero volts (except \square function; quiescent level is at negative peak value).
11	MANUAL TRIGGER	Press, hold and release. Return to FUNC CONT.	A burst of \sim for the period the MAN TRIG is depressed.

Set MODE to CONT (FUNC). (All other controls will be as for initial setup.) Setup oscilloscope and Model 191 as shown in figure 2-3. Display both channels.

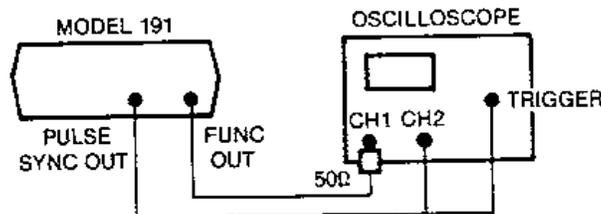


Figure 2-3. Pulse Checkout Setup

12	FUNCTION	PULSE	Pulse
13	AMPLITUDE	Vary, then return cw.	Upper and lower levels vary from 0.5V to 15 Vp-p.
14	PULSE/SQUARE OUTPUT	Depress INV, then release INV.	180° phase inversion of pulse relative to PULSE SYNC OUT.
15		Depress \square .	Positive offset pulse + 7.5V.
16	AMPLITUDE	Vary, then return to full cw.	Upper level varies, lower level remains fixed. Full variation from 0.5V to + 7.5 Vp-p.
17	PULSE/SQUARE OUTPUT	Depress \square .	Negative offset pulse - 7.5 Vp-p.
18	AMPLITUDE	Vary, then return to full cw. Return to \square .	Low level varies, upper level remains fixed. Full variation from 0.5V to - 7.5 Vp-p.

The next 2 steps demonstrate maximum and minimum pulse width range.

Table 2-1. Checkout Procedure (Cont)

Step	Control	Position/Operation	Observation
19	Dial FREQ MULT PULSE WIDTH Scope PULSE WIDTH VERNIER	2.0 1 10 ms - 100 ms. 20 ms/div. Rotate ccw, cw.	Minimum PULSE WIDTH at ccw; maximum PULSE WIDTH at cw.
20	Dial FREQ MULT PULSE WIDTH Scope PULSE WIDTH VERNIER	.2 10M 20 ns - 100 ns. 0.05 μ s/div. Rotate ccw, cw.	Minimum PULSE WIDTH at ccw; maximum PULSE WIDTH at cw.
<i>The next steps demonstrate maximum and minimum pulse delay range.</i>			
21	PULSE PULSE DELAY Scope PULSE DELAY VERNIER	Depress PULSE DLY. 0 ns - 100 ns. 0.05 μ s/div. Rotate ccw, cw.	Minimum PULSE DELAY from PULSE SYNC at ccw; maximum PULSE DELAY from PULSE SYNC at cw.
22	Dial FREQ MULT PULSE WIDTH PULSE DELAY Scope PULSE DELAY VERNIER	2.0 1 10 ms - 100 ms. 10 ms - 100 ms. 20 ms/div. Rotate ccw, cw.	Minimum PULSE DELAY from PULSE SYNC at ccw; maximum PULSE DELAY from PULSE SYNC at cw.
<i>The next step demonstrates double pulse.</i>			
23	Dial FREQ MULT PULSE PULSE WIDTH PULSE DELAY Scope PULSE WIDTH VERNIER PULSE DELAY VERNIER	0.5 10K DBL pulse 10 μ s - 100 μ s 10 μ s - 100 μ s 0.05 ms/div. ccw Rotate cw, ccw	Double Pulse — maximum delay of second pulse from first pulse at cw. Second pulse merges with first pulse at ccw.
<i>The next step demonstrates sync delay.</i>			

Table 2-1. Checkout Procedure (Continued)

Step	Control	Position/Operation	Observation
24	PULSE Scope PULSE DELAY VERNIER	Depress SYNC DLY Trigger: INT CHANNEL 1 (FUNC OUT). Then return to EXT. Rotate ccw, cw.	Minimum SYNC DELAY from PULSE at ccw. Maximum SYNC DELAY from PULSE at cw.

The next step demonstrates burst control.

25	MODE FUNCTION Dial FREQ MULT BURST RATE BURST RATE VERNIER BURST WIDTH Scope BURST WIDTH VERNIER	BURST CONT ~ 2.0 10K 100 - 1K 12 o'clock. 100 μ s - 1 ms. 0.5 ms/div. Rotate cw, ccw.	Number of cycles in burst increases (cw) and decreases (ccw).
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Set up trigger source as shown in figure 2-4. Set trigger source for 200 Hz triangle 10 Vp-p signal. Set scope for one cycle of triggering waveform; display both channels. Setup Model 191 controls for initial setup except set MODE to FUNC GATE.

26	TRIG LEVEL	Rotate throughout its range. Return to 10 o'clock.	The number of waveform cycles in each gated "burst" varies with the trigger level. Notice relationships between Channels 1 and 2 waveforms as the TRIGGER LEVEL is rotated.
27	MODE	Select FUNC TRIG	A single triggered ~ recurring at the 200 Hz trigger rate.
28	Dial FREQ MULT MODE BURST RATE BURST RATE VERNIER BURST WIDTH BURST WIDTH VERNIER MODE	2.0 1M BURST GATED 1K - 10K 12 o'clock 100 μ s - 1 ms 12 o'clock BURST TRIG	CW reduces number of bursts per gate. CCW increases number of bursts per gate. A single triggered burst at 200 Hz trigger rate.

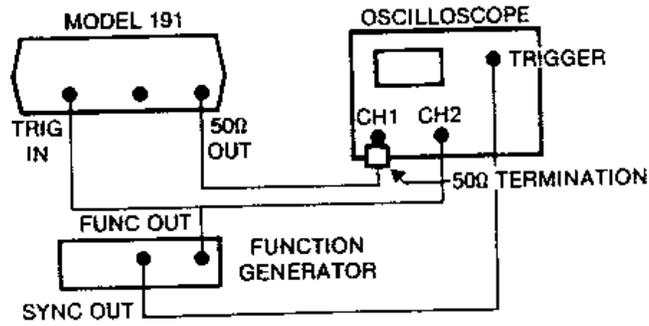


Figure 2-4. Trigger Checkout Setup

SECTION 3

OPERATION

3.1 CONTROLS AND CONNECTORS

The generator front panel controls and connectors are shown in figure 3-1 and keyed to the following descriptions.

- 1 **Frequency Dial** — Settings under the dial index mark summed with VCG IN 19 and multiplied by FREQ MULT 17 determine the output signal frequency.
- 2 **PULSE DELAY/BURST RATE Selector** — Outer coax knob selects one of seven ranges. An inner coax knob, VERNIER, controls the delay or rate within each range.
- 3 **SYM Pushbutton** — When depressed, allows the waveform symmetry to be varied from 19:1 to 1:19 by the VERNIER/SYM control 17; (as a result the generator frequency is divided by 10).

In pulse function, these controls set the delay of the pulse at FUNC OUT 10 and PULSE/SQUARE OUT 12 (PULSE DLY 4 depressed), or the delay of the pulse at PULSE SYNC OUT 16 relative to FUNCTION OUT 10 and PULSE/SQUARE OUT 12 (SYNC DLY 4 depressed). Pulse delay and sync delay are variable between 0ns to 100 ns.

In burst modes, the BURST RATE and VERNIER controls set the burst repetition rate. Repetition varies between 1 Hz and 5 MHz.

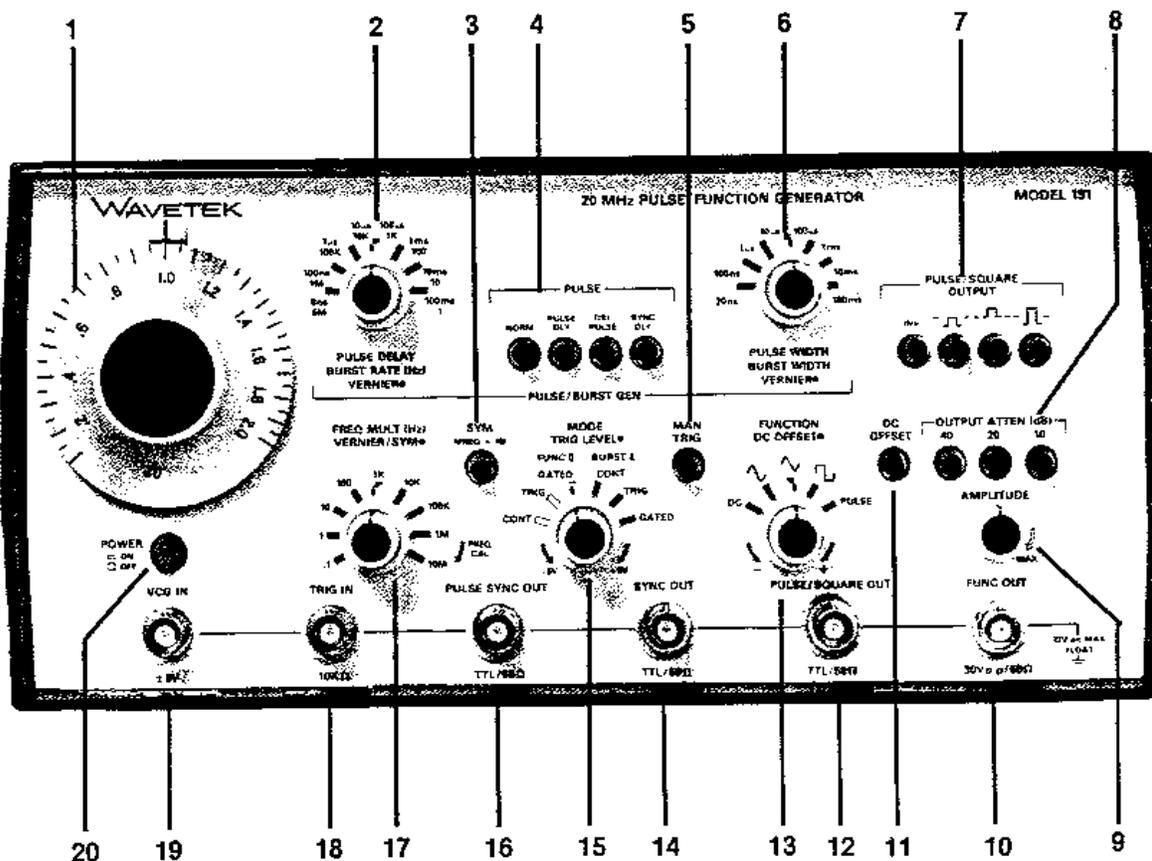


Figure 3-1. Controls and Connectors

When extended, the switch allows the generator to produce normal (50% duty cycle) waveforms.

- 4 PULSE Pushbuttons** — Four mutually exclusive switches that select either normal pulse, pulse delay, double pulse or sync delay when FUNCTION switch **13** is set to PULSE.
- NORM** — Selects a pulse at FUNC OUT **10** and PULSE/SQUARE OUT **12** in phase with PULSE SYNC OUT **16**. PULSE WIDTH **6** controls the width of the normal pulse, and the frequency dial **1** and FREQ MULT **17** set the pulse repetition rate.
- PULSE DLY** — Selects a pulse that is delayed relative to PULSE SYNC OUT **16**. PULSE DELAY **2** controls the delay of the pulse, the frequency dial **1** and FREQ MULT **17** control pulse repetition rate, and PULSE WIDTH **6** sets the width of each pulse.
- DBL PULSE** — Selects two pulses for each pulse period. In double pulse, PULSE DELAY **2** sets the start of the second pulse relative to the first. The frequency dial **1** and FREQ MULT **17** control the repetition rate for each pulse pair. PULSE WIDTH **6** controls pulse width of both pulses.
- SYNC DLY** — Selects a variable delay sync pulse at the PULSE SYNC OUT **16** relative to FUNC OUT **10** and PULSE/SQUARE OUT **12**. PULSE DELAY **2** controls the delay of the pulse sync. Frequency dial **1** and FREQ MULT **17** set repetition rate of the pulse.
- 5 MAN TRIG Pushbutton** — Triggers or gates the output signals when generator mode is TRIG or GATED **15**. In function trigger mode, one waveform cycle is output when the button is pushed; in burst trigger mode, one burst. In function gated mode, waveform cycles are continuously output as long as the button is held in; in burst gated mode, burst are continuously output.
- 6 PULSE WIDTH/BURST WIDTH** — Outer coax knob selects one of seven decade ranges. An inner coax knob, VERNIER, controls the width within each range. In pulse function PULSE WIDTH sets the width of the pulse at FUNC OUT **10** and PULSE/SQUARE OUT **12**.

In burst modes, BURST WIDTH sets the burst duration at FUNC OUT **10** and, in \square function only, at PULSE/SQUARE OUT **12**.

- 7 PULSE/SQUARE OUTPUT** — Selects the pulse amplitude symmetry relative to the baseline (ref: figure 3-2). With DC OFFSET **11** off, the baseline is 0 volts. With DC OFFSET on, the baseline is varied by the DC OFFSET control **13**.
- \square selects a pulse that maintains amplitude symmetry about its centerline. AMPLITUDE **9** adjust the peak-to-peak level of the pulse.
- \square selects the positive pulse. AMPLITUDE **9** adjust the positive peak while the negative peak remains a fixed baseline.
- \square selects the negative pulse. AMPLITUDE control **9** adjusts the negative peak while the positive peak remains a fixed baseline.
- INV pushbutton — selects normal or inverted pulse output. An inverted pulse is a reversal of the active and inactive levels of the pulse. The net result for a square pulse inversion would be a 180° phase shift with respect to the PULSE SYNC OUT **16**.
- 8 OUTPUT ATTEN Pushbuttons** — Select the attenuation range of the FUNC OUT **10** signal. The AMPLITUDE control **9** allows continuous waveform level variations within each attenuator range. Each of the three buttons may be used individually for 40, 20 or 10 dB steps of attenuation, or pressed in combinations for up to 70 dB of attenuation. The attenuator attenuates both the waveform and dc offset.
- 9 AMPLITUDE Control** — Continuously varies the waveform amplitude within each OUTPUT ATTEN **8** range. CCW rotation reduces waveform amplitudes at FUNC OUT **10** by greater than 10 dB. DC and dc offset voltages are not affected by this control.
- 10 FUNC OUT Connector** — This BNC is the waveform (or dc) output of the generator. Maximum output is 30 Vp-p (15 Vp-p into 50 Ω). Source impedance is 50 Ω .
- 11 DC OFFSET Pushbutton** — Depressed button activates the dc offset (ref: **13**). Extended button ensures zero dc offset.

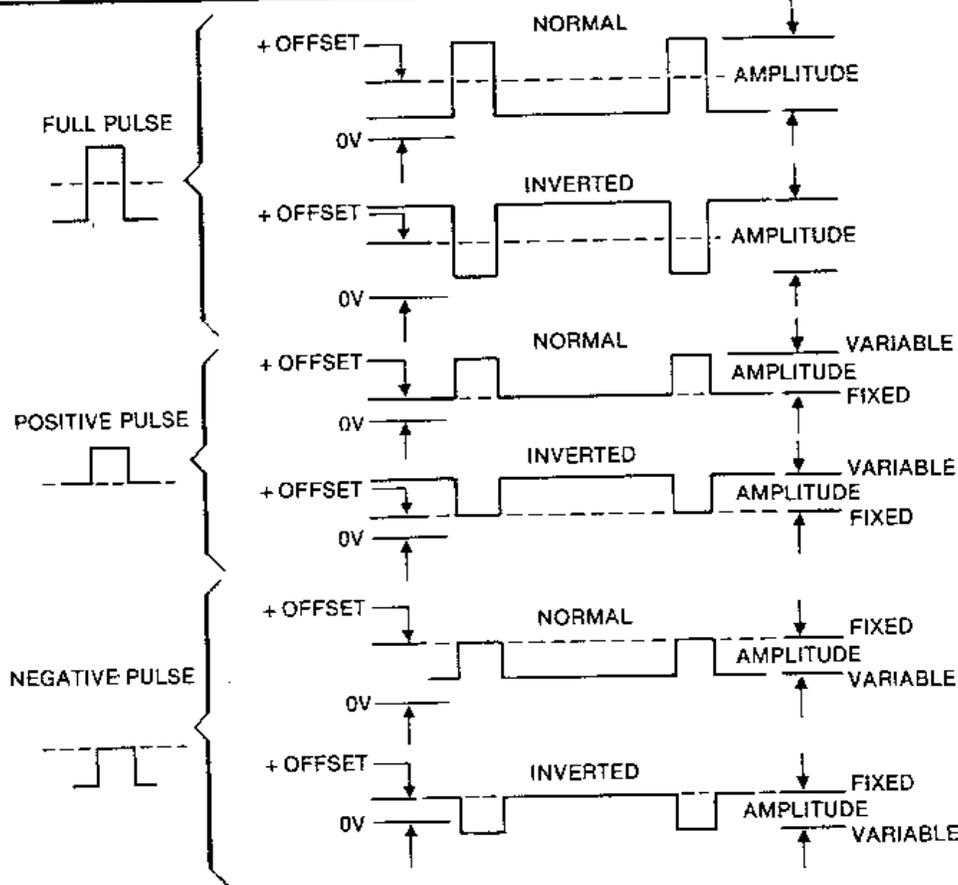


Figure 3-2. PULSE/SQUARE OUTPUT Amplitude/Offset Relationship

12 PULSE/SQUARE OUT Connector — BNC output is a TTL level into 50Ω . Output is simultaneous and exclusive with FUNC OUT 10 square wave or pulse output. Source impedance is 50Ω .

13 FUNCTION Selector — Outer coaxial knob selects one of four waveforms (sine, triangle, square, pulse) or dc.

DC OFFSET Control — Inner coaxial knob offsets the FUNC OUT 10 output waveform vertically from its normal position and when FUNCTION (outer coaxial knob 13) is in the DC position, controls polarity and voltage of dc output. DC output range is 0 ± 10 Vdc (± 5 Vdc into 50Ω). DC OFFSET switch 11 must be depressed to enable this DC OFFSET Control. Extending the DC OFFSET switch ensures zero volt offset. DC offset and waveform are attenuated by the OUTPUT ATTEN control 8 but dc offset is not attenuated by the AMPLITUDE control 9. Waveform peak voltage plus dc offset is limited to ± 15 Vdc (± 7.5 Vdc into 50Ω). See figure 3-3.

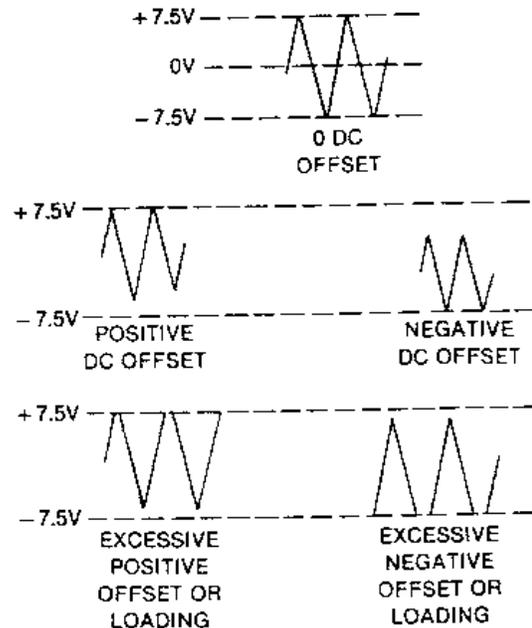


Figure 3-3. DC OFFSET Control

- 14 SYNC OUT Connector** — The sync signal from this BNC is a TTL level into 50Ω synchronous with FUNC OUT 10 signal. Duty cycle varies with waveform symmetry. Source impedance is 50Ω.
- 15 MODE Control** — This outer coax knob selects one of the six operating modes. Three of the modes are burst generator modes (switch detents are solid black) and three are function generator modes (switch detents are white). Figure 3-8 illustrates the output in each of these modes.

FUNC Modes

CONT — Continuous output at FUNC OUT 10 and SYNC OUT 14 connectors.

TRIG — A dc level output at FUNC OUT 10 until the generator is triggered by the MAN TRIG 5 or with a signal at the TRIG IN connector 18. When triggered the generator output is one cycle of waveform followed by a dc level.

GATED — As for TRIG except the output is continuous for the duration of the manual or external trigger signal. The last waveform cycle started is always completed.

BURST Modes

CONT — Continuous burst is a series of bursts from FUNC OUT 10 at a continuous repetition rate. BURST RATE 2 sets the repetition rate of each burst. Frequency dial 1 and FREQ MULT 17 determine the frequency of waveform cycles in each burst. BURST WIDTH 6 sets the number of cycles within each burst.

TRIG — A trigger (manual 5 or external 18) initiates a burst of cycles from FUNC OUT 10. The trigger rate determines the burst repetition rate. Frequency dial 1 and FREQ MULT 17 determine the frequency of waveform cycles in each burst. BURST WIDTH 6 sets the number of cycles within each burst.

GATED — When triggered (external 18 or manual 5), FUNC OUT 10 produces a series of bursts for the active period of the trigger signal. Frequency dial 1 and FREQ MULT 17 sets the frequency of the cycles in the burst. BURST RATE 2 controls the repetition rate between bursts and BURST WIDTH 6 sets the number of cycles within each burst.

TRIG LEVEL Control — This inner coax knob is a continuously variable adjustment of the trigger circuitry firing point. When full ccw, a positive going signal at approximately +5V is required for triggering (see figure 3-4). In the full cw position, a positive going signal at approximately -5V or more positive voltage is required for triggering. In the GATED modes, the generator will run continuously when the control is cw of 12 o'clock.

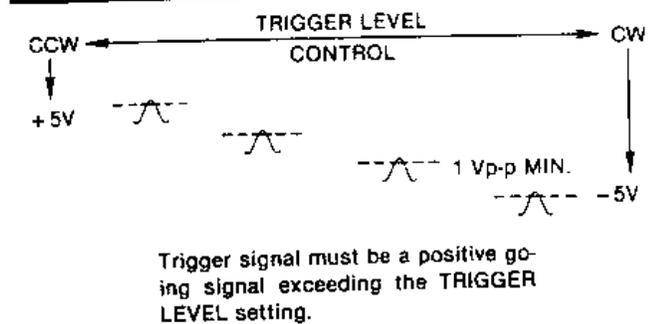


Figure 3-4. Minimum Trigger Signal

- 16 PULSE SYNC OUT Connector** — With normal pulse function or burst mode selected, this BNC output supplies a TTL level pulse that is coincident with the leading edge of the pulse or burst at FUNC OUT 10. Sync pulse width is 20 to 60% of minimum selected pulse/burst width except on the 20 ns to 100 ns range, which will have a sync pulse width between 10 and 30 ns. Source impedance is 50Ω.

In sync delay (ref: 4), PULSE DELAY 2 controls the delay of PULSE SYNC OUT relative to FUNC OUT 10 and PULSE/SQUARE OUT 12.

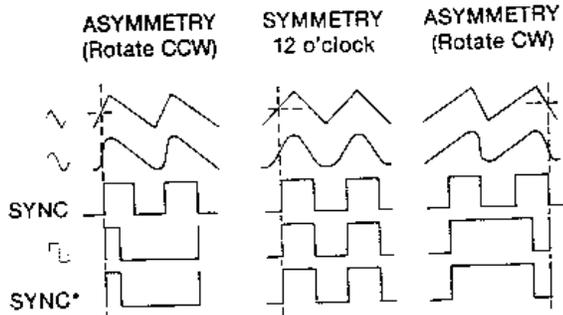
NOTE

PULSE SYNC OUT is the correct sync signal for the pulse waveform and the burst mode.

- 17 FREQ MULT Control** — Outer coax knob selects one of nine frequency multipliers for dial 1 setting.

VERNIER/SYM Control — When the SYM switch 3 is off (extended) this inner coax knob is a fine adjustment of the frequency dial 1 setting. CCW rotation decreases the frequency by approximately 1%. When in cw position (FREQ CAL), the settings on the dial will be accurate. When SYM switch is on (depressed) this control

varies the symmetry of the waveforms (normally 50% duty cycle). Symmetry range is 19:1 to 1:19 (half cycle to half cycle ratio). When SYM is used, the main generator frequency is divided by 10. Extending SYM switch ensures 1:1 (50%) symmetry. See figure 3-5.



* SYNC DUTY CYCLE VARIES SAME AS FUNC OUT SIGNAL WHEN SQUARE FUNCTION (\square) IS SELECTED.

Figure 3-5. Effect of Symmetry Control

- 18 TRIG IN Connector — BNC receives the external trigger and gate signals. These signals are applied to the trigger and gate circuit when the MODE switch 15 is in the TRIG or GATED positions. Refer to Section 1 Trigger (and Gate) Input specifications, for trigger signal requirements. The TRIG LEVEL control 15 selectively accepts trigger and gate signals for the trigger and gate circuits.
- 19 VCG IN Connector — BNC accepts ac or dc voltages to proportionately control frequency within the range determined by the FREQ MULT 17. Positive voltages increase the frequency set by the dial 1; negative voltages decrease the frequency. The VCG IN will not drive the generator frequency beyond the normal limits of a range. Input impedance is 10 k Ω .
- 20 POWER Pushbutton — Depressed is power on, extended is power off.

3.2 OPERATION

Perform the initial checkout in Section 2 for the feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.1.

3.2.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. For example, the proper termination of the 50 Ω OUT connector is shown in figure 3-6. Placing the 50 ohm terminator, or 50 ohm resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

The input and output impedances of the generator connectors are listed below.

Connector	Impedance
FUNC OUT	50 Ω
SYNC OUT (TTL)	50 Ω
PULSE/SQUARE OUT (TTL)	50 Ω
PULSE SYNC OUT (TTL)	50 Ω
TRIG IN	1.5k Ω
VCG IN	10k Ω

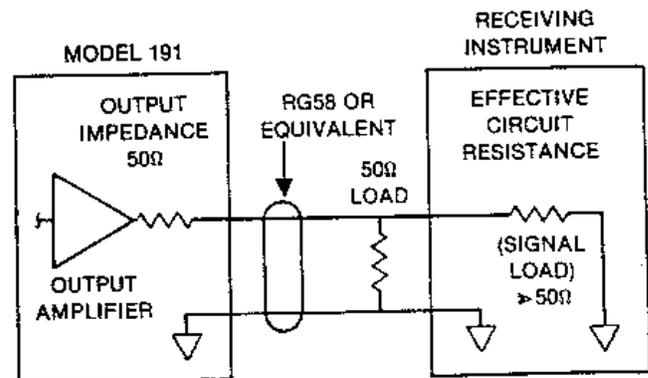


Figure 3-6. Signal Termination

3.2.2 Manual Function Generator Operation

The following steps demonstrate manual control of the function generator. (Bold numbers are keys to figure 3-1.)

Step	Control/Connector	Setting
1	FUNC OUT	10 Connect circuit to output (refer to paragraph 3.2.1).

- 2 MODE 15 Select CONT (FUNC).
- 3 SYM 3 Extended.
- 4 FREQ MULT 17 Set to desired range of frequency.
- 5 Frequency Dial 1 Set to desired frequency within the range.
- 6 FUNCTION 13 Set to desired waveform.
- 7 DC OFFSET 11, 13 Set as desired. Limit offset to prevent waveform clipping (see figure 3-3).
- 8 OUTPUT ATTEN 8 Select for desired attenuator range.
- 9 AMPLITUDE 9 Select for desired waveform amplitude.

NOTE

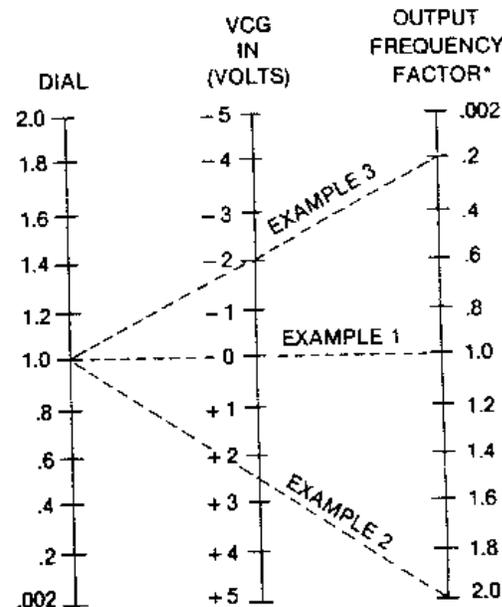
Nonlinear operation may result when the VCG input voltage is excessive; that is, when the attempted generator frequency exceeds the range limits. The upper limit is 2 times the multiplier setting, and the lower limit is 1/1000th of the upper limit.

3.2.3 Voltage Controlled Function Generator Operation

Operation as a voltage controlled function generator (VCG) is as for a manually controlled function generator, only the frequency within particular ranges is additionally controlled by an external voltage ($\pm 5V$ excursions) injected at the VCG IN connector. Perform the steps given in paragraph 3.2.2, only set the frequency dial to determine a reference from which the frequency is to be voltage controlled.

1. For frequency control with positive dc inputs at VCG IN, set the dial for a lower frequency limit.
2. For frequency control with negative dc inputs at VCG IN, set the dial for an upper frequency limit.
3. For modulation with an ac input at VCG IN, set the dial at the desired center frequency. Do not exceed the maximum dial range of the selected frequency range.

Figure 3-7 is a nomograph with examples of dial and voltage effects. Example 1 shows that with 0V VCG input, frequency is determined by the main dial setting, 1.0 in this example. Example 2 shows that with a positive VCG input, output frequency is increased. Example 3 shows that with a negative VCG input, output frequency is decreased. (Note that the Output Frequency Factor column value must be multiplied by a frequency range multiplier to give the actual output frequency.)



*Must be multiplied by FREQ MULT switch setting

Figure 3-7. VCG Voltage-to-Frequency Nomograph

The up to 1000:1 VCG sweep of the generator frequencies available in each range results from a 5V excursion at the VCG IN connector. With the frequency dial set to 2.0, excursions between $-5V$ and $0V$ at VCG IN provide the up to 1000:1 sweep within the set frequency range.

3.2.4 Waveforms

See figure 3-8 for definition of controllable waveform characteristics.

3.2.5 Pulse Generator Operation

Operation as a pulse generator is similar to the manual and VCG controlled generator except a single pulse, double pulse or square wave may be selected.

The following steps describe the pulse operation setup.

Step	Control/Connector	Setting
1	MODE	15 CONT (FUNC)
2	Frequency dial	1 Select pulse repetition rate.
3	FREQUENCY MULTIPLIER	17 Select pulse repetition rate.
4	FUNCTION	13 Select PULSE.
5	PULSE/SQUARE OUTPUT	12 Select desired pulse format.
6	PULSE	4 Select desired pulse mode.
7	PULSE WIDTH	6 Select desired pulse width range and approximate portion of range.
8	PULSE DELAY	2 Select desired pulse delay range and approximate portion of range. (Applicable only if PULSE DLY was selected in step 6.)
9	DC OFFSET	11, 13 Set as desired. Limit pulse amplitude as necessary to prevent clipping (see figure 3-2).
10	AMPLITUDE	8, 9 Select desired amplitude.

3.2.6 Burst Generator Operation

In burst mode, the burst generator initiates a gate pulse, controlled by BURST RATE and BURST WIDTH, that gates the main generator. The main generator controls parameters of the signal being burst; i.e., frequency, function and amplitude. Refer to figure 3-8 for burst characteristics.

Set the main generator controls as for manual function generator operation (paragraph 3.2.2) and verify that the output signal is correct (other than not being in a "burst" mode). Then, set the burst controls as follows. (Bold numbers are keys to figure 3-1.)

Step	Control/Connector	Settings
1	MODE/BURST	15 Select either continuous, triggered or gated burst mode.
2	BURST RATE	2 Select desired burst repetition rate.
3	BURST WIDTH	6 Select desired number of cycles in burst length.

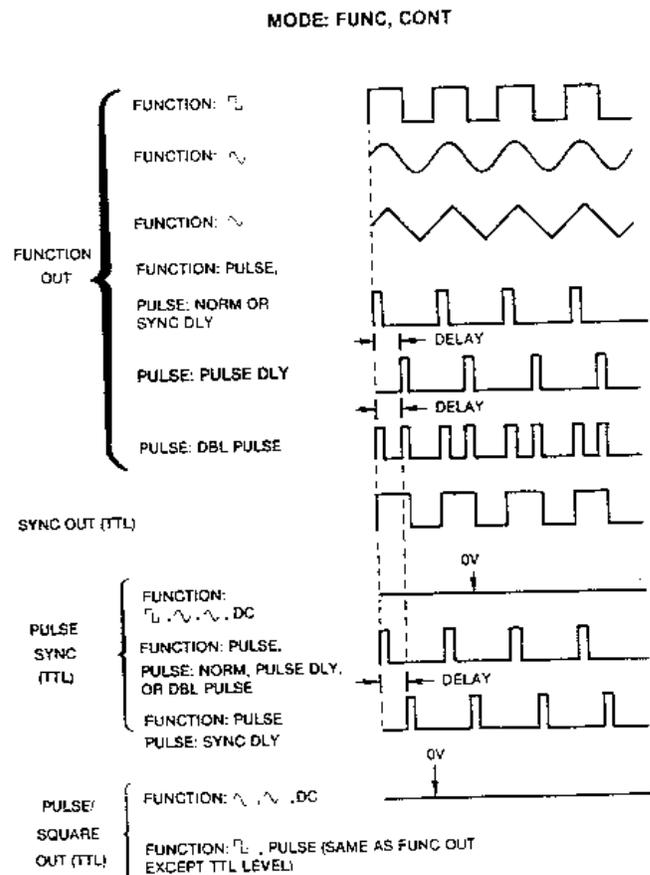


Figure 3-8. Waveform Characteristics

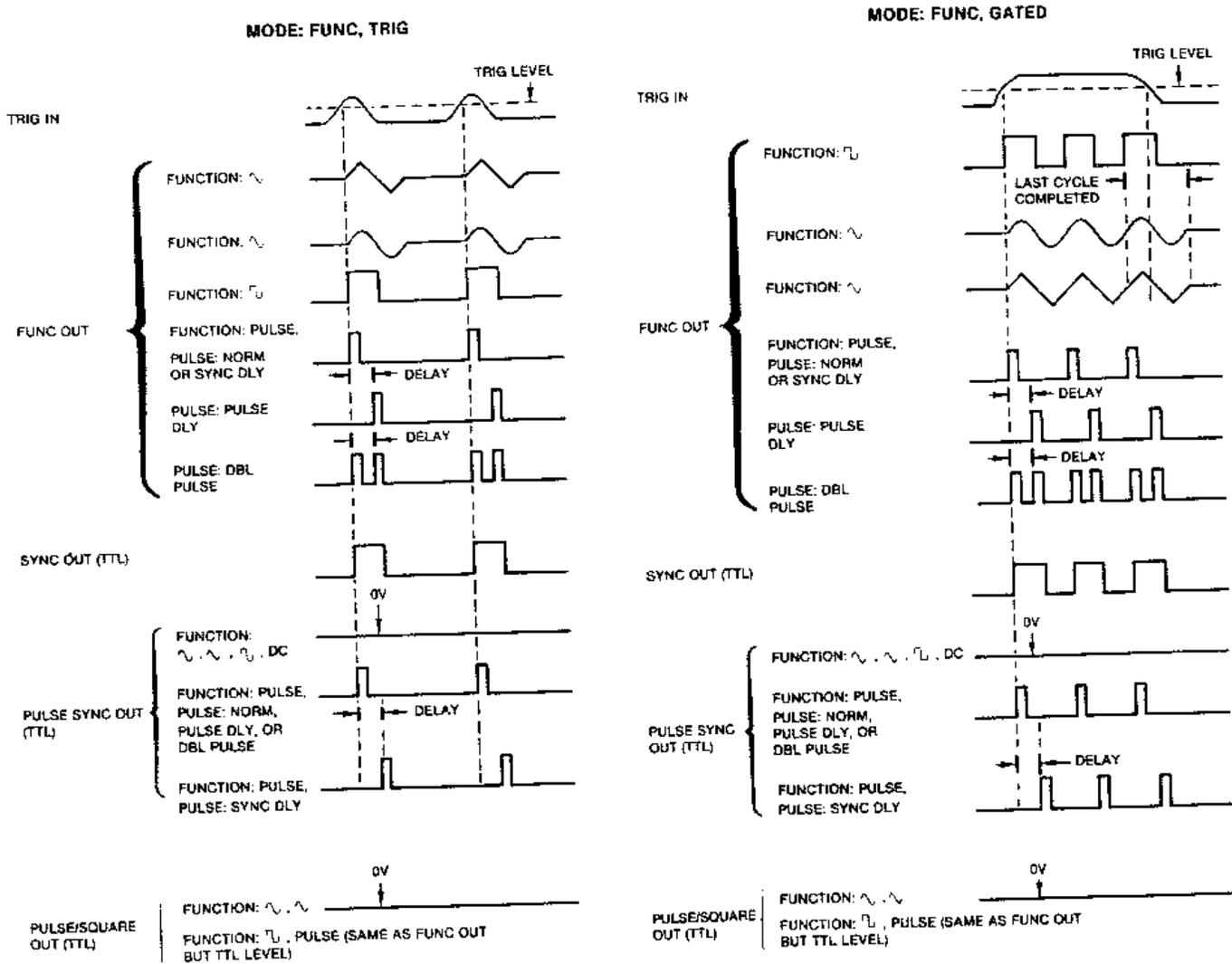


Figure 3-8. Waveform Characteristics (Cont)

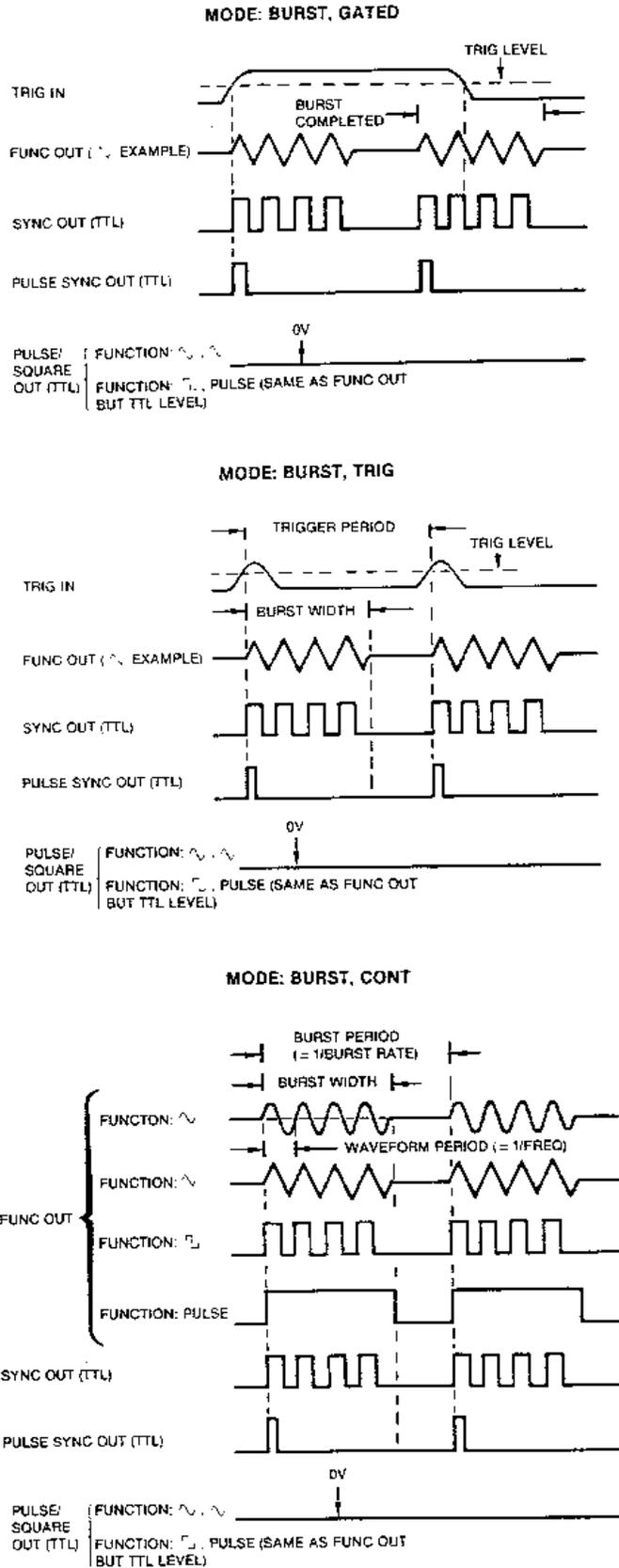


Figure 3-8. Waveform Characteristics (Cont)

4

SECTION 4

CIRCUIT DESCRIPTION

4.1 INTRODUCTION

This section describes the functions of the major circuits elements and their relationships to one another as shown in figures 4-1 and 4-2. First, the function generator portion is described, then the pulse circuit and, last, detailed circuit descriptions are given.

4.2 FUNCTION GENERATOR BLOCK DIAGRAM ANALYSIS

As shown in figure 4-1, the VCG (Voltage Controlled Generator) sums the voltage inputs from the frequency dial, VCG IN, and frequency vernier to provide a voltage control signal for the positive and negative current sources. The positive and negative current sources generate precision currents, linearly related to the output of the VCG summing amplifier, which pass through the current switch to the timing capacitors. Additional linear currents are generated for loop dc delay compensation and the trigger baseline compensation.

The current switch, controlled by the hysteresis output, causes either the positive current source or the negative current source to charge the timing capacitor selected by the frequency multiplier. When the positive current source is switched in, the charge on the timing capacitor will rise linearly producing the positive-going triangle slope. Likewise the negative current source produces the negative going triangle slope.

The triangle buffer amplifier is a unity gain amplifier whose output is fed to the hysteresis switch, sine converter and output circuits. The hysteresis switch operates as a "window" comparator with limit points set to the triangle peaks. When the positive going ramp reaches +1.0V, the hysteresis switch toggles to a low state causing the current switch to connect the negative current source. This causes the timing capacitor voltage to linearly ramp to -1.0V as the timing capacitor voltage reaches -1.0V, the hysteresis switch toggles to a high state, switching in the positive current source. The generator loop continues to oscillate producing simultaneous triangle and square waves, at a frequency determined by the frequency multiplier and the magnitude of the timing

current controlled by the sum of the dial setting, the VCG input, and the vernier.

Depressing the SYM button produces an unsymmetrical waveform and a division of the frequency by a factor of 10. The VERNIER/SYM control creates an imbalance in the current sources and therefore an imbalance in the waveform symmetry up to a ratio of 19:1. The result is variable duty cycle pulse, variable skewed sine wave and variable "sawtooth" triangle waves.

The dc loop delay compensation circuit is used on the two highest frequency ranges to compensate for loop delay. This circuit causes the hysteresis switch trip points to switch earlier in the cycle, and prevents the timing capacitors from charging beyond $\pm 1.0V$. The switch points are adjusted in proportion to the charging current, thus ensuring a constant amplitude as frequency is varied.

The capacitance multiplier is an active circuit which simulates capacitors up to 10,000 times larger than the timing capacitor, thus allowing very long charging times using physically small capacitors. This circuit is used in the four lowest frequency ranges.

The sine converter accepts a ± 1.0 volt triangle signal from the triangle buffer and converts it to a sine wave current. The output is fed via the function switch to the preamplifier.

The trigger circuit allows precise single or multiple (gated) cycles at the output in response to external trigger signals or manual trigger operation. The trigger circuit operates by holding the timing capacitor at 0 volts, via the loop stop signal, on the positive going triangle ramp, until a trigger signal occurs. In the TRIG mode a single cycle is produced for each trigger signal above the variable trigger level threshold. In the GATED mode continuous cycles are generated for the time period at which the external signal is above the trigger level threshold plus the time for completion of the last partial cycle. The \overline{RUN} signal causes the SYNC output to stay in the low state when the generator is quiescent. The TRGRST signal resets the trigger circuit and generator to the quiescent state on every generator cycle to arm it for the next trigger input. The trigger baseline compensation circuit holds

the generator output at zero volts (within specified limits) during the quiescent intervals at any position (value) of the frequency dial, FREQ MULT, VCG IN, or VERNIER.

The sync circuit accepts the square wave signal from the hysteresis switch and converts it to a true 50Ω TTL level output. In square wave function the sync is in phase with the output, but in triangle or sine functions, a zero crossing detector causes the sync output to be in phase with the zero crossing of the output waveform.

When square is selected by the function switch, the square shaper accepts the signal from the hysteresis switch and converts it to a clean, fast square wave current to drive the preamplifier. The function switch also sends a signal to the sync circuit, causing the sync output to be in phase with the positive going edge of the output squarewave. In sine, triangle or DC functions, the square shaper input and output are disabled so as not to interfere with the selected waveform.

The preamplifier is fed from both the function switch and the square shaper. The voltage output drives the output amplifier via the amplitude control.

The output amplifier accepts signals from the preamplifier by way of the amplitude control and drives the output attenuator. DC offset is achieved by offsetting the output amplifier.

The output attenuator, fed directly from the output amplifier, provides up to 70 dB of attenuation to the selected waveform or DC offset. This signal is connected directly to the FUNC OUT BNC.

4.3 PULSE BLOCK DIAGRAM ANALYSIS

Refer to figure 4-2. All signals found on the pulse board originate from the hysteresis switch, trigger circuit, and zero crossing detector, all on the main board. In addition, when the unit is in one of the three BURST modes, the delay one shot acts as an auxiliary generator which can be triggered and gated from the front panel TRIG controls and TRIG IN connector. The signals return to the square shaper and trigger baseline circuits on the main board, and terminate at the PULSE/SQUARE OUT and PULSE SYNC OUT front panel connectors.

In the □ function, the hysteresis switch output (HYS OUT) is sent directly to the PULSE/SQUARE OUT connector by way of the ECL-to-50Ω converter. This signal also passes through a normal/invert circuit before being sent to the main board square shaper, where it can be modified to a positive pulse, negative pulse, or

provide an output balanced about ground, depending on which PULSE/SQUARE OUTPUT button is depressed. In PULSE function, the output of the width one shot (WOS) is substituted for the □ function.

With the MODE switch in one of the three FUNC positions, the output of the trigger circuit is sent directly to the trigger baseline compensation circuit.

Three signal lines labeled T, DLY, and TD are used to drive the width, delay and sync one shot. T originates from either the trigger or zero crossing detector circuits on the main board. With the FUNCTION switch set to PULSE/BURST and the MODE switch set to CONT FUNC or GATE FUNC, T is driven by the zero crossing detector, but when the MODE switch is set to TRIG FUNC or one of the three BURST modes, T is driven by the trigger circuit. TD is a delayed T signal and originates from the trigger delay circuit. DLY is the one shot output of the delay one shot. The one shot trigger steering logic circuit connects T, DLY, and TD to the three one shot circuits depending on which PULSE button is depressed. Refer to the one shot trigger steering logic of figure 4-2 and use PULSE DLY as an example: DLY is connected to the width one shot, T is connected to the delay one shot, and TD is connected to the sync one shot.

In the CONT BURST or GATED BURST modes, DLY is also sent to the width and sync one shots. The sync one shot output (SOS) is sent to the ECL-to-50Ω converter which drives the PULSE SYNC OUT connector.

In BURST mode, the width one shot output (WOS) is sent to the main board trigger baseline circuit.

The PULSE DELAY/BURST RATE selector controls the delay one shot and the PULSE WIDTH/BURST WIDTH selector controls the width one shot, along with their respective verniers.

4.4 DETAILED CIRCUIT DESCRIPTIONS

4.4.1 Current Sources

Refer to the Generator Board Schematic sheet 4. The VCG IN (J7) and FREQ VERNIER (R88) are summed with the dial potentiometer (R56) at the summing node, U14 pin 6 of the VCG amplifier. Full scale on the dial causes a -5 volt control signal at the dial buffer output U14 pin 7. Rotating the dial to minimum, plus turning the FREQ VERNIER ccw produces -5 mV at U14 pin 7. The output of the buffer drives both the GCV buffer and current sources. The GCV output at U14 pin 1 is +5.0 volts at full scale.

The current source from U14 pin 7 is present at U13 pin 1. The output of U13 at pin 12 is fed through level

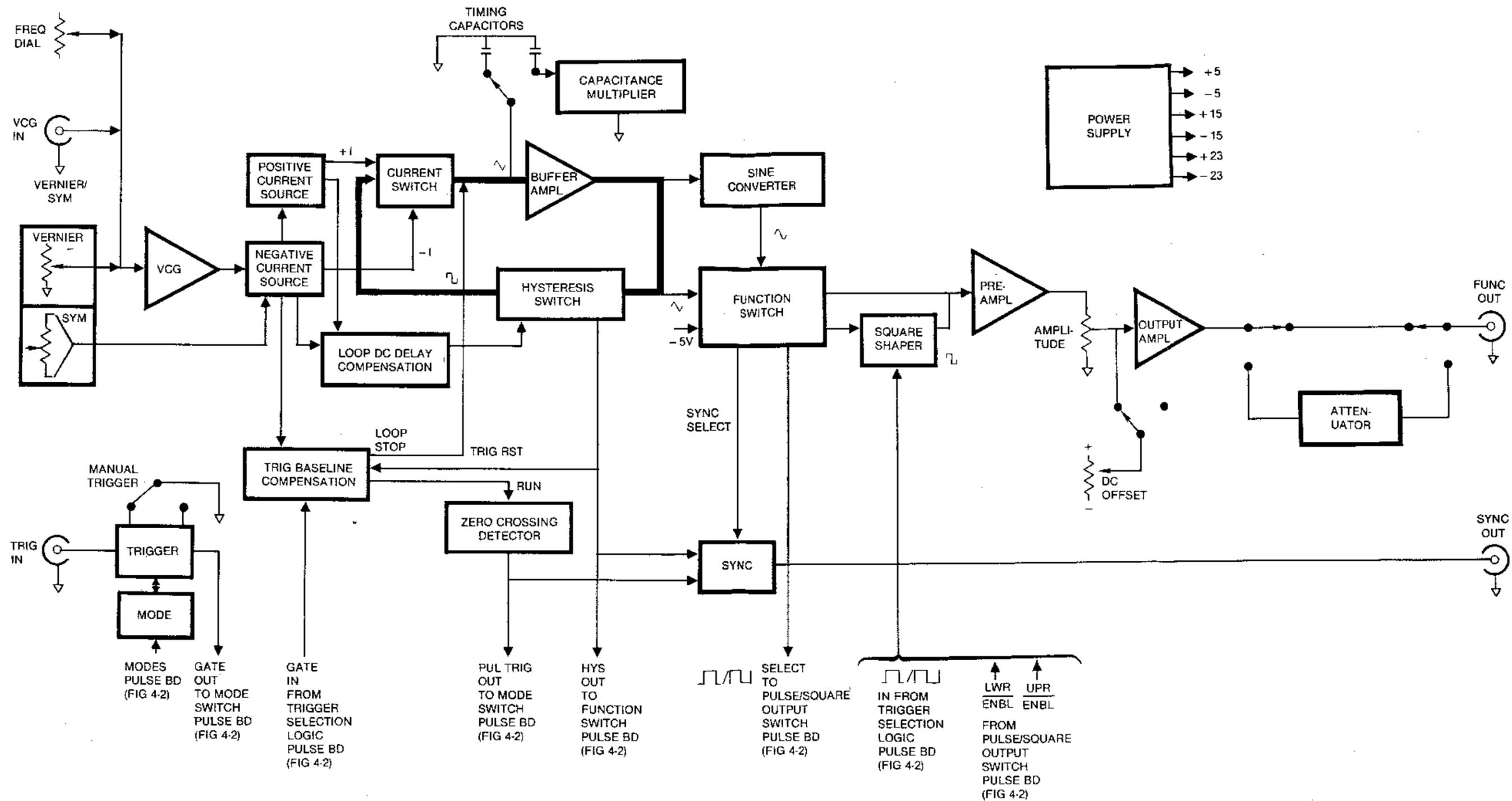


Figure 4-1. Function Generator Functional Block Diagram

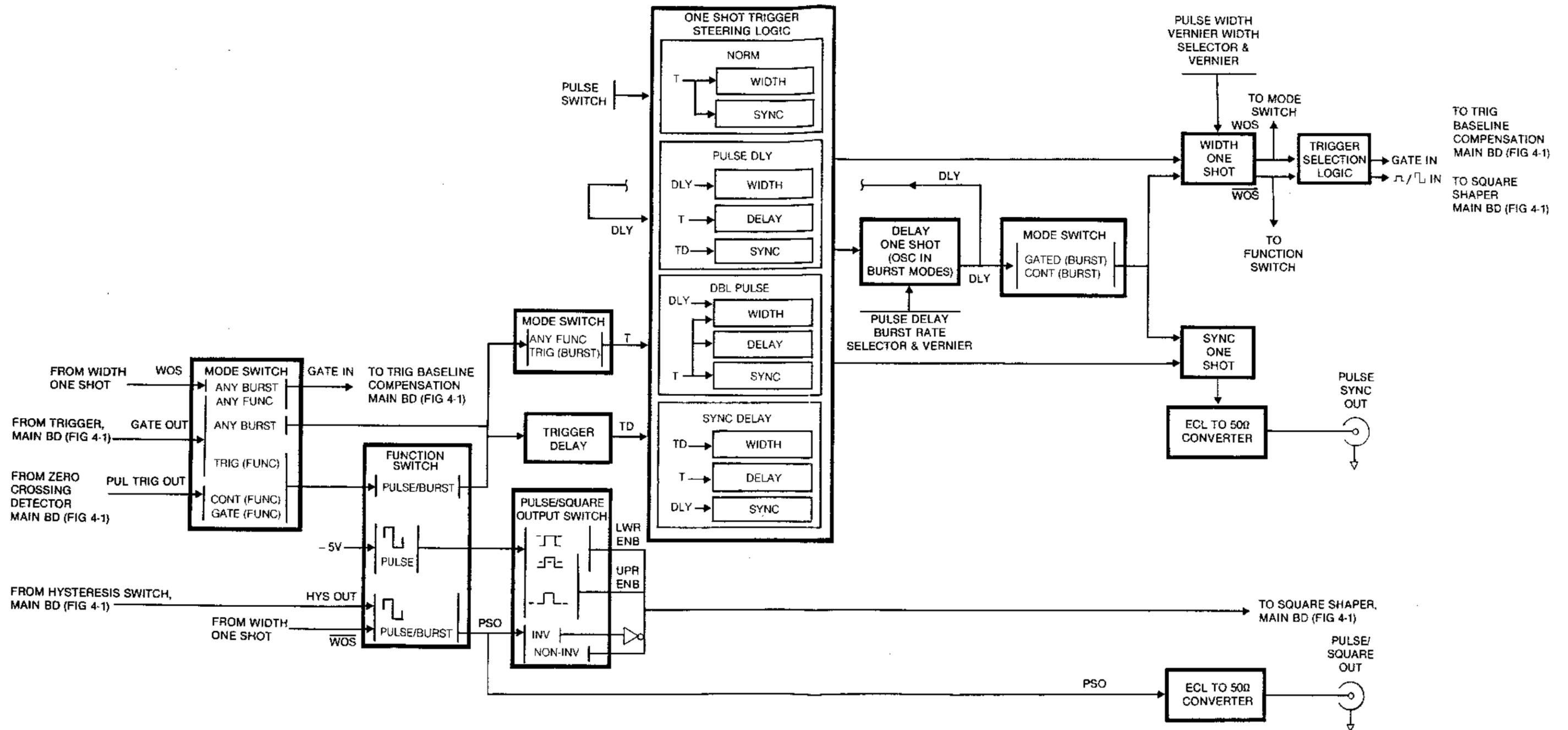


Figure 4-2. Pulse Block Diagram

shifting transistor Q14 to U8 pin 6. The collector current at pin 7 flows from ground through R81 and R80. As the voltage at U14 pin 7 varies, amplifier U13 and transistor Q14 adjust the base drive of U8 pin 6, and hence the collector current, until the voltage at U13 pin 2 equals the voltage at U13 pin 1. Because U8 is an array of matched transistors with the bases connected together, and all emitter resistors are equal with VERNIER selected, all collector currents are also equal.

The positive current source is controlled by a current control signal at U8 pin 1, which is held at 0 volts by the servo action of U13 pins 6, 7 and 10, level shifting transistor Q15 and U7 pins 6 and 7. The current "I" in R84 must flow through R93, and because these resistors are both 1k Ω , an equal but opposite base control voltage is present on U7 pin 6 compared to U8 pin 6. Because the transistors in U7 are matched and their bases are at the same point, a positive current "I" flows in R97 and hence the positive current source. A small amount of adjustable balance is provided by R95 and R94 to enable the positive and negative currents to be set for correct symmetry.

On the 1M and 10M ranges, the timing current is increased by approximately 25%, allowing the use of larger timing capacitors and hence, minimizing the effect of any stray capacitance. On the higher ranges, the parallel resistance across R83 (at ISCAL) is greater than the resistance on the lower ranges. This would decrease the current through U8 pin 8 were it not for the servo loop action of U13 pin 12, Q14 and U8 pins 6, 7 and 8. For any VCG setting at U14 pin 7 and U13 pin 1, no matter which range is selected, this servo loop maintains the voltage at U13 pin 2 equal to pin 1. Because the voltage at U13 pin 2 remains constant from range to range, the voltage across, and therefore the current through R80 and R81 also remains constant. This current also flows through U8 pins 7 and 8. To enable this current to remain constant, the servo loop drives the base voltage at U8 pin 6 in a positive direction. Because all of the bases in U8 are at the same point, the current relative to the lower ranges increases in R84 through R87 and also in the collectors of U8 pins 1, 14, 2, and 9.

Variable symmetry is controlled by R88 which doubles as the frequency vernier. With VERNIER selected, R88 functions as a frequency vernier with one end of the control connected to ground and the other connected to the -15 volt supply. The wiper supplies current to the summing node U14 pin 6. Additionally, one end of 1k Ω resistors R84 through R87 are all connected to the -15 volt supply. For any given dial setting, the current through each of the four resistors is

"I". With SYM selected, R88 functions as a variable symmetry vernier with the wiper connected to the -15 volt supply. One end of this vernier supplies current to R84 and R85, while the other end supplies current to R86 and R87. With the vernier centered, each leg is approximately 5000 Ω and reduces the current through each of these 4 resistors to 1/10 I, dividing the generator frequency by 10. As the symmetry control is varied, resistors for the positive and negative current sources are changed in ratio, hence the current sources are unbalanced and the timing for the positive waveform is varied in respect to the negative waveform, resulting in variable symmetry.

Loop delay dc compensation currents (+ICMP and -ICMP), are supplied by Q16 and U8 pin 9 and track the timing currents.

A current (ITRGBL), is supplied by U8 pin 14 to the trig baseline circuit to compensate for variations in freq dial settings when the generator is in a quiescent trigger or gated mode.

4.4.2 Current Switch

Refer to sheet 3. The current switch is driven by the square wave signal (ISWCTRL) from the hysteresis switch. Level shifting transistor Q10 provides a control signal for the diode bridge CR8, CR9, CR30 and CR31. When the control signal is +1.8 volts, CR30 is reversed biased, allowing CR8 to conduct current from the positive current source to the timing capacitor selected by SW9-D. This produces a positive going ramp. CR31 is also turned on, which reverse biases CR9 and prevents current sinking from the timing capacitor to the negative current source. When the control signal is -1.8 volts, both CR30 and CR9 are forward biased, while CR31 and CR8 are reversed biased. At this time, current from the negative current source sinks from the timing capacitor, producing a negative going ramp.

4.4.3 Triangle Buffer Amplifier

Refer again to sheet 3 of the schematic. The signal on the selected timing capacitor is present at both the gate of Q11, and at U9 pin 2. These devices provide a very high input impedance for the signal to avoid leakage which would otherwise cause poor triangle linearity. The output current of Q11 controls the base drive to emitter follower Q13 and hence the output voltage on the emitter. This voltage is sensed at U9 pin 3, causing U9 to adjust the base voltage of Q12 until the differential input of U9 is zero. The low impedance source output voltage at the emitter

follower Q13 now follows the high impedance input signal at the gate of Q11 with a circuit gain of unity.

4.4.4 Hysteresis Switch

Refer to sheet 2. U10 pin 5 is the input to the positive peak comparator, while pin 10 is the input to the negative peak comparator. A level shifted triangle signal of -0.9 volts to -2.8 volts is present at pins 5 and 10 of U10. Assume a positive going ramp. R18 and R19 set the reference voltage on U10 pin 4 at -0.9 volts. When the voltage on pin 5 exceeds the reference voltage on pin 4, the positive comparator changes state and the voltage on pin 3 pulses from an ECL low ($-1.8V$) to an ECL high ($-0.8V$). This signal is connected to clear direct (pin 4) of D flip flop U5. The output of U5 pin 2 goes low, while U5 pin 3 goes high. These outputs toggle the differential pair Q7 and Q8 so that Q7 is on and Q8 is off. This causes the current switch control signal (ISWCTRL) to go low, which connects the negative current source to the timing capacitor, and causes the triangle to begin to ramp negative. The negative peak comparator functions in an identical manner to the positive comparator except that the reference voltage at U10 pin 9 is -2.8 volts. At the negative triangle peak, U10 pin 6 pulses high, causing a set direct at U5 pin 5, toggling the current switch signal (ISWCTRL) high and producing a positive going ramp. In addition to being used to store the first peak comparison pulse from U10 pins 3 and 6, U5 also ignores "chatter" from both positive and negative comparators.

4.4.5 Loop DC Delay Compensation

The circuit is also located on sheet 2 of the schematic diagram. The purpose of this circuit is to adjust the reference voltages on the comparators in the two highest frequency ranges so that the triangle peaks do not increase in amplitude due to loop delay. Q2 functions as a variable positive current source controlled by the range switch and the main current source. As the generator frequency is increased, the base voltage of Q2 progressively moves negative causing positive current through R15 and increasing the reference voltage on U5 pin 9 in a positive direction. This causes the negative peak to switch earlier in time, compensating for the loop delay and maintaining constant triangle amplitude and correct frequency tracking.

The positive peak comparator reference is changed in an identical way, except that the voltage on U10 pin 4 becomes more negative with increased frequency. Q4 is a variable negative current source. Q1 and Q3 function as temperature compensating diodes.

4.4.6 Capacitance Multiplier

Refer to schematic diagram sheet 5. The capacitance multiplier is a precision current splitter which shunts up to 99.990% of the VCG current away from the integrating capacitor (C57) to produce the 100 through 0.1 frequency ranges. Timing current is divided between C57 and R114, then again between R113 and the selected timing resistor (R110 through R112 or R108).

The signal at U11 pins 2, 6, and 7 is a ± 1.0 volt triangle. U11 (pins 6, 7, and 10) is a non-inverting amplifier with a gain of 8. The waveform at U11 pin 1 is a ± 1.0 volt triangle with 0.5 volt spikes at each peak. At any given moment, the junction of R103 and C55 (differentiator circuit input) has 8 times the voltage as the junction of R104 and C55. This voltage difference causes a constant current to charge C55 through R104 and the selected timing resistor. Thus a frequency dependent charging current flows into the summing node of U11 pin 1, producing an inverted square wave component at the differentiator output U11 pin 12 sinking or sourcing current from the main current sources and limiting the amount of current available to charge C57. The ± 1.0 triangle at U11 pin 2 provides the triangle portion of the waveform at U11 pin 12. Since the triangle slopes on U11 pins 1 and 12 are identical, only the square wave component of the waveform at U11 pin 12 is across the timing resistor. The amount of current supplied to charge C55 is therefore this voltage divided by the range resistor value. As the range resistor is increased, the feedback for U11 between pins 1 and 12 is also increased, causing less current to charge C55 and increasing the amount of current being shunted to U11 pin 12 by a factor of 10 for each lower frequency range.

4.4.7 Sine Converter

Refer to sheet 6 of the circuit diagram. The sine converter converts the buffered ± 1.0 volt peak triangle to a sinusoidal current of 2mA peak. The input triangle voltage (TRIBUFC) passes through a voltage divider network to the input of the diode at pins 1, 4 and 6. As this signal progressively increases, the diode between pins 1 and 9 is progressively reversed biased, sinking less current and causing the diode between pins 2 and 5 to pass increasingly more current in a sinusoidal manner to IFUNC. This produces the positive half of the sine wave at the output of the preamplifier. At the same time, the diode between pins 2 and 8 is progressively reversed biased. This slows and eventually prevents current from flowing from the negative portion of the sine converter.

When the input waveform moves negatively, the diode between pins 2 and 5 is reversed biased and the diode

between pins 2 and 8 progressively conducts, producing the negative half of the sine wave.

R159 sets the input amplitude for correct biasing of the sine conversion diodes, while R165 adjusts the input signal offset. Thermister R161 adjusts the input voltage to compensate for the diode voltage change with temperature. The network consisting of R166, R167 and C102 provides a signal (SINCMP) to the non-inverting input of the preamplifier to compensate for the effects of diode capacitance which would otherwise distort the sinewave peaks at high frequencies.

4.4.8 Trigger Circuit

Refer to sheet 5. The trigger input at J8 is added to the voltage from the trigger level control R119 and compared at U12 pin 5 with a reference at U12 pin 4. When the signal at U12 pin 5 exceeds pin 4 by a few millivolts, U12 pin 3 goes high. R120 and C60 ensure a noise free pulse at U12 pin 3 which is one of two wire ORed inputs to U4 pin 7. The second input originates from the MAN TRIG switch circuit. When this switch is depressed, R115 pulls U12 pin 10 low. Pin 10 is compared to the Vbb reference voltage at pin 9, latching pin 6 high and preventing false triggering due to switch contact bounce. Pin 13 connected to pin 6, is referenced to pin 12, causing pin 15 to also go high. When either U12 pin 3 or pin 15 go high, U4 pin 3 goes low because these outputs are wire ORed to U4 pin 7. U4 pin 3 is connected to pins 4 and 10. Because pin 10 was previously high, U4 pin 14 was low causing a low at U4 pin 5. The trigger pulse low at U4 pin 4 causes a 10 ns ECL high pulse at U4 pin 2. At the same time, U4 pin 14 goes high and after the time delay set by R126 and C62, U4 pin 5 also goes high. This causes U4 pin 2 to return low.

In the gate mode CR14 holds U4 pin 11 high, forcing pin 14 low. The length of the control pulse at U4 pin 2 is now equal to the period during which U4 pin 7 is held high. In the continuous mode, U4 pin 2 is held high by CR16 regardless of any input trigger signals.

4.4.9 Trigger Baseline

Refer to sheet 5. In the trigger mode, with no trigger inputs, U5 pin 12 is held low. On the next positive going triangle, the trigger reset (TRIG RST) signal at U5 pin 11 causes U5 pin 14 to go high. This turns Q18 off and Q17 on, which turns off Q19. The Q19 emitter voltage is pulled down by the negative current sources Q20 and Q21, causing CR19 to conduct. Because the anode is at ground and CR18 is matched to CR19, the voltage at the anode of CR18 is also zero. This causes the triangle on the positive going ramp to stop at ex-

actly zero volts. When a trigger signal occurs, U5 pin 12 goes high for about 10ns, causing pin 15 to also go high. This turns on Q18 and turns off Q17, which turns on Q19, causing the emitter to rise to about 1.7 volts. This reverse biases CR18 and CR19 causing the generator to run for exactly one cycle. In the gate mode, U5 pin 12 is held high for the duration of the input signal causing the generator to run for this interval plus the time required to complete a partial cycle.

In the trigger or gated mode, quiescent state, positive charging current I flows in CR18. As the VCG current is varied, I also varies, causing the voltage across CR18 to vary. To prevent this from causing a baseline shift, current (I) must also flow in the reference diode CR19. A negative current source (ITRGBL) is connected to the bases of Q20 and Q21. Negative current ($-I$) flows through the collector of Q20 and R133. Because of the configuration of Q20 and Q21, and because R133 and R134 are both $1k\Omega$, an equal amount of current $-I$ also flows through the collector of Q21 and R134, causing $-2I$ to flow at the junction of R133 and R134. Half of this current ($-I$) flows through CR19, while the remaining current flows through CR18. Therefore, the anode of CR18 is held at zero volts regardless of the VCG summing node current.

The \overline{RUN} signal is used to hold the sync output low during quiescent periods.

4.4.10 Sync

Refer to sheet 2. The SYNC OUT amplifier is driven from the signal at U6 pin 10 in the triangle and sine functions, and from U6 pin 7 when the function switch is in the square function. These two inputs are wire ORed at U6 pin 13.

In the triangle and sine functions, SYNC SEL allows R23 to pull CR4 high causing a low at U6 pin 2. This enables the signal from the zero crossing detector output (U10 pin 15), and disables the hysteresis switch input at U6 pin 7. When the positive going ramp crosses 0 volts at the zero crossing detector input U10 pin 13, U10 pin 15 and U6 pin 10 go high. This causes a low at U6 pins 14 and 13. U6 pin 9 goes low and pin 15 goes high turning on Q5 and turning off Q6. This results in a high at SYNC OUT. As the triangle at U10 pin 13 crosses 0 volts in a negative direction, pin 15 goes low, causing Q5 to be turned on, producing a low at SYNC OUT. Therefore the SYNC OUT always toggles when the triangle crosses 0 volts.

When the square wave function is selected, CR4 pulls U6 pins 4 and 6 low. U6 pins 2 and 11 now go high, disabling the zero crossing detector input from pin 10,

and enabling the square wave input from U6 pin 7. U5 pin 3 now drives the SYNC OUT connector in a similar manner as U10 pin 15. The SYNC OUT is in phase with the square wave output.

R26, a 49.9Ω resistor sets the 50Ω output impedance.

4.4.11 Square Shaper

The square shaper schematic is located on sheet 6. In square function, CR20 pulls U4 pin 13 low, enabling the hysteresis switch input (HYS) at U4 pin 12. A low at U4 pin 12 causes a low at U4 pin 15 and a high at pin 9. Q22 turns on while Q23 is turned off, producing a +1.2 volt high at the bases of the current switch control transistors Q24 and Q25. Transistor Q25 is on, reverse biasing CR23. Transistor Q24 is off allowing positive current to flow through R147, CR22, R154 and into the preamplifier node via R152.

When HYS toggles high, Q23 turns on forcing the bases of Q24 and Q25 to -1.2 volts. Q24 turns on and Q25 turns off, allowing negative current to flow through R157, CR23, R154 and the the amplifier node via R152.

R152 and R154 form a current divider to obtain a 2mA full scale current into the preamplifier. Overshoot caused by diode capacitance is reduced by R153 and C73. The output of the square shaper is disabled in all other functions by turning on Q26 and CR24 which reverse bias CR22 and CR23 and prevents current from flowing through R152.

4.4.12 Preamplifier

Refer to sheet 7 of the schematic circuitry. For all functions, full scale output voltage is produced when 2mA is injected into the input summing node U1 pin 8. Transistor array U1 forms a cascaded differential stage. Transistor Q27 is a fixed current source. Q28 and Q29 form a high gain voltage follower. DC negative feedback is applied through R195 to U1 pin 8. The closed loop voltage gain of the amplifier is determined by the ratio of R195 to the input resistors, R152 for square wave and R176 for triangle. The sine converter output supplies the correct current directly from U3 pin 2 to U1 pin 8. The servo action of the preamplifier holds this point at 0 volts, therefore no voltage can be measured. U1 pin 4 is the non-inverting input and is used both to adjust the offset to 0 volts at TP2 using R185 and to inject the sine converter compensation signal (SINCOMP) described under paragraph 4.3.7, Sine Converter. High frequency compensation is provided by R182, C81, C86 and C153. Zener diode CR29 provides increased collector voltages for U1 pins 11 and 12 and also allows these two points to be relatively close in voltage.

4.4.13 Output Amplifier

The output amplifier consists of an ac coupled amplifier for signals above about 16 kHz, and a dc coupled amplifier for signals below about 16 kHz, and to maintain zero dc output offset within specified limits. Refer to the simplified output amplifier schematic, figure 4-3.

Assume zero input voltage at the junction of R203 and R218. The output at R222 and R224 is maintained at 0 volts by dc amplifier U2. U2 pin 3 is connected to a 0 volt reference. If the output drifts away from 0 volts, this will be sensed at U2 pin 2 through R256, R257 and R254. Amplifier U2 will sense a difference between its inputs and produce an output voltage which adjusts the bias in the ac coupled amplifier to return the output to 0 volts. Because R218 and R223 form half of a balanced bridge, and R253, R256 and R257 form the second half, the amplifier node at the junction of R218 and R223 will be held at 0 volts as U2 has returned the junction of R253 and R256 to 0 volts.

A dc input of +1 volt at R218 and R253 is sensed as a positive increase at U2 pin 2, causing U2 pin 6 to go negative. The ac amplifier output goes negative in response to the dc control input. This continues until the output becomes sufficiently negative to sink all the input current, and return U2 pin 2 to 0 volts. The bridge circuit causes the ac amplifier node to be 0 volts. If the input is +1 volt and the node at the junction of R218 and R223 is 0 volts then the input current is $1/12 I = 8.26 \text{ mA}$. All of this current must flow in R223. Because the node is at 0 volts, the output voltage must be $-8.26 \text{ mA} \times 2\text{k}\Omega = -16.52\text{V}$. Therefore the amplifier voltage gain = $R223/R218 = 16.52$.

Above about 16 kHz, the ac amplifier controls the summing node directly, sinking or sourcing current through R223 by adjusting the output voltage to hold the node at 0 volts. The ac amplifier gain is also $R223/R218 = 16.25$. This is divided by 2 at the output terminal, due to the 50Ω source impedance resistors R222 and R224, providing the output is also terminated into 50Ω .

Refer to sheet 7. The top half of the circuit amplifies the positive portion of the signal, and the bottom half amplifies the negative part. Q30 and Q31 form an ac gain stage. An emitter follower stage is formed by Q32 and Q33, to provide a low impedance drive to the second voltage gain stage Q36 and Q39. This stage drives the parallel output emitter followers Q37 and Q38 on the positive side, and Q40 and Q41 on the negative. Diodes CR23 and CR26 set thermally stable bias for the output transistors. Networks R211, R212, C94 and C93 bypass emitter resistor R208, while R245, R246, C107 and C106 bypass R244. As fre-

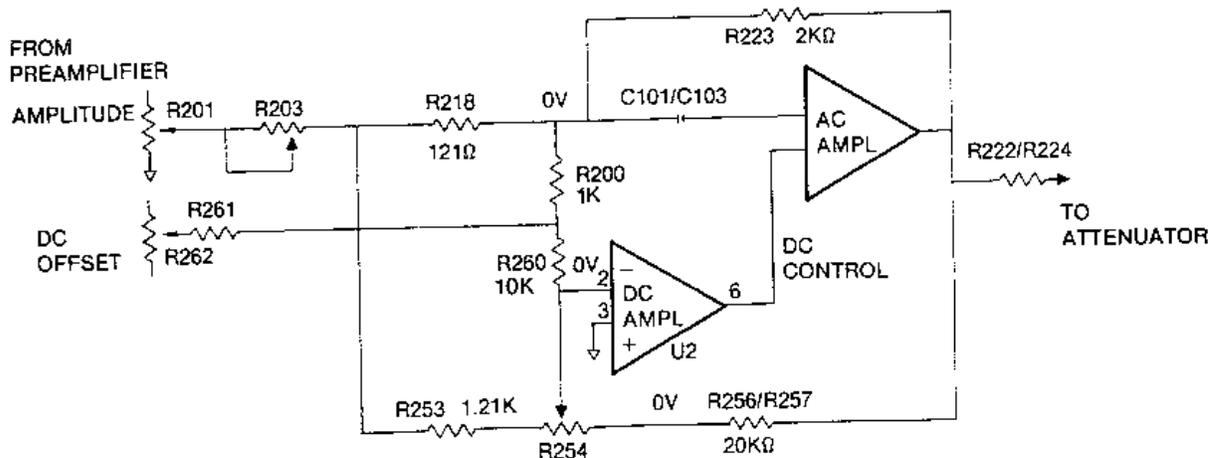


Figure 4-3. Simplified Output Amplifier

quency is increased, these components decrease the local negative feedback in the driver stage, increasing the high frequency gain. Voltage regulators VR5 and VR6 have external current limiting circuitry set to limit at about 220 mA to prevent damage in the event of a shorted transistor. When the offset button is depressed, offset current is injected directly into both nodes in proportion to the feedback resistor values. The amplifier responds exactly as described above for a dc input.

4.4.14 Output Attenuator

Refer to sheet 7. Each attenuator button selects an independent voltage divider, which has 50Ω input and output impedances to correctly load the amplifier and to provide a constant 50Ω impedance at the FUNC OUT terminal.

The 10dB attenuator has a 3.16/1 voltage division ratio. The 20dB attenuator has a 10/1 voltage division ratio, and the 40dB stage has a 100/1 ratio. These ratios multiply in voltage. For example if the 20dB and 40dB buttons are depressed, the voltage division ratio is 1000/1. The attenuators add algebraically in dB, therefore any attenuation from 10 to 70dB may be selected in 10dB steps.

4.4.15 Signal Routing Gates

All signal routing is performed by logic gates that are controlled by the MODE, PULSE, and FUNCTION switches, refer to the pulse board schematics sheets 1 and 3. These logic gates are part of the following circuit blocks: Switch Position Decoding logic, One Shot Trigger Steering logic, and Trigger Selection logic. For detailed information on signal routing relative to

switch settings, refer to the simplified pulse board schematics in section 6.

4.4.16 Variable Duty Cycle One Shots

When triggered, a one shot produces a pulse whose duty cycle is controlled by a variable current source and timing capacitor. There are three variable duty cycle one shots on the pulse board: Width, Delay/Burst, and Sync. The three one shots each serve special functions, but they all have certain common features. First, a general description provides an understanding of how a variable one shot works. Then, subsequent paragraphs gives detailed descriptions of each of the three one shots.

4.4.16.1 General Description

A basic variable one shot, refer to figure 4-3, consists of a fixed duty cycle one shot, latch, comparator, range capacitors, and variable current source.

The one shot is initiated by the positive going transition of a triggering pulse. A fixed duty cycle one shot converts this positive transition to a 5ns pulse, which sets the latch. When set, the latch output (pin 3) becomes reversed biased, essentially an open circuit. At this time, the timing capacitor (C1 or C2) begins charging via the variable current source. As the capacitor is charged, a negative going ramp is produced. When the ramp reaches $-2.4V$, the comparator changes state (low to high) to produce a positive going transition. This transition resets the latch, terminates the ramp, and returns the comparator output to low. Another trigger pulse now can retrigger the one shot. The one shot output is a buffered pulse from the latch (pin 4).

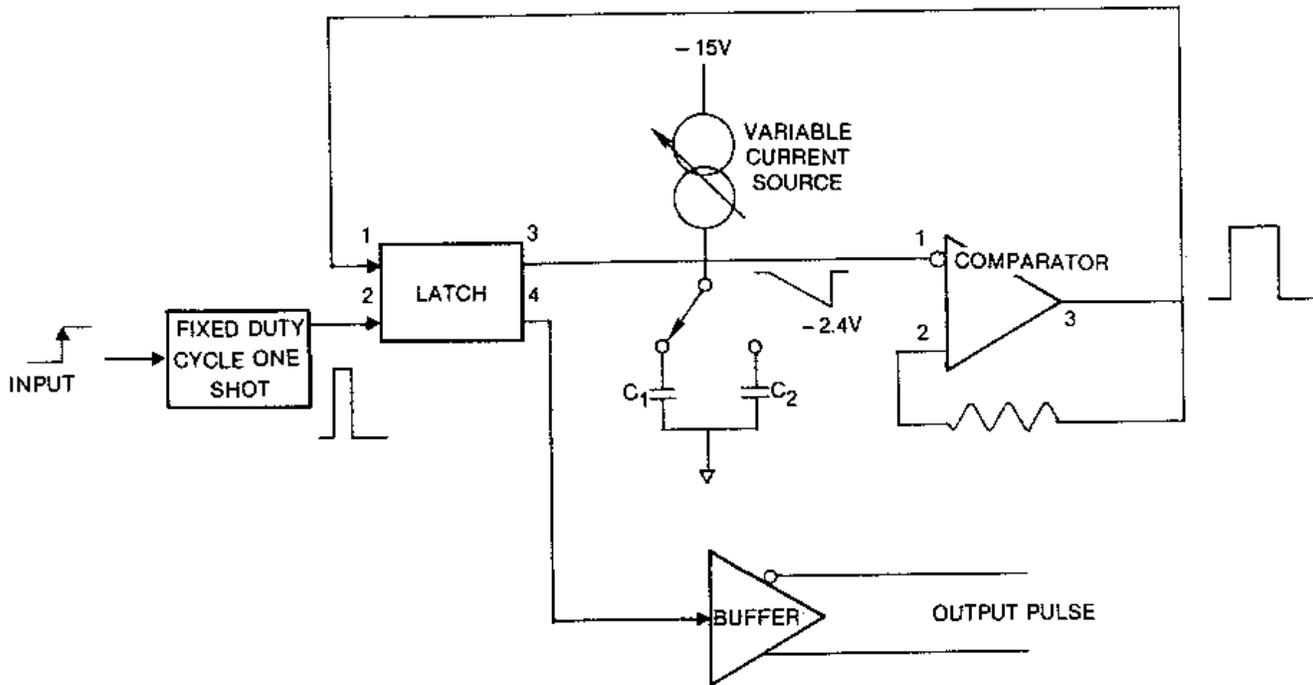


Figure 4-4. Variable Duty Cycle One Shot

The variable current source controls the timing capacitor charging rate. The front panel vernier controls the current source over a 10:1 range.

4.4.16.2 Width One Shot

The width one shot, refer to the pulse board schematic sheet 2, receives a trigger pulse from either WIDTH TRIG 1 or 2. This trigger pulse is converted to a 5ns pulse which sets the latch (U13 pin 6). When set, the latch output (U13 pin 9) goes low which turns off Q2 that reverse biases Q3 and Q5. Now the current source, Q9 and Q7 can charge the timing capacitor (C11, C12, C13, C14, C15, C16, or C18). The amount of charging current is controlled by the PULSE WIDTH/BURST WIDTH vernier. Charging the capacitor produces a negative-going ramp. The ramp is buffered by transistor Q6 which drives the comparator U12 pin 4. The emitter current of Q6 is controlled by transistor Q8, part of the current source. This makes the buffers current proportional to the charging current, which minimizes timing errors at long pulse width settings. The comparator output U12 pin 3 changes states (low to high) when the comparator input reaches its trip point (approximately $-2.4V$). The positive-going transition resets the latch U13 pin 13.

When reset, the latch output U13 pin 9 goes high turning on Q2 and Q3. Q3 begins to discharge the timing capacitor at a 30 mA rate. At the same time, Q5 is turned on which forces U12 pin 7 high; this prevents triggering of the one shot.

As the ramp discharges and approaches $- .4V$, Q4 acts as a fast clamp circuit which reduces the discharge current to 10 mA. As the current through R15 increases the current through R16 will decrease to cause the current through Q3 and Q5 to decrease. With less current through Q5, U12 pin 10 returns low, thus enabling the latch U13 pin 12. The one shot can be triggered again.

During the quiescent state, transistor Q3 and Q4 sink all the current from the current source. This prevents the timing capacitor from charging.

The pulse from the width one shot is originated at the latch (U13 pin 15), buffered by the amplifier (U12 pins 14 and 15), and fed to the trigger selection logic.

4.4.16.3 Delay One Shot/Burst Oscillator

The delay one shot/burst oscillator is similar to the width one shot (ref: paragraph 4.4.16.2), except added circuits allow it to function, in burst modes, as an oscillator.

As a one shot, a trigger pulse will set the latch (U11 pin 3). The current source (Q20 and Q22) charges the timing capacitor (C38, C39, C40, C41, C42, C43, C44 or C45); the PULSE DELAY/BURST RATE VERNIER controls the amount of charging current. A negative-going ramp is produced. When the ramp reaches $-2.4V$, the comparator toggles resetting the latch. The output pulse from the one shot is originated at the latch (U11 pin 15), buffered by the amplifier (U10 pins 14 and 15), and routed to the one shot trigger steering logic.

When continuous or gated modes are selected, the delay one shot functions as an oscillator. BURST RATE and VERNIER controls the oscillator frequency. To enable the oscillator, the control line $\overline{B(G+C)}$ goes low. This turns on Q18 and forces control line BED high. With BED high Q23 turns on, this disables the trip point compensation circuit (U10 pin 5). In addition, control line DLY DIS goes high, thus turning off transistor Q17 and Q19 which reduces the current from the current sources.

With BURST CONT selected, the control lines GATE OUT (U3 pin 11) and GATE ENB (U3 pin 10) goes high, which forces T (U3 pin 14) high. With $\overline{B(G+C)}$ and T high, the one shot is enabled as an oscillator.

With BURST GATE selected, the control line $\overline{B(G+C)}$ remains high, but, the line T follows the trigger input signal. This enables the oscillator each time T goes high.

With BURST TRIG selected, a pulse will trigger the oscillator to produce a single oscillator cycle.

4.4.16.4 Sync One Shot

The sync one shot, refer to pulse board schematic sheet 2, receives its trigger input (SYNC TRIG) from the one shot trigger steering logic. The fixed duty cycle one shot converts the SYNC TRIG pulse into a 5ns pulse that sets the latch (U5 pin 9). The current source (R41) charges the range capacitor (C25, C26, C27, C28, C29, or C30) to produce a negative going ramp. When the ramp reaches the reference level (approximately $-2.4V$) the comparator (U4 pin 7) toggles high to reset the latch (U5 pin 12). On the 100ns and 20ns pulse width ranges the resistors R43 and R44 parallels the current source resistor R41, this increases the charging current to C30.

The output pulse from the sync one shot is originated at the latch (U5 pin 15), buffered by an amplifier (U4 pins 14 and 15), and routed to the ECL to 500 Ω converter.

5

SECTION
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter Millivolt dc measurement (0.1% accuracy), true rms
 Oscilloscope, Dual Channel . . . 100 MHz bandwidth
 Counter 20 MHz (0.01% accuracy)
 50Ω Feedthru ± 1% accuracy, 2W
 Distortion Analyzer To 200 kHz
 RG58U Coax Cable . . . 3 ft length BNC male contacts
 Spectrum Analyzer To 20 MHz

5.3 COVER REMOVAL

NOTE

Before removing the covers, disconnect the instrument from the ac power source.

Invert the instrument and remove the four screws in the bottom cover. Remove the bottom cover.

NOTE

Remove the cover only when it is necessary to make adjustments or measurements.

5.4 CALIBRATION

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1, 5-2. If performing partial calibration, check previous settings and adjustments for applicability. Calibration points are

shown in figure 5-1. Notice that the pulse board does not require calibration.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Section 1 of this manual.

1. All measurements made at the FUNCTION OUT connector must be terminated into a 50Ω (± 1%) load.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

2. Start the calibration by removing covers as described in paragraph 5.3, connecting the unit to an ac source and setting these front panel switches as follows:
 - SYM Off (extended)
 - TRIG LEVEL 12 o'clock
 - DC OFFSET Off (extended)
 - OUTPUT ATTEN 0 dB (all extended)
3. Allow the unit to warm up at least 2 hours for final calibration. Keep the instrument covers on to maintain heat. Remove covers only to make adjustments or measurements.

Table 5-1. Calibration Procedure

Note: Where there are no entries, open column indicates previous entry is applicable.

	Test	Dial	Freq Mult	Vern/ Sym	Mode	Func	Ampl	Test Point	Tester	Adjust	50Ω Load	Result	Remarks
1 (1)	± 15V Supply	2.0	1K	cw	FUNC CONT	Sqr	cw	See remarks	DVM	Verify	No	30 ± 1.5 Vdc	Read voltage between +15V and -15V on PC board.
1 (2)	± 15V Balance	—	—	—	—	—	—	Board +15V	—	R3	—	See remarks	Match +15V and -15V readings within 10mV. Ref gnd is TP7.
1 (3)	—	—	—	—	—	—	—	Board -15V	—	Verify	—	—	
2	+5V Supply	—	—	—	—	—	—	+5V	—	—	—	+5 ± .25 Vdc	
3	-5V Supply	—	—	—	—	—	—	-5V	—	—	—	-5 ± .25 Vdc	
4	+23V Supply	—	—	—	—	—	—	FB1	—	—	—	+21.9 ± 1.1 Vdc	
5	-23V Supply	—	—	—	—	—	—	FB2	—	—	—	-21.9 ± 1.1 Vdc	
6	Power Ampl Zero	—	—	—	—	dc	ccw	FUNC OUT	—	R258	Yes	0 ± 20 mVdc	
7	Preamp Zero	—	—	—	—	—	cw	—	—	R185	—	—	
8	Top of Dial Symmetry	—	—	—	—	Sqr	—	—	Scope	R96	—	Asym < 1μs	Set for min asym. (Set by alternate triggering of scope ± slope.)
9	VCG Null	.02	100K	—	—	—	—	—	—	R65	—	See remarks	Set for min freq shift when VCG is grounded. Repeat steps 8 and 9 as necessary.
10	100:1 Symmetry	—	—	—	—	—	—	—	—	R94	—	Asym < 1μs	Set for min asym.
11	1000:1 Frequency	—	—	ccw	—	—	—	—	Counter	R63	—	160 (+0, -20) Hz	
12	Triangle Offset	2.0	1K	cw	—	Tri	—	—	DVM	R17	—	0 ± 20 mVdc	
13 (1)	Sine Distortion	—	—	—	—	Sine	—	—	Dist. Analyzer	R159	—	< .18%	If not < 0.35%, perform step 26 and continue with step 13.
13 (2)	—	—	10K	—	—	—	—	—		R165	Verify	—	
14 (1)	Triangle Trigger Baseline	—	1K	—	FUNC TRIG	Tri	—	—	DVM	R51	—	0 ± 20 mV	Note reading for use in next step.
14 (2)	—	Traverse	—	—	—	—	—	—	Scope	See remarks	—	Step 14 (1) reading ± 180 mV	Verify the dc limits.
15	Sine Trigger Baseline	—	—	—	—	Sine	—	—	—	—	—	—	
16 (1)	Dial Alignment	2.0	—	—	FUNC CONT	Sqr	—	SYNC OUT	Counter	R81	—	2 kHz ± 10 Hz	
16 (2)	—	0.2	—	—	—	—	—	—	—	Verify	—	100 ± 10 Hz	If satisfactory skip to step 18 (1).
16 (3)	—	See remarks	—	—	—	—	—	—	—	R81	—	2.068 kHz ± 10 Hz	Remove dial and set the shaft ccw.
16 (4)	—	—	—	—	—	—	—	—	—	See remarks	—	200 ± 20 Hz	Replace dial, align to 0.2, tighten set screw and verify setting.
17	Dial Tracking	See remarks	1K	—	—	—	—	—	—	Verify	—	Dial mark ± 40 Hz	Verify frequency at each major dial mark.
18 (1)	X10M Frequency	2.0	10M	—	—	—	—	—	Counter	C37	—	200 MHz ± 100 kHz	Optimize C66 value if setting is out of range for C37.
18 (2)	—	See remarks	—	—	—	—	—	—	—	Verify	—	Dial mark ± 600 kHz	Verify frequency at each major dial mark. Retouch C37 setting if necessary.

Table 5-1. Calibration Procedure (Continued)

	Test	Dial	Freq Mult	Vern/ Sym	Mode	Func	Ampl	Test Point	Tester	Adjust	500 Load	Result	Remarks
19 (1)	X1M Frequency	2.0	1M	cw	FUNC CONT	Sqr	--	SYNC OUT	Counter	Verify	Yes	See remarks	Trim C33 to Set 2MHz freq between 2.020 and 2.040MHz
19 (2)	--	Major Div.	--	--	--	--	--	--	--	Verify	--	Dial mark ± 40 kHz	
20	X100K Frequency	2.0	100K	--	--	--	--	--	--	--	--	200 ± 4.0 kHz	Optimize R39 value if necessary
21	X10K Frequency		10K	--	--	--	--	--	--	Verify	--	20 ± .4 kHz	
22	Capacity Mult Symmetry	0.1	100	--	--	--	--	FUNC OUT	Scope	R106	--	<20µs	Set for min asym. (Verify important for low freq sine dist.)
23 (1)	Capacity Mult Frequency	2.0	--	--	--	--	--	SYNC OUT	Counter	R102	--	199.5 ± 5 Hz	
23 (2)	--	--	10	--	--	--	--	--	--	Verify	--	50 ± 1 ms	Retouch R102 setting if necessary
23 (3)	--	--	1	--	--	--	--	--	--	--	--	500 ± 10 ms	
23 (4)	--	--	0.2	--	--	--	--	--	--	--	--	5s ± 100 ms	
24	Low Frequency Aberrations	--	1K	--	--	--	--	FUNC OUT	Scope	R254	--	See remarks	Adjust the "Corner Shape" for just noticeable peaking
25 (1)	Function Output Amplitude	--	--	--	--	Sine	--	--	DVM	R203	--	5.35 Vrms ± 01V	
25 (2)	--	.5	100K	--	--	See re- marks	--	--	Scope	See remarks	--	15 Vp-p (-0, +1.5V)	Verify sine, tri and sqr ampl
26	High Frequency Aberrations	--	10M	--	--	Sqr	--	--	Sample Scope	R245 R211	--	<0.6 Vp-p	Worst case aberrations not to exceed 4% of full ampl for each peak.
27	Square Wave Rise & Fall Time	--	--	--	--	--	--	--	--	Verify	--	<13ns	
28 (1)	Harmonic Content	See re- marks	--	--	--	Sine	--	--	Spec. Analyzer	--	--	<27 dB	Look for worst case over calibrated dial travel
28 (2)	--	--	1M	--	--	--	--	--	--	--	--	<33 dB	
29 (1)	Sine Roll-off	1.0	--	--	--	--	See	--	DVM	AMPLI- TUDE	--	17.5 dBm ± 1 dB	Set OUTPUT ATTN to -10 dB Set AMPLITUDE to 17.5 dBm ± 1 dB.
29 (2)	--	See re- marks	--	--	--	--	Hold setting	--	--	See remarks	--	17.5 dBm ± 2 dB	Look for worst case over calibrated dial travel.
29 (3)	--	--	10M	--	--	--	--	--	--	--	--	175. dBm ± 1 dB	

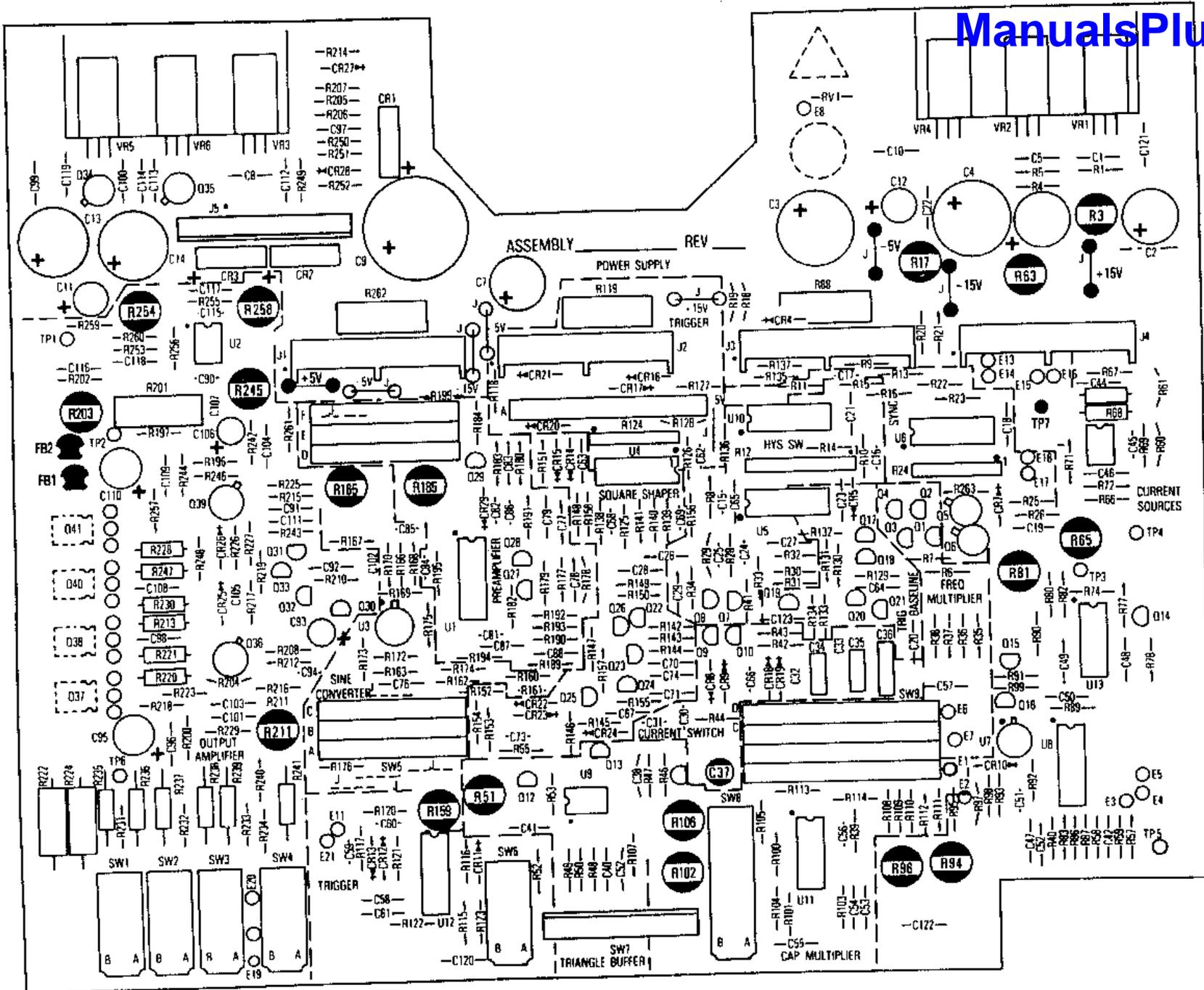


Figure 5-1. Calibration Points

6

SECTION

TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description in conjunction with the schematic. Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

For pulse problems, refer to paragraph 6.5. For all other problems, refer to paragraph 6.3.

6.3 MAIN BOARD TROUBLESHOOTING

Table 6-1 gives an index of common symptoms for the main board. (For pulse board troubleshooting, refer to paragraph 6.5.) For each symptom a troubleshooting guide is referenced (Paragraphs 6.3.1 through 6.3.15) that, when correctly followed, will lead to a solution to the problem.

The main board troubleshooting guide is arranged in three (3) levels:

1. Identify improperly set controls.
2. Isolate the faulty functional blocks.
3. Identify the faulty circuit or component.

Individual component troubleshooting is given in paragraph 6.6, recommended test equipment is given in paragraph 5.2 and circuit schematics are in the back of this manual.

In all problems:

1. Double check for proper control settings.
2. Calibrate or rule out calibration as a problem.
3. Inspect components, wiring and circuit boards for heat damage.
4. Recalibrate as necessary after circuit repair.

Find the instrument symptom caused by main board in table 6-1 and proceed as directed to the proper troubleshooting paragraph. See paragraph 6.5 for pulse board related problems.

Table 6-1. Main Board Related Symptoms

Symptom	Paragraph
Fuse blows, no dial lamp.	6.3.1
Power supply > 100 mVp-p ripple or out of specification.	6.3.2
Function out (all functions) distorted or missing.	6.3.3
Square output distorted or missing.	6.3.4
Sine wave output distorted or missing.	6.3.5
Triangle output distorted or missing.	6.3.6
Sync output distorted or missing (FUNC OUT normal).	6.3.7
Excessive high frequency sine or triangle roll off, excessive square wave overshoot and rise/fall time.	6.3.8
Low frequency square wave tilt.	6.3.9
Time symmetry cannot be adjusted within specification.	6.3.10
Frequency accuracy and dial response problems.	6.3.11
Trigger, gate and trigger baseline problems.	6.3.12
Voltage at VCG IN connector not changing frequency properly.	6.3.13
DC offset not functioning correctly.	6.3.14
Variable symmetry problems	6.3.15

6.3.1 Fuse Blows, No Dial Lamp

1. Fuse size incorrect for voltage setting.

2. Line voltage selector incorrectly positioned.
3. Disconnect P5. If ac voltages are now correct, refer to the power supply guide, paragraph 6.4.1. If not, inspect the transformer and power receptacle.

6.3.2 Power Supply > 100 mVp-p Ripple or Out of Specification

1. Check line voltage selector for correct position.
2. If the supply is 0V, check for a short between the faulty supply and ground by lifting the jumpers at rear of the board and removing the pulse board..
3. Lift P5 from the board. If the voltages at P5 are not close to the values shown on the schematic table, inspect the transformer and power receptacle. If the voltages are normal, connect P5, then lift the jumpers (rear of board) for faulty supply. If the supplies are still bad, refer to paragraph 6.4.1. If not, the problem is caused by an excessive current drain by the generator circuits.

6.3.3 All Waveforms at FUNC OUT Distorted or Missing

Improperly set controls:

1. OUTPUT ATTEN or AMPLITUDE controls incorrectly set too low for scope gain or voltmeter range.
2. FUNCTION switch incorrectly set to DC or PULSE/BURST.
3. MODE switch incorrectly set to TRIG (FUNC) or GATE (FUNC) or BURST modes.
4. SYM or DC OFFSET buttons depressed.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1
2. Check for a nonlinear triangle. If the triangle is nonlinear on only one range, check for a leaky capacitor on that range. If the triangle is nonlinear in more than one range, check for leaky capacitors or faulty active components in the frequency multiplier and triangle buffer circuits.
3. If the waveform is bad in one of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to the capacitance multiplier guide 6.4.9.
4. If the waveform is bad only in 1M or 10M FREQ MULT positions, refer to paragraph 6.4.3. If the

delay compensation circuit appears normal, refer to figure 6-1.

5. If square wave symmetry, measured at FUNC OUT, is out of specification and cannot be calibrated, refer to paragraph 6.3.10.
6. If none of the above conditions apply, refer to figure 6-1.

6.3.4 Square Wave Distorted or Missing

Improperly set controls:

1. SYM button depressed.
2. Excessive dc offset overdriving output amplifier.
3. Function switch improperly set to PULSE/BURST.
4. Incorrect PULSE/SQUARE OUTPUT button depressed.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If symmetry is not in specification and cannot be calibrated refer to paragraph 6.3.10.
4. If none of the above conditions apply, refer to figure 6-2.

6.3.5 Sine Wave Distorted or Missing

Improperly set controls:

1. SYM button depressed
2. Excessive dc offset overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Check the triangle for nonlinearity at FUNC OUT. If it is nonlinear, but only on one range, check for a leaky capacitor on that range. If the triangle is nonlinear on more than one range, check for a leaky capacitor or faulty active component in the frequency multiplier and triangle buffer circuits. (NOTE: Some nonlinearity above 200 kHz is normal and not specified.)
3. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.

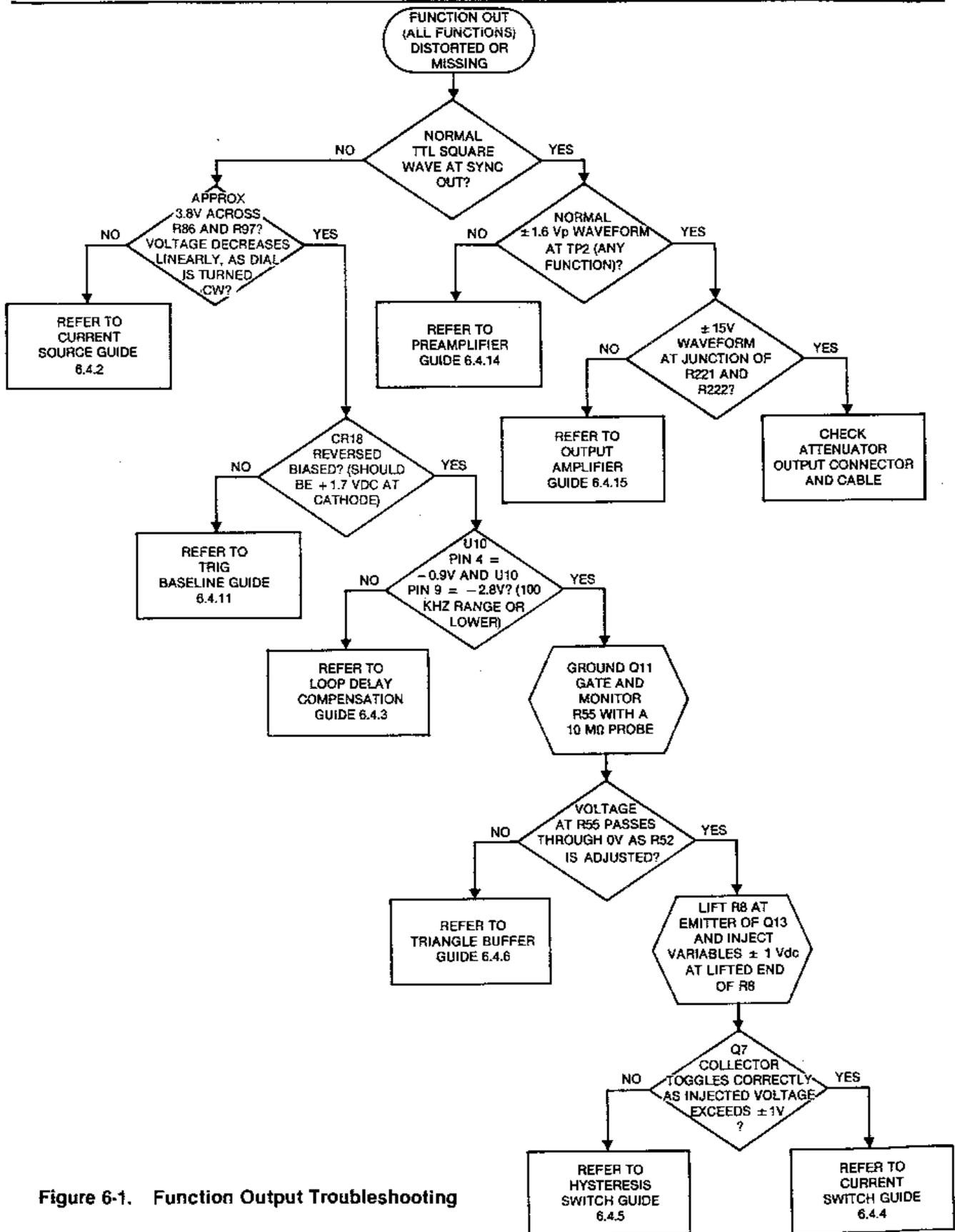


Figure 6-1. Function Output Troubleshooting

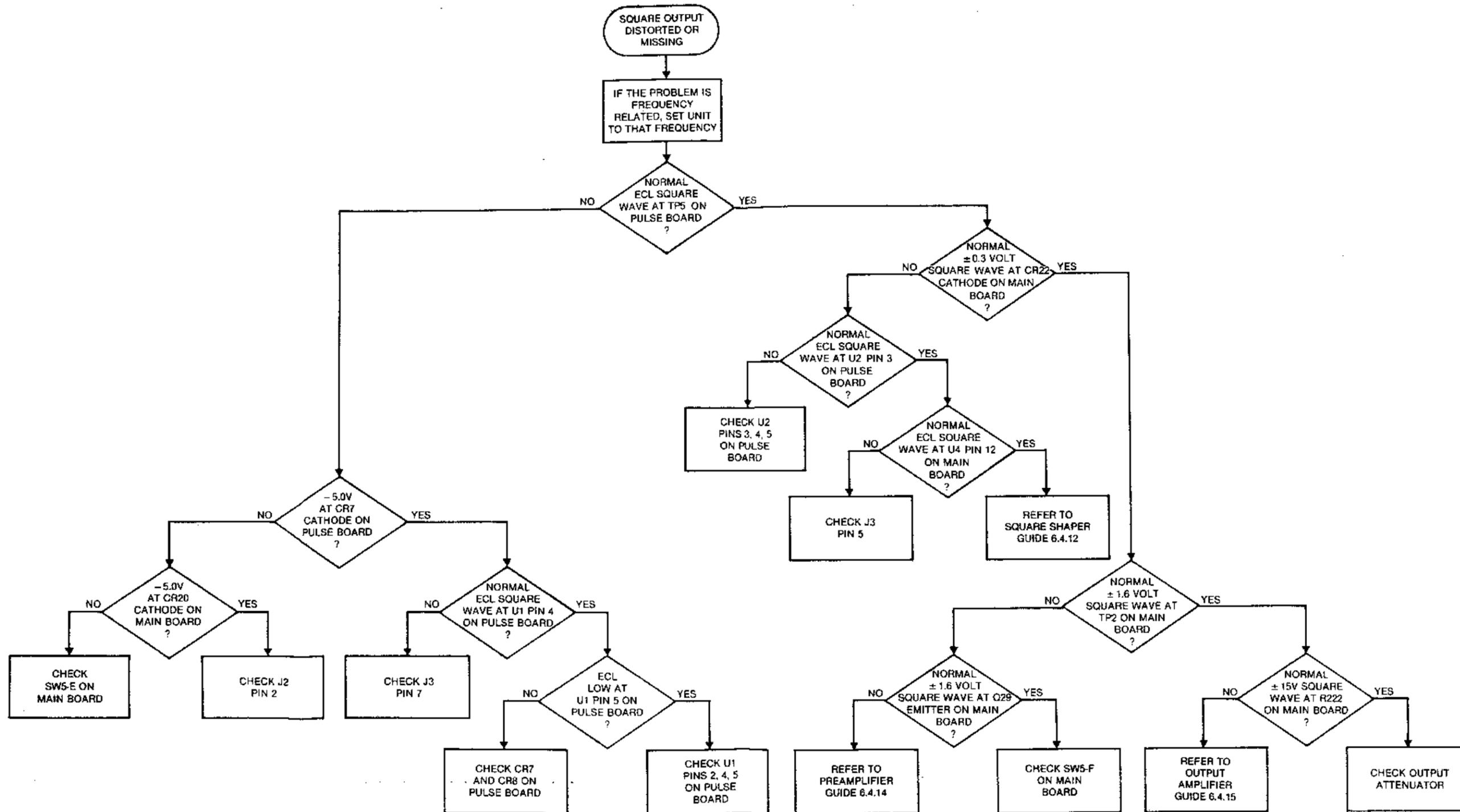


Figure 6-2. Square Output Troubleshooting

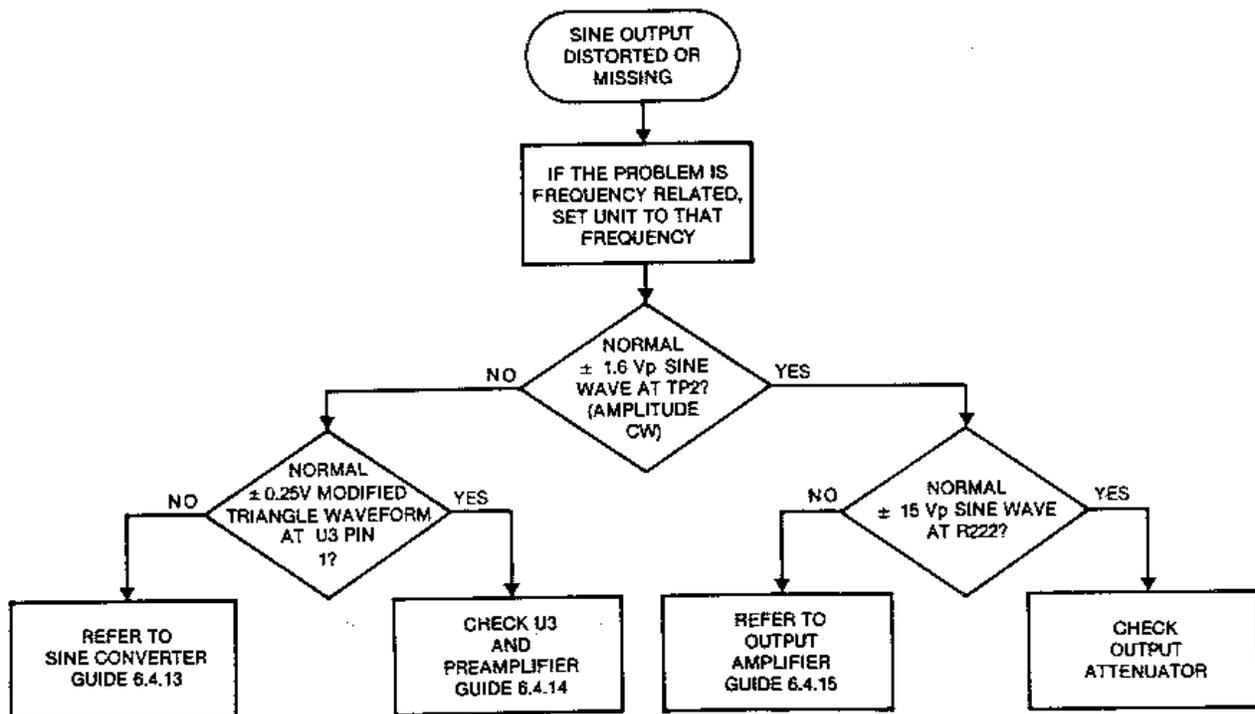


Figure 6-3. Sine Output Troubleshooting

4. Verify that square wave symmetry, at FUNC OUT, is in specification. If not and cannot be calibrated, refer to paragraph 6.3.10.
5. If none of the above conditions apply, refer to figure 6-3.

6.3.6 Triangle Distorted or Missing

Improperly set controls:

1. SYM button depressed.
2. Excessive dc offset overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Check the triangle for nonlinearity at FUNC OUT. If it is nonlinear, but only on one range, check for a leaky capacitor on that range. If the triangle is nonlinear on more than one range, check for a leaky capacitor or faulty active component in the frequency multiplier and triangle buffer circuits. (NOTE: Some nonlinearity above 200 kHz is normal and not specified.)
3. If the waveform is bad in one or more of the four

lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.

4. Verify square wave symmetry at FUNC OUT is in specification. If not and cannot be calibrated, refer to paragraph 6.3.10.
5. If none of the above conditions apply, refer to figure 6-4.

6.3.7 Sync Output Distorted or missing (FUNC OUT Normal)

Improperly set controls:

1. Because the FUNC OUT is normal, this cannot be caused by improperly set controls.

Functional block isolation:

1. If there is no ECL square wave at U6 pin 10, refer to paragraph 6.4.7. If there is an ECL square wave, refer to paragraph 6.4.8.

6.3.8 Excessive High Frequency Sine or Triangle Roll Off

Improperly set controls:

1. Excessive dc offset overdriving output amplifier.

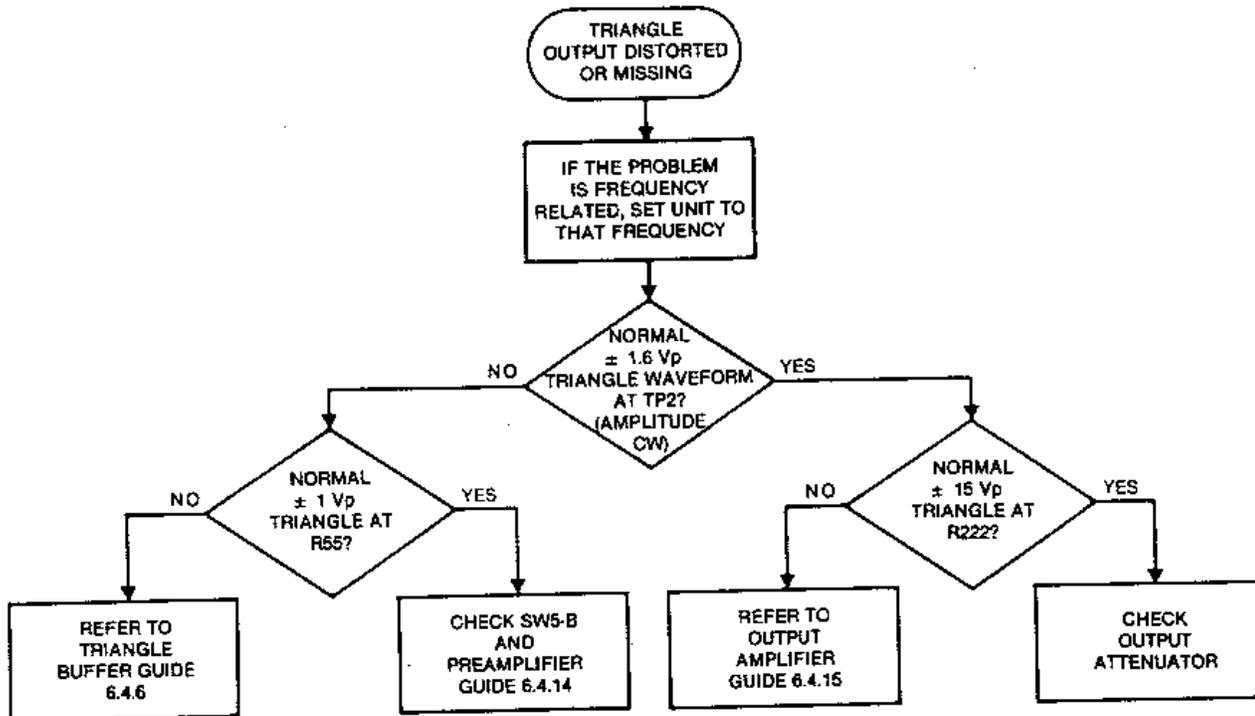


Figure 6-4. Triangle Output Troubleshooting

2. Verify 50Ω load on the cable at oscilloscope end.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal with less than 100 mVp-p of ac ripple. If not refer to paragraph 6.4.1. Use a X10 probe with a very short ground lead and a spectrum analyzer, RF voltmeter or a 200 MHz bandwidth scope when performing sine or triangle roll-off tests.
2. If none of the above conditions apply, refer to figure 6-5.

6.3.9 Low Frequency Square Wave Tilt

Improperly set controls:

1. Scope improperly set to ac.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, and less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1
2. If none of the above conditions apply, refer to figure 6-6.

6.3.10 Time Symmetry Cannot Be Adjusted To Within Specifications

Improperly set controls:

1. SYM button depressed.
2. Function switch improperly set to PULSE/BURST.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If symmetry is out of specification in one of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If symmetry is out of specification on FREQ MULT settings 1M or 10M only, refer to paragraph 6.4.3.
4. If the voltages across R86 and R97 are not equal (typically 3.8V, Freq Dial: 2.0 Freq Mult: 100K or less), refer to paragraph 6.4.2

6.3.11 Frequency Accuracy and Dial Response Problems

Improperly set controls:

1. SYM button depressed.
2. External signal connected to VCG in BNC.
3. VERNIER not in FREQ CAL position.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of

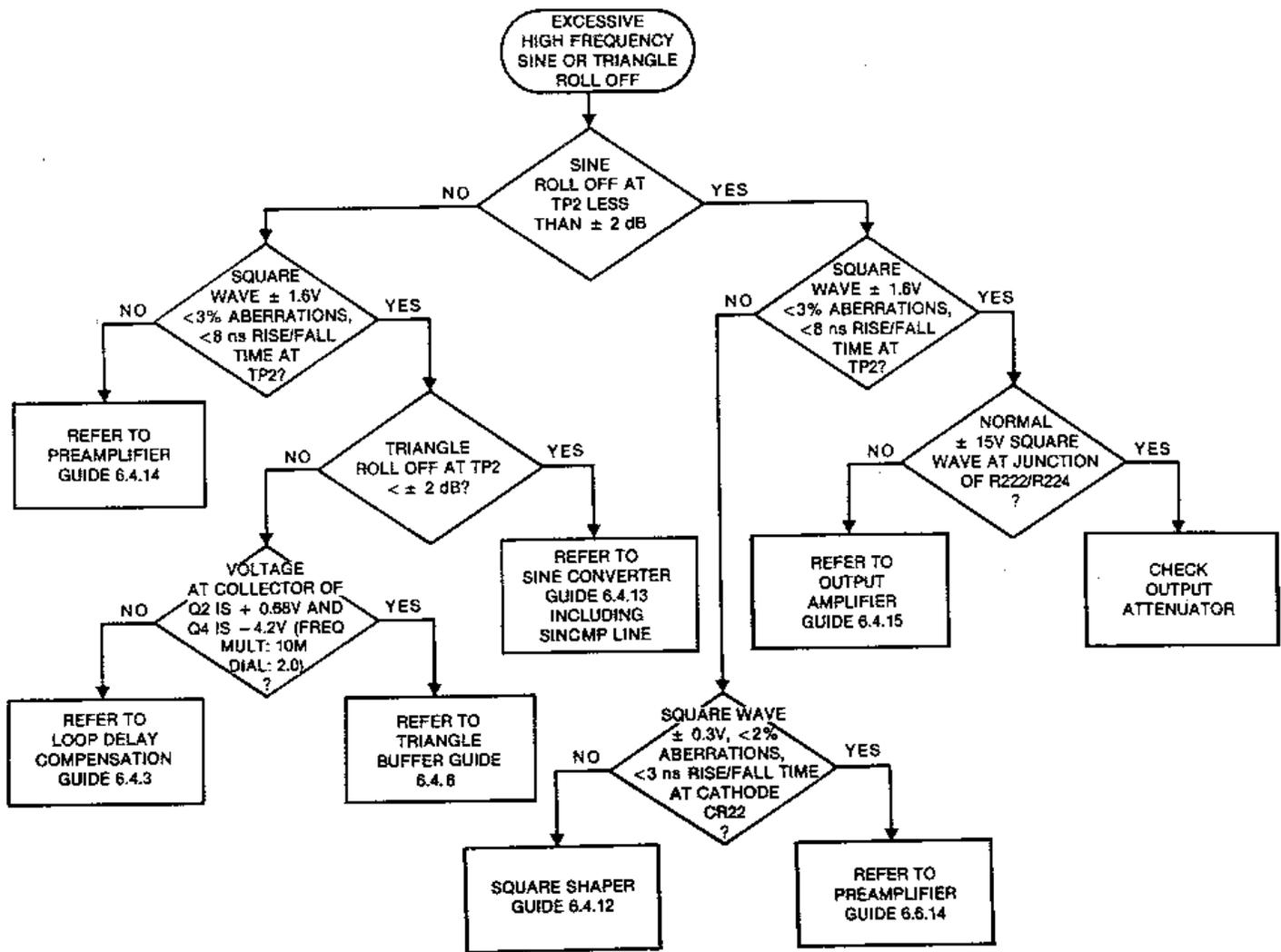


Figure 6-5. High Frequency Waveform Troubleshooting

nominal with less than 100 mVp-p ac ripple. If not, refer to paragraph 6.4.1.

2. If the problem occurs in one of the four lowest frequency ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If the frequency accuracy is out of specification on FREQ MULT settings 1M and 10M, refer to paragraph 6.4.3.
4. If the frequency is out of specification, but only on one range, check the range capacitor for that range.
5. If the problem occurs on the 1K, 10K, or 100K range, check the range capacitor.
6. On the 1K range and frequency dial set at 2.0, check for 3.8V across R86 and R97. As the dial is

rotated, this voltage should linearly track the dial settings within $\pm 3\%$ of full scale. If not, refer to paragraph 6.4.2.

7. If none of the above conditions apply, refer to figure 6-7.

6.3.12 Trigger, Gating and Trigger Baseline Problems

Improperly set controls:

1. MODE incorrectly set to other than TRIG (FUNC) or GATE (FUNC).
2. FUNCTION incorrectly set to DC or PULSE/BURST with improper PULSE DELAY or PULSE WIDTH settings.
3. DC OFFSET overdriving output amplifier.

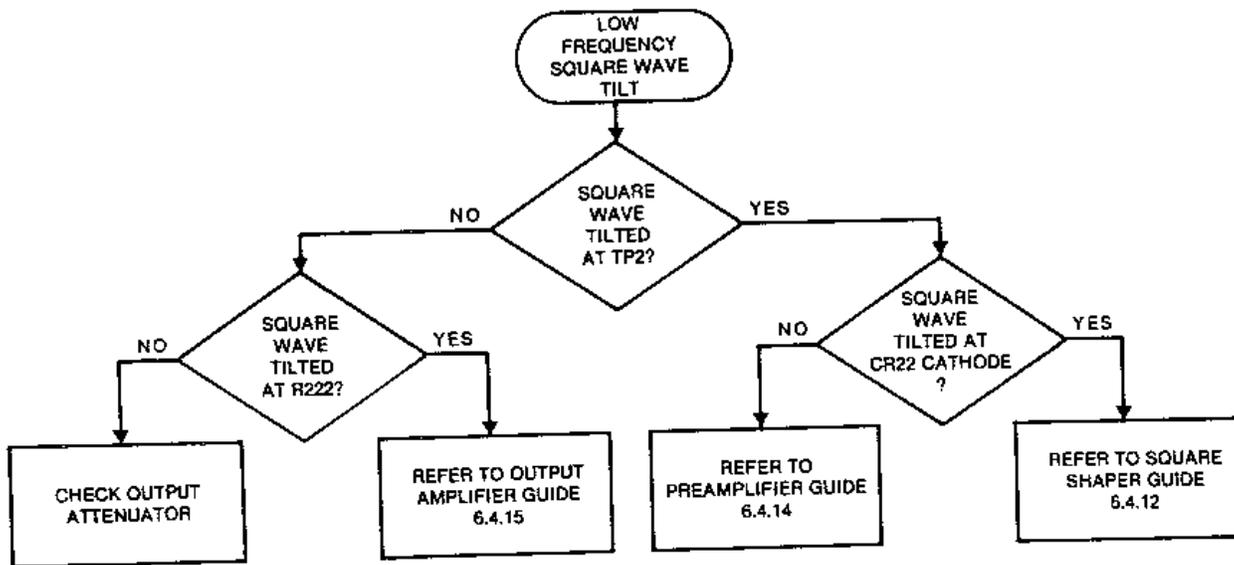


Figure 6-6. Low Frequency Square Wave Troubleshooting

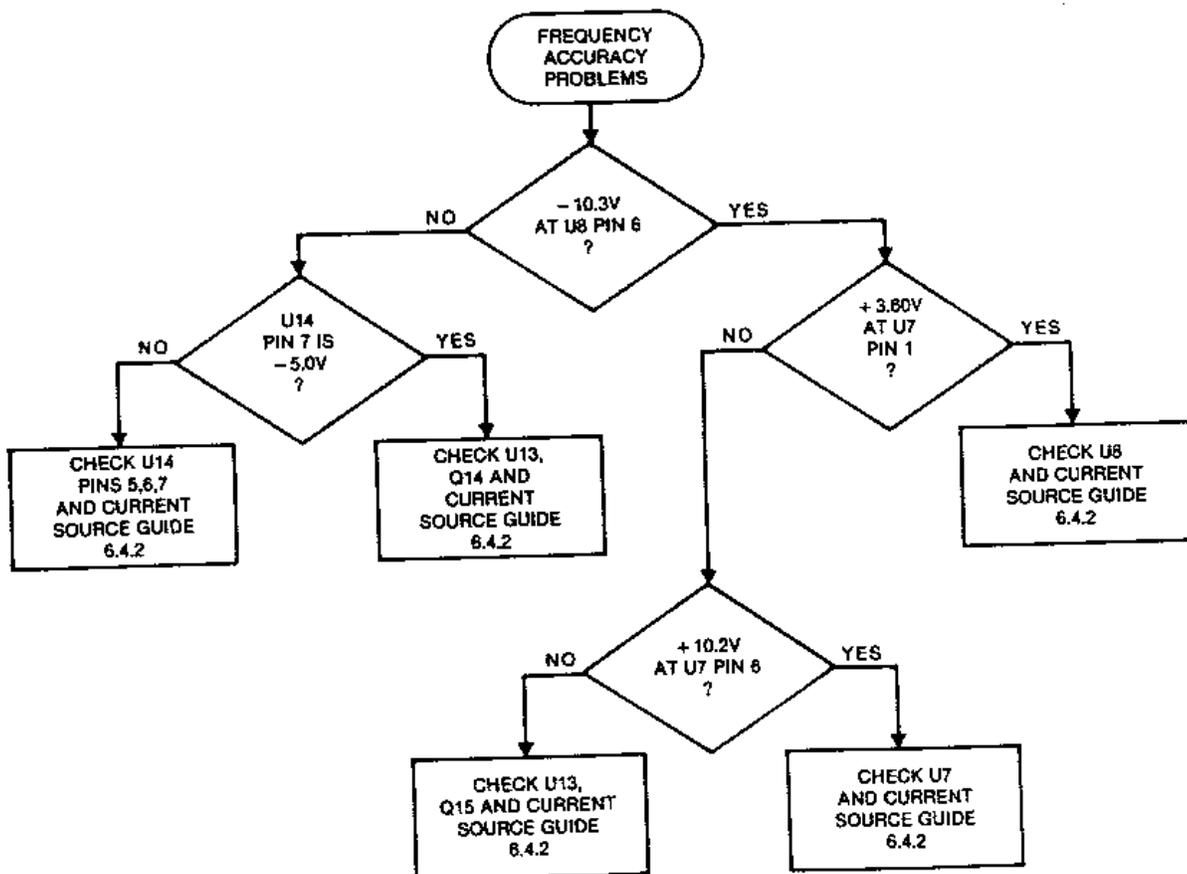


Figure 6-7. Frequency Accuracy Troubleshooting

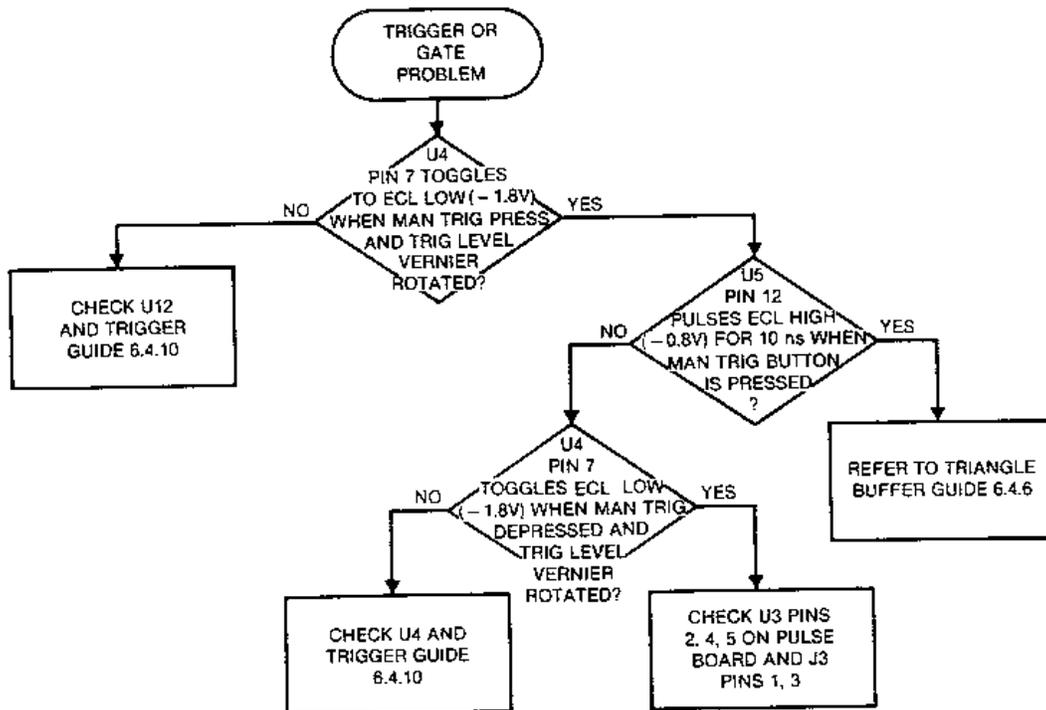


Figure 6-8. Trigger Gate Troubleshooting

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If the trigger baseline cannot be calibrated within specification, set MODE to GATE and monitor the emitter of Q19. With TRIG IN disconnected, rotate the TRIG LEVEL ccw. The voltage should go about -0.7 Vdc. Rotating the TRIG LEVEL cw should change this voltage to about $+1.8$ Vdc. If these voltage readings are normal, check CR18 and CR19.
3. If none of the above conditions apply, refer to figure 6-8.
4. For high frequency (1M and 10M ranges) trigger or gate problems, set the controls as follows:

Frequency Dial	2.0
FREQ MULT:	10M
SYM:	OFF
MODE:	TRIG or GATE (Depends on symptom- GATE preferred)
TRIG LEVEL:	12 o'clock

Set the scope as follows:

Horizontal:	20 ns/div
Vertical:	1 V/div

Inject a 15 MHz 1 Vp-p trigger signal and refer to figure 6-9.

6.3.13 Voltage At VCG IN Connector Not Changing Frequency Properly

Improperly set controls:

1. Excessive VCG IN voltage for dial setting (maximum input voltage is $+5.0$ Vdc with the dial set at .02 and the Freq VERNIER turned ccw).
2. Mode control improperly set to a BURST mode.

Functional block isolation:

1. Set the frequency dial to 2.0, FREQ MULT to 1K, and VCG IN with no input. Measure voltage across R86 and R97 ($+3.8$ Vdc). In addition, as the frequency dial is rotated, the voltage linearly tracks the dial settings within $\pm 3\%$ full scale. If it functions properly, check R67, R68, R69 and associated circuitry, but if not, refer to paragraph 6.3.11.

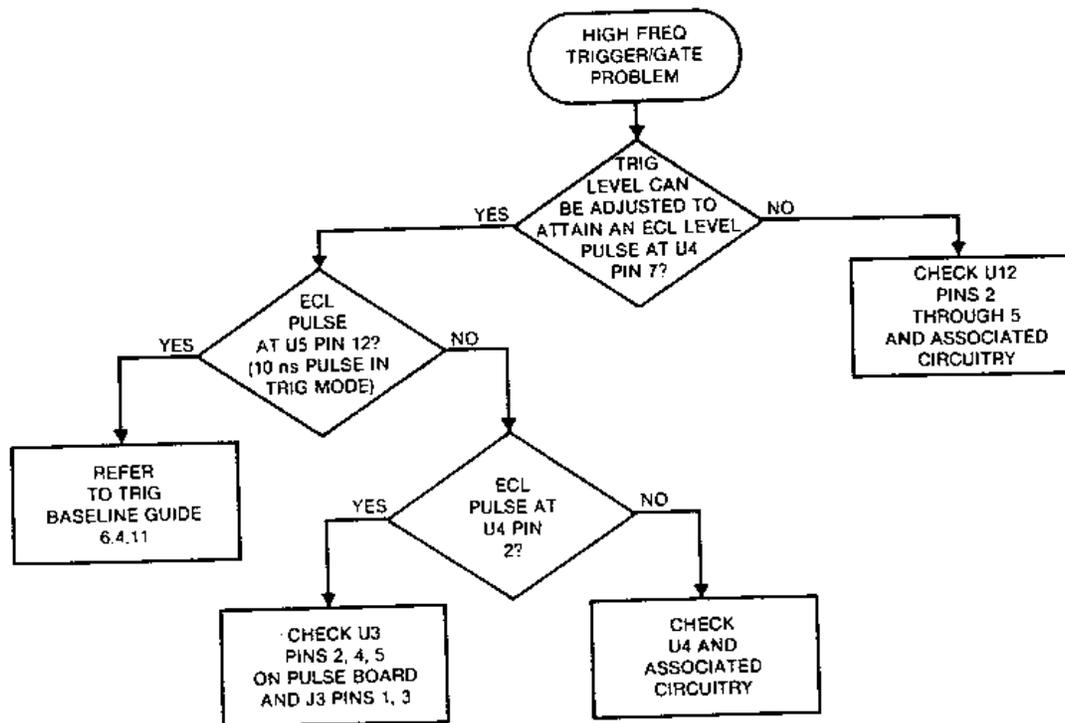


Figure 6-9. High Frequency Trigger/Gate Troubleshooting

6.3.14 DC Offset Not Functioning Correctly

Improperly set controls:

1. Signal peak plus offset exceeding + or - 7.5V (with a 50Ω load), or ± 15V open circuit.
2. Check OUTPUT ATTEN since this also attenuates output offset.

Functional block isolation:

1. Verify power supply voltages are within ±5% of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Take the following voltage measurements with the DC OFFSET button depressed and the DC OFFSET control rotated cw:
 - a) The junction of R260 and C116 should vary from +8.0V to -8.0V.
 - b) U2 pin 2 should hold at 0.0V.
 - c) U2 pin 6 should vary from -1.0V to +1.0V. (Drifting of this voltage is typical because of constant compensation by U2 of variations in output transistor currents.)

3. If none of the above conditions apply, refer to paragraph 6.4.15.

6.3.15 Variable Symmetry Problems

Improperly set controls:

1. SYM button is incorrectly extended.
2. Note: When SYM is depressed the output frequency should be one-tenth the selected frequency.
3. DC offset is overdriving the output amplifier.
4. Mode switch incorrectly set to a BURST mode.

Functional block isolation:

1. Verify power supply voltages within ±5% of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. When the voltage at the right leg of R88 (VERNIER/SYM CW) is -15V and when the voltage at the left leg of R88 (VERNIER/SYM CCW) is -15V, refer to paragraph 6.4.2. If not, check R88 and SW8.

6.4 CIRCUIT GUIDES

Circuit guides provide listings of voltage levels, waveforms, and hints that, when used with the schematics, are helpful in isolating faulty circuits. Table 6-2 is an index of circuit guides.

Table 6-2. Circuit Guide Index

Circuit Guide	Paragraph
Power Supply	6.4.1
Current Source	6.4.2
Loop Delay Compensation	6.4.3
Current Switch	6.4.4
Hysteresis Switch	6.4.5
Triangle Buffer	6.4.6
Zero Crossing Detector	6.4.7
Sync	6.4.8
Capacitance Multiplier	6.4.9
Trigger	6.4.10
Trig Baseline	6.4.11
Square Shaper	6.4.12
Sine Converter	6.4.13
Preamplifier	6.4.14
Output Amplifier	6.4.15

6.4.1 Power Supply Guide

- To determine a faulty power supply, check for the voltages given in table 6-3.

Table 6-3. Power Supply Checks

Supply	Voltage Tolerance	Maximum Regulator Input Ripple (p-p)	Maximum Regulator Output Ripple (p-p)
±15V Balance	30 ± 1.5 Vdc (a)	—	—
+15V	(b)	1.5 Vac	10 mV
-15V	(c)	1.5 Vac	10 mV
+5V	± 750 mV	1.5 Vac	10 mV
-5V	± 750 mV	1.5 Vac	10 mV
+23V	± 1.15 Vdc	1.5 Vac	10 mV
-23V	± 1.15 Vdc	1.5 Vac	10 mV

(a) Measured between +15V and -15V supplies.
 (b) Measure and note +15V supply (V_{+15}).
 (c) -15V supply = $-|V_{+15} \pm .01V|$.

- if the regulator input is bad, remove P5 and check for:
 - Shorted or open diodes (CR1, CR2, or CR3).
 - Shorted or open capacitors at the input of the regulator.
 - Short between the regulator metal mounting tab and chassis ground.
- If the regulator input is good, check for:
 - Shorted or open capacitors at the output of the regulator.
 - Short between regulator metal mounting tab and chassis ground.
 - Excessive loading by main board circuits; to verify, lift jumper of the appropriate supply.
 - If all of the above conditions appear normal, replace the voltage regulator.

6.4.2 Current Source Guide

Top of Dial Check: Set the controls as follows; then perform the checks in table 6-4.

Control	Setting
Frequency Dial	2.0
FREQ MULT	1K
VERNIER	FREQ CAL
SYM	Off (extended)
VCG IN	Disconnected

Table 6-4. Current Source Check (Top of Dial)

Test Point	Desired Results
U14 pin 7	- 5 ± .5 Vdc
U13 pins 1, 2	- 5 ± .5 Vdc
Measure across R83	+ 3.8 ± .38 Vdc
U8 pin 6	- 10.3 ± 1.03 Vdc
Measure across R84 and R93	+ 3.8 ± .38 Vdc
U13 pin 6	0 ± .01 Vdc
U7 pin 6	+ 10.2 ± 1.02 Vdc
Measure across R86 and R97	+ 3.8 ± .38 Vdc

VCG Check: Set the controls as follows; then perform the checks in table 6-5.

Control	Setting
Frequency Dial	.02
FREQ MULT	1K
VERNIER	Full ccw
SYM	Off (extended)
VCG IN	+5.0 Vdc input

Table 6-5. Current Source (VCG IN)

Test Point	Desired Results
U7 pin 6	+ 14.38 ± 1.44 Vdc
U8 pin 6 (disconnect VCG IN)	- 14.3 ± 1.43 Vdc

10 MHz Range Check: Set the controls as shown below, then perform the checks in table 6-6.

Control	Setting
Frequency Dial	2.0
FREQ MULT	10M
VERNIER	FREQ CAL
SYM	Off (extended)
VCG IN	Disconnected

Table 6-6. Current Source Check (10 MHz Range)

Test Point	Desired Results
Measure across R99	+ 5.9 ± .59 Vdc
Measure across R83	+ 6.05 ± .61 Vdc
U8 pin 6	- 8.2 ± .82 Vdc

Variable Symmetry Check: Set the controls as shown then measure the voltage across resistors R84, R85, R86, R87, R93, and R97. The measured voltages should read +0.38 ± .04V.

Control	Settings
Frequency Dial	2.0
VERNIER	12 o'clock position
VCG IN	Disconnected
FREQ MULT	1K
SYM	On (depressed)

6.4.3 Loop Delay Compensation Guide

Set the controls as shown; then perform the checks in table 6-7.

Controls	Settings
Frequency Dial	2.0
VERNIER	FREQ CAL
VCG IN	Disconnected
FREQ MULT	10M
SYM	Off (extended)

Table 6-7. Loop Delay Compensation Checks

Test Point	Desired Results
Q1 and Q2 emitters	+ 9.2 ± .92 Vdc
Q1 base and collector, Q2 base	+ 8.5 ± .9 Vdc
Q2 collector	+ 0.68 ± .07 Vdc
Q3 and Q4 emitter	- 9.05 ± .91 Vdc
Q3 and Q4 base Q3 collector	- 8.32 ± .83 Vdc
Q4 collector	- 4.2 ± .42 Vdc
U10 pin 4	- 1.6 ± .16 Vdc (+ Peak reference)
U10 pin 9	- 2.17 ± .22 Vdc (- Peak reference)

6.4.4 Current Switch Guide

Set the controls as shown; then take waveform measurements. Refer to figure 6-10.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off (extended)
MODE	CONT (FUNC)

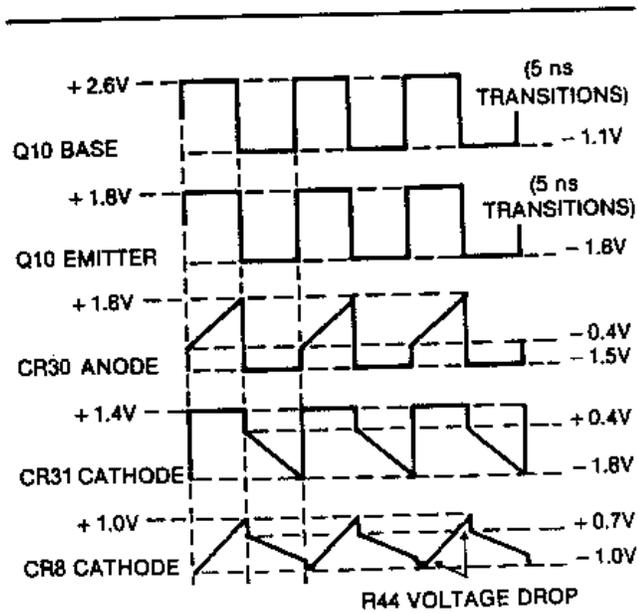


Figure 6-10. Current Switch Waveforms

6.4.5 Hysteresis Switch Guide

Set the controls as shown; then perform the checks in table 6-8, and take waveform measurements. Refer to figure 6-11.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT (FUNC)

Table 6-8. Hysteresis Switch Guide

Test Point	Desired Results
U10 pin 4	-0.9 ± .09 Vdc (+ Peak reference)
U10 pin 9	-2.8 ± .28 Vdc (- Peak reference)
Q7 and Q8 emitters	-3.0 ± .3 Vdc

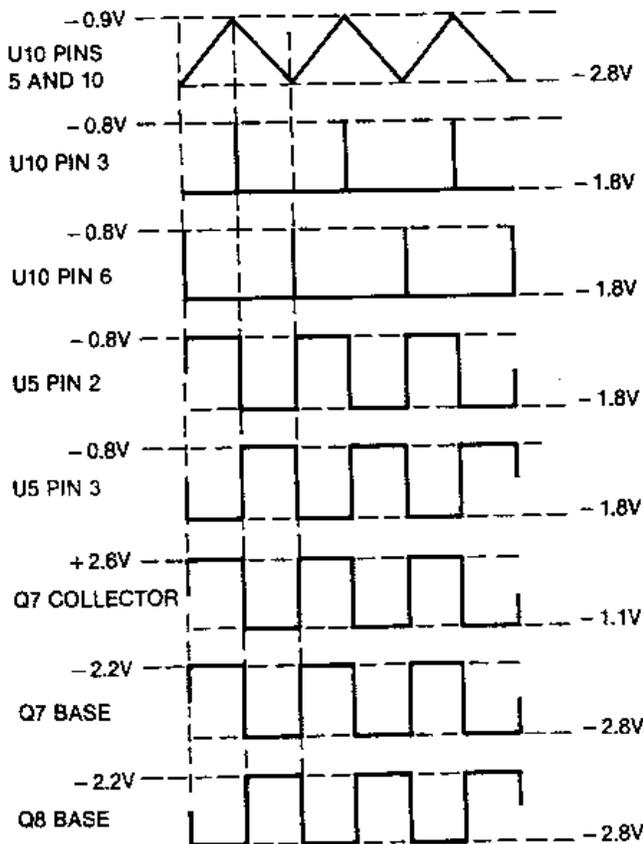


Figure 6-11. Hysteresis Switch Waveforms

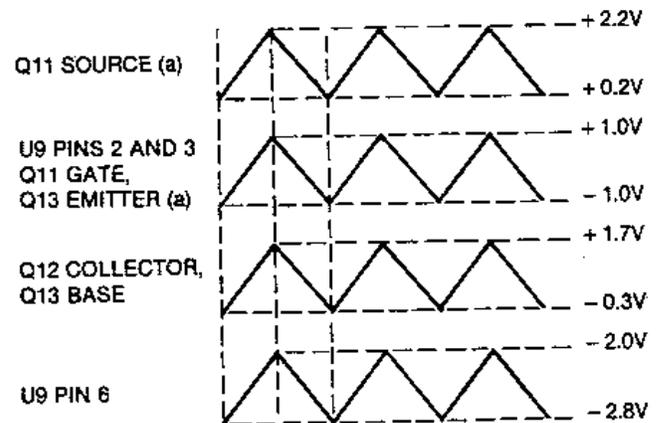
6.4.6 Triangle Buffer Guide

Set the controls as shown; then perform the checks in table 6-9 and take waveform measurements. Refer to figure 6-12. If, after setting the controls, the generator loop does not run, lift R45 at E23 and inject a ± 1.0V triangle into R45.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT (FUNC)

Table 6-9. Triangle Buffer Checks

Test Point	Desired Results
Q11 drain	+6.5 ± .65 Vdc
Q12 emitter	0.3 ± .03 Vp-p triangle, offset -10 ± 1 Vdc
Q12 base	0.3 ± .03 Vp-p triangle, offset -9.3 ± .9 Vdc
Q13 collector	+5.0 ± .5 Vdc



(a) Requires a X10 Probe (high impedance)

Figure 6-12. Triangle Buffer Waveforms

6.4.7 Zero Crossing Detector Guide

Set the controls as shown; then take waveform measurements. Refer to figure 6-13.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT (FUNC)

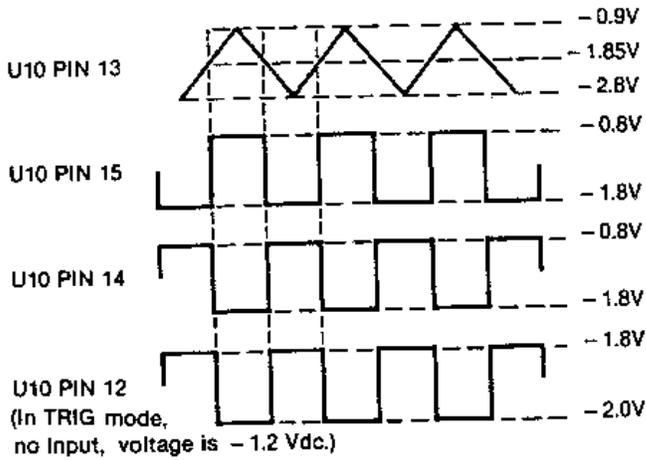


Figure 6-13. Zero Crossing Detector Waveforms

6.4.8 Sync Guide

Set the controls as shown then perform the checks in table 6-10 and take waveform measurements, see figure 6-14.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT (FUNC)

Table 6-10. Sync Check

Test Point	Desired Results	
	Function: Sine or Triangle Wave	Function: Square Wave
CR4 cathode	+1.2 ± .12 Vdc	-5 ± .5 Vdc
U6 pins 4 and 6	-1 ± .1 Vdc	-4.3 ± .43 Vdc
U6 pins 2 and 11	-1.8 ± .18 Vdc	-0.8 ± .08 Vdc
Q5/Q6 emitters	-1.6 ± .16 Vdc	-1.6 ± .16 Vdc

6.4.9 Capacitance Multiplier Guide

Set the controls as shown; then take the waveform measurements. Refer to figure 6-15.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	100
SYM	Off
MODE	CONT (FUNC)

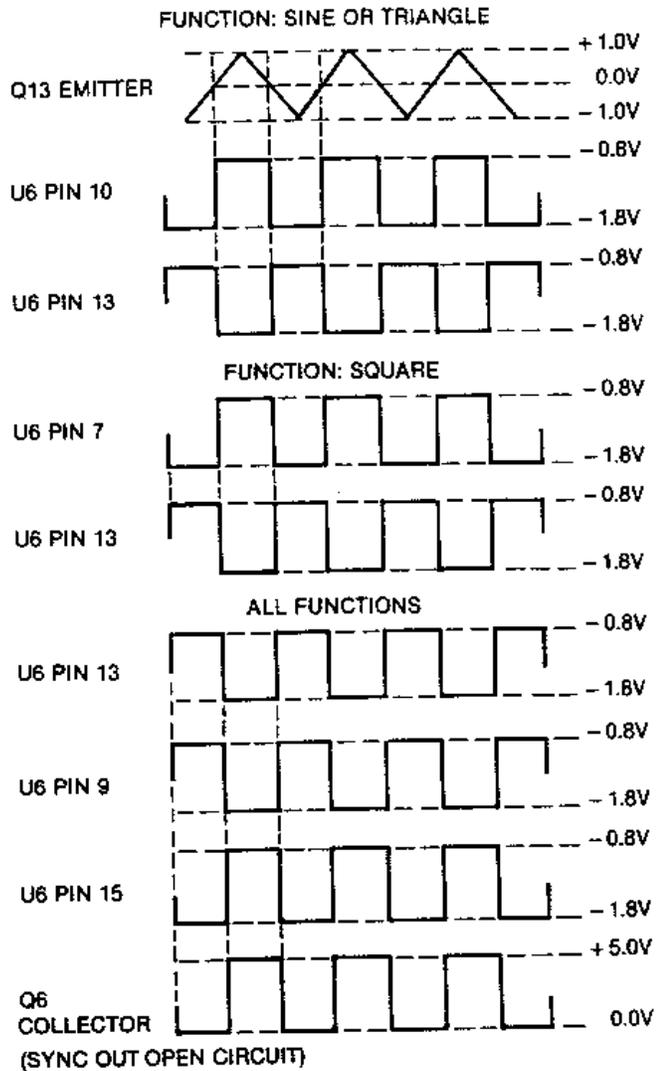


Figure 6-14. Sync Waveforms

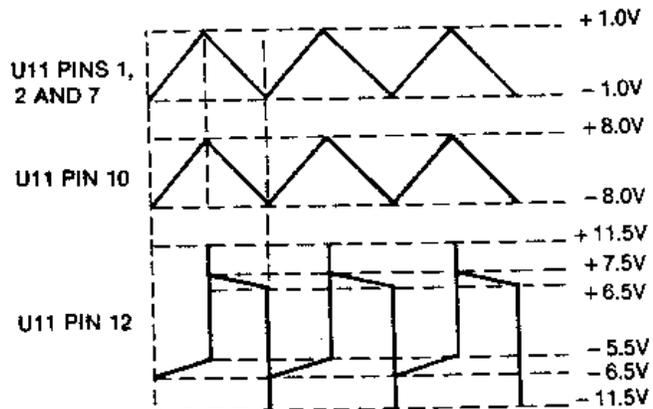


Figure 6-15. Capacitance Multiplier Waveforms

6.4.10 Trigger Guide

TRIG or CONT Check: Set the controls as shown; then take the waveform measurements. Refer to figure 6-16.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
MODE	TRIG (FUNC) or CONT (FUNC)
TRIG IN	$\pm 1V$ 1 kHz Square wave

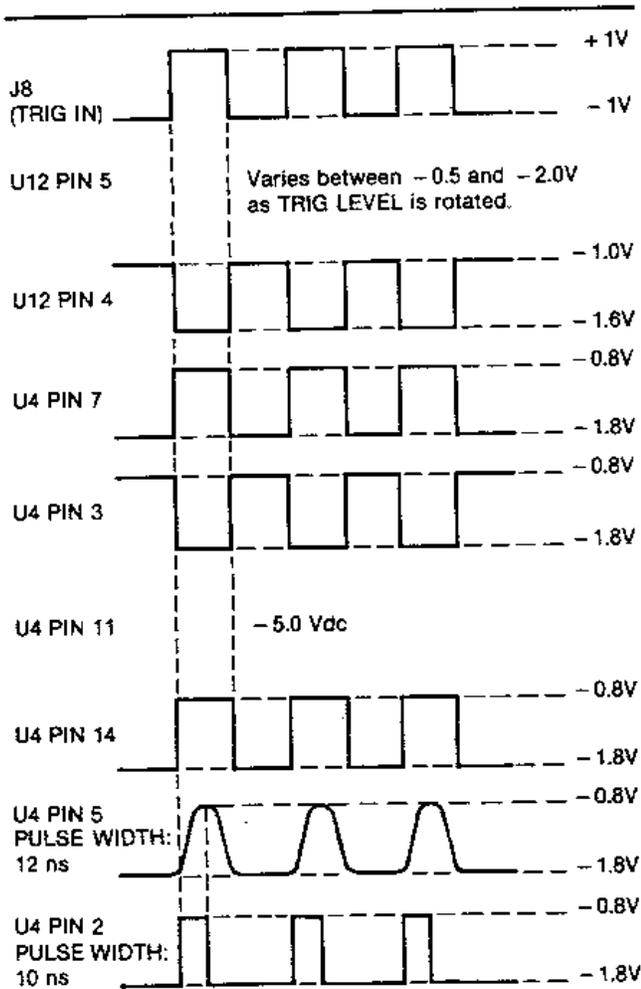


Figure 6-16. Trigger Waveforms (TRIG or CONT)

GATE Checks: Set the controls as shown; then take the waveform measurements. Refer to figure 6-17.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
MODE	GATE (FUNC)
TRIG IN	$\pm 1V$ 1 kHz Square wave

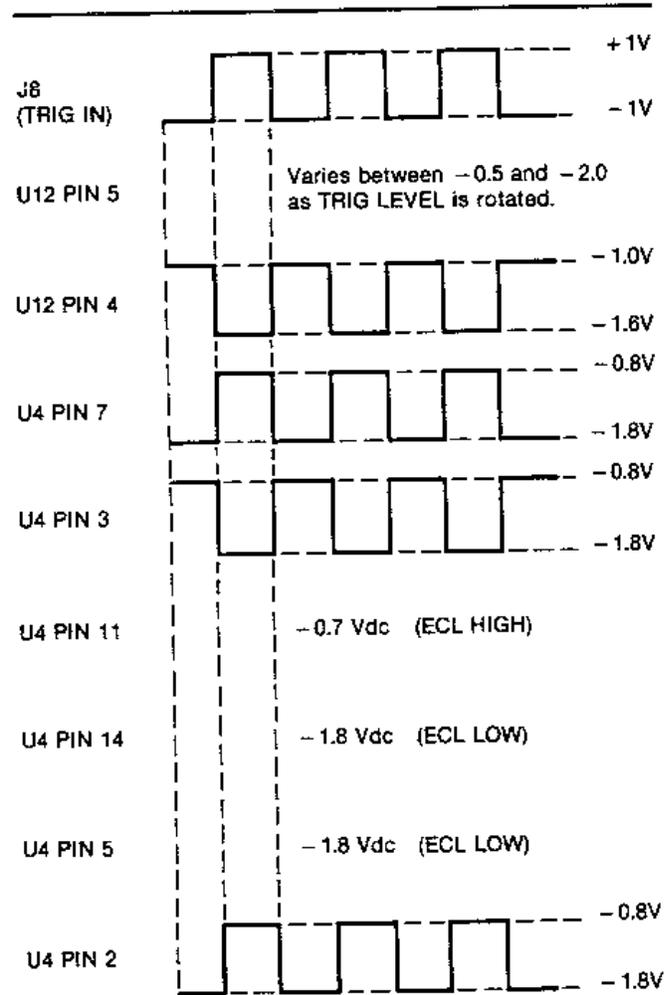


Figure 6-17. Trigger Waveforms (Gate)

6.4.11 Trigger Baseline Guide

Trigger or Gate Mode Problems: Set the controls as shown; then take the waveform measurements. Refer to figure 6-18.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	10K
SYM	Off
MODE	TRIG (FUNC) or GATE (FUNC) (Depends on symptom—GATE (FUNC) preferred)
TRIG LEVEL	Approximately centered
TRIG IN	$\pm 1V$ 10 kHz Square wave

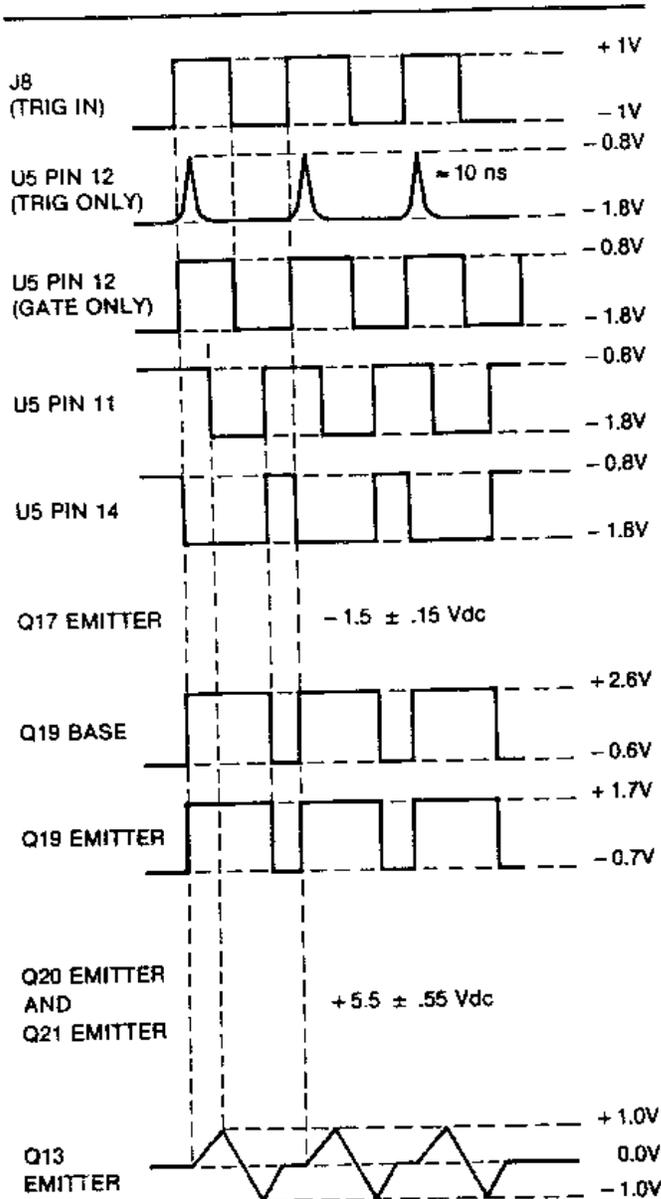


Figure 6-18. Trigger Baseline Waveforms

Continuous FUNCTION Mode Problems: Set the controls as shown; then take the waveform measurements. Refer to table 6-11.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	10K
SYM	Off
MODE	CONT (FUNC)

Table 6-11. Trigger Baseline Check (Continuous)

Test Point	Desired Results
U5 pin 12	-0.8 ± .08 Vdc
U5 pin 14	-1.8 ± .18 Vdc
Q17 emitter	-1.5 ± .15 Vdc
Q19 base	+2.6 ± .26 Vdc
Q19 emitter	+1.7 ± .17 Vdc
Q20 emitter	+5.5 ± .55 Vdc
Q21 emitter	+5.5 ± .55 Vdc
Q13 emitter	±1.0V triangle

6.4.12 Square Shaper Guide

Set the controls as shown; then perform the checks in table 6-12 and take waveform measurements. Refer to figure 6-19.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT (FUNC)
FUNCTION	See Table 6-12 and Fig 6-19

Table 6-12. Square Shaper Checks

Test Point	Desired Results	
	Sine or Triangle	Square
Q22 emitter	-3.0 ± .3 Vdc	-3.0 ± .3 Vdc
U4 pin 13	-0.8 ± .08 Vdc	-4.3 ± .43 Vdc
Q26 base	-0.8 ± .08 Vdc	-4.2 ± .42 Vdc
Q26 emitter	-1.6 ± .16 Vdc	-4.0 ± .4 Vdc
CR24 anode	+1.6 ± .16 Vdc	-1.5 ± .15 Vdc

6.4.13 Sine Converter Guide

Set the controls as shown; then perform the checks in table 6-13 and take waveform measurements. Refer to figure 6-20.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT (FUNC)
FUNCTION	Sine

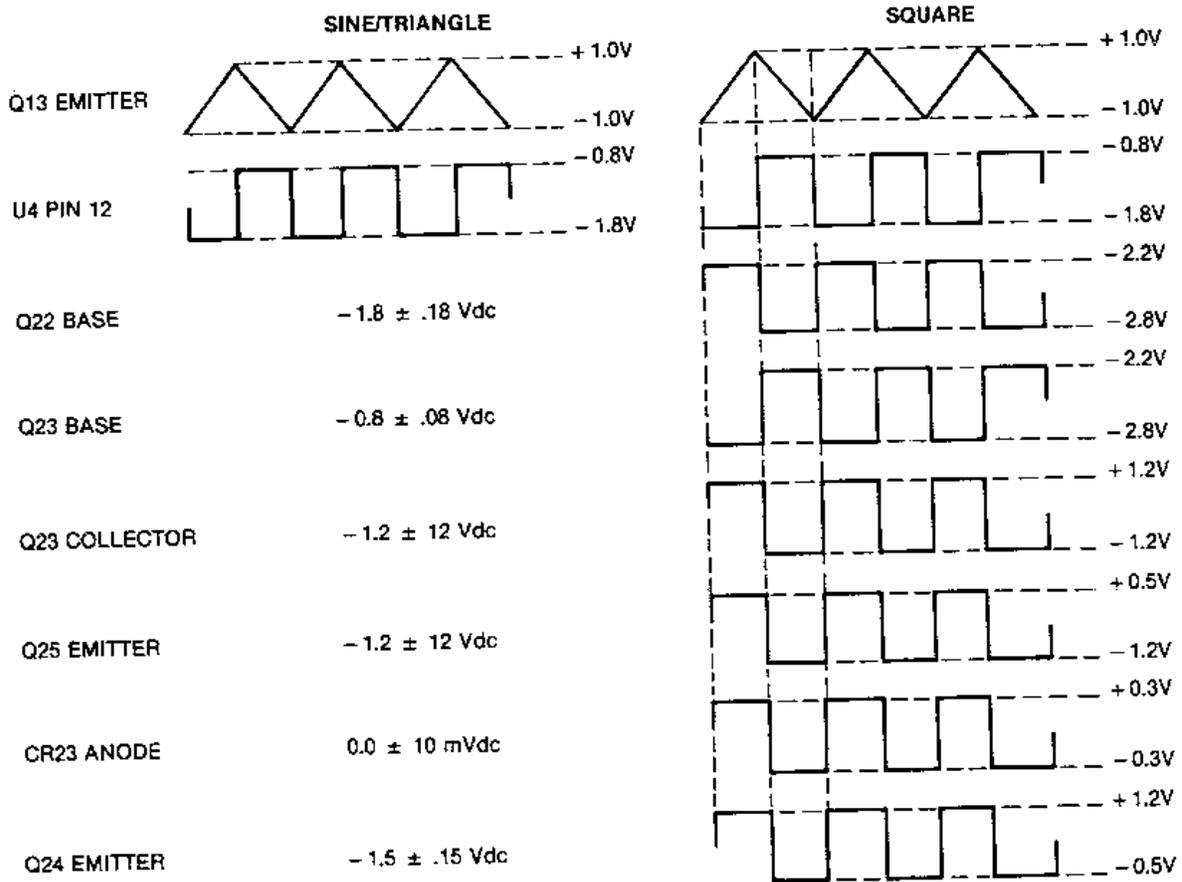


Figure 6-19. Square Shaper Waveforms

Table 6-13. Sine Converter Checks

Test Point	Desired Results
Junction R170 and R171	$+14.8 \pm 1.5$ Vdc
Junction R173 and R174	-14.8 ± 1.5 Vdc
U3 pin 2	0.0V (Full scale current = 2 mA)

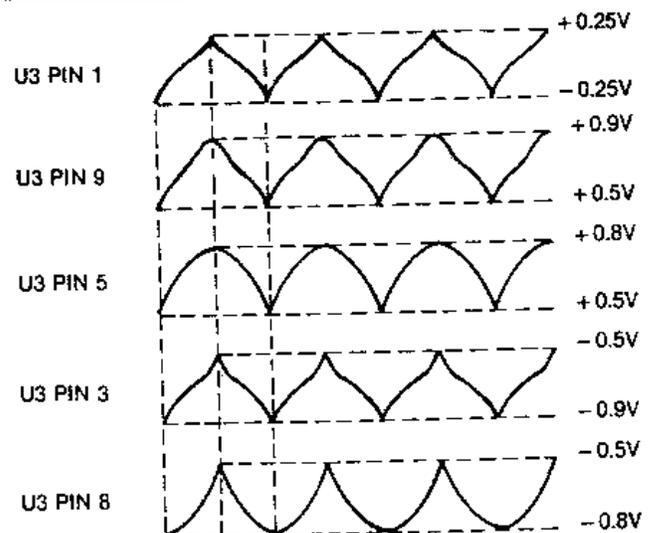


Figure 6-20. Sine Converter Waveforms

6.4.14 Preampifier Guide

DC Problems: Set the FUNCTION control to DC; then perform the checks in table 6-14.

Table 6-14. Preampifier Checks (DC)

Test Point	Desired Results
U1 pin 2	+14.86 ± 1.5 Vdc
U1 pin 3	-0.7 ± .07 Vdc
U1 pin 13	-1.4 ± .14 Vdc
U1 pin 9	-0.7 ± .07 Vdc
U1 pin 4	0.0 ± 10 mV
U1 pin 8	0.0 ± 10 mV
U1 pin 12	+5.8 ± .58 Vdc
U1 pin 11	+6.6 ± .66 Vdc
Q27 base	+9.6 ± .96 Vdc
Q27 emitter	+10.3 ± 1 Vdc
Q28 collector	+11.3 ± 1.1 Vdc

Function Problems: Set the controls as shown; then take the waveform measurements. Refer to figure 6-21.

Controls	Settings
Frequency Dial	2.0
FREQ MULT	1K
SYM	Off
MODE	CONT (FUNC)
FUNCTION	Square

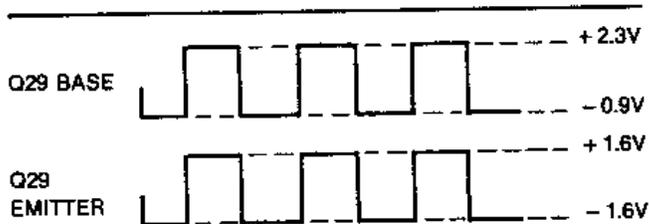


Figure 6-21. Preampifier Waveforms

6.4.15 Output Amplifier Guide

Set the controls as shown; then take the waveform measurements. Refer to table 6-15.

Controls	Settings
FUNCTION	DC
DC OFFSET	Off

Table 6-15. Output Amplifier Checks

Test Point	Desired Results
Base	+11.7 ± 1.2 Vdc
Q30 Emitter	+11 ± 1.1 Vdc
Collector	+19 ± 1.9 Vdc
Q32 Collector	+22.8 ± 2.3 Vdc
Base	-12 ± 1.2 Vdc
Q31 Emitter	-11.3 ± 1.1 Vdc
Collector	-19 ± 1.9 Vdc
Q33 Collector	-22.7 ± 2.3 Vdc
Base	+18.3 ± 1.8 Vdc
Q36 Emitter	+19 ± 1.9 Vdc
Collector	+0.7 ± .07 Vdc
Q37 Emitter	+0.05 ± .003 Vdc
Collector	+22.5 ± 2.3 Vdc
Q38 Emitter	+0.05 ± .005 Vdc
CR27 Cathode	+23 ± 2.3 Vdc
Anode	+0.6 ± .06 Vdc
VR5 Input	+31 ± 3.1 Vdc
Output	+24 ± 2.4 Vdc
Q34 Collector	+22.8 ± 2.3 Vdc
Base	-18.3 ± 1.8 Vdc
Q39 Emitter	-19 ± 1.9 Vdc
Collector	-0.05 ± .005 Vdc
Q40 Emitter	-0.05 ± .005 Vdc
Collector	-21 ± 2.1 Vdc
Q41 Emitter	-0.05 ± .005 Vdc
CR28 Anode	-23 ± 2.3 Vdc
Q35 Base	-0.6 ± .06 Vdc
IN	-31 ± 3.1 Vdc
VR6 ADJ	-21.3 ± 2.1 Vdc
OUT	-23.6 ± 2.4 Vdc
U2 Pin 2	0.0 ± 10 mVdc
Pin 6	-0.05 ± .005 Vdc

6.5 PULSE BOARD TROUBLESHOOTING

The easiest method of isolating pulse board problems is to use the front panel switches. To begin, set the controls as shown in table 6-16. If the malfunction is present, go to figures 6-22 and 6-23. If the malfunction is not present, begin pressing the switches listed in table 6-17 until the malfunction occurs. Use the figure or table referenced to further isolate and solve the problem.

Figures 6-22 through 6-33 and table 6-19 are directly related to switch positions. Most figures associated with the switch positions are simplified schematics, timing diagrams, or troubleshooting charts.

The simplified schematics are provided as aids because of the complicated logic switching of the pulse board. These schematics use solid-heavy lines to indicate signal flow, and dashed-heavy lines to indicate logic control lines. Rectangles represent circuit blocks, most of which are covered in figures 6-34 through 6-44. See table 6-18 for a listing of these figures. Those blocks not covered are simple circuits and are shown on the schematics in the rear of this manual.

Table 6-16. Initial Settings

Controls	Settings
Frequency Dial	2.0
PULSE DELAY/BURST RATE	10K/1K
VERNIER	ccw
PULSE	NORM
PULSE WIDTH/BURST WIDTH	10 μ s/100 μ s
VERNIER	ccw
INV	Extended (noninverted)
PULSE/SQUARE OUTPUT	
FREQ MULT	10K
VERNIER/SYM	FREQ CAL (cw)
SYM	Extended (VERNIER selected)
MODE	CONT (FUNC)
TRIG LEVEL	ccw
FUNCTION	PULSE/BURST
DC OFFSET button	Extended (off)
OUTPUT ATTEN	All extended (0 dB)
AMPLITUDE	MAX (cw)

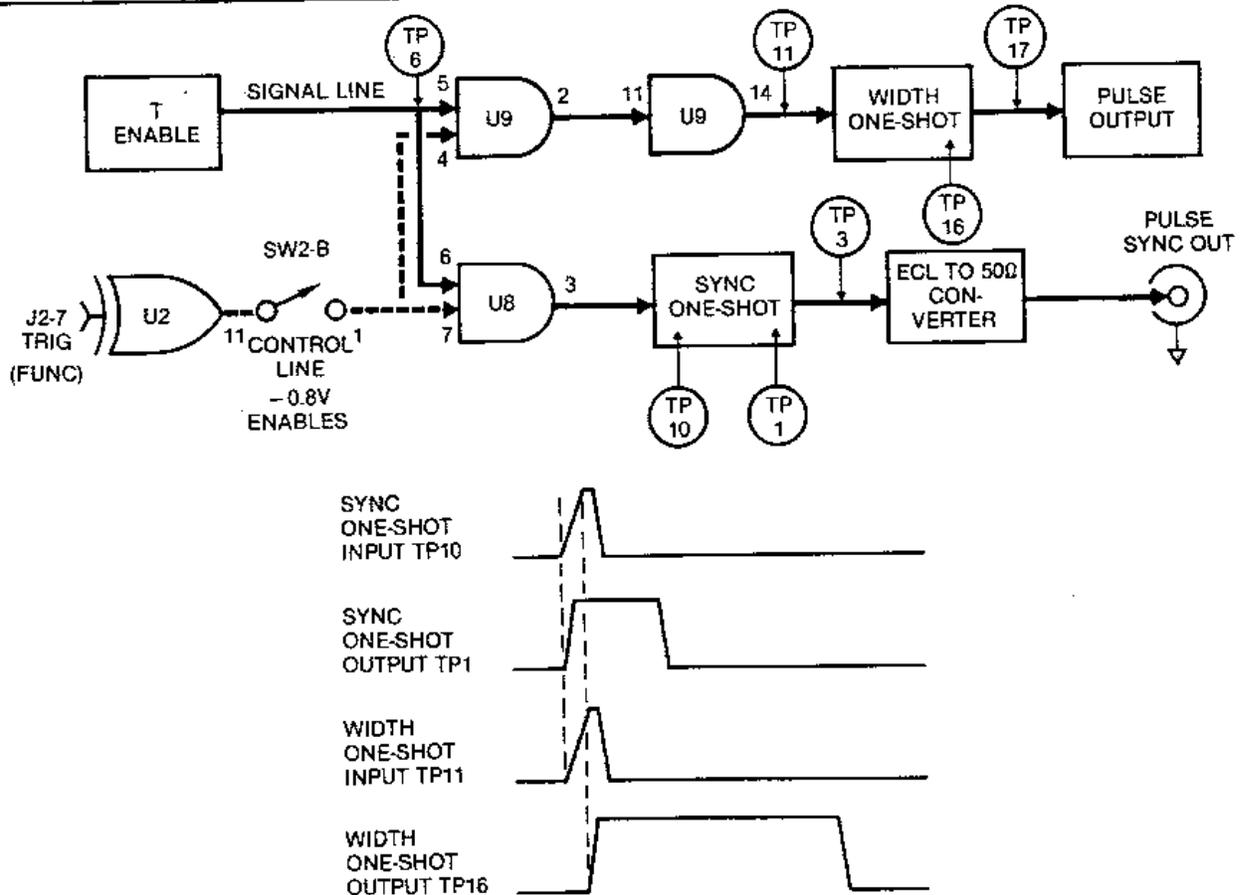


Figure 6-22. Pulse-norm Block and Timing Diagram

Table 6-17. Pulse Board Problem Switch Position

Controls	Figure	Table	Paragraph
PULSE: NORM	6-22 and 6-23		
PULSE DLY	6-24 and 6-25		
DBL PULSE	6-26 and 6-27		
SYNC DLY	6-28 and 6-29		
FUNCTION: PULSE	6-22 and 6-23		6.3.4
MODE: FUNC: CONT	6-22 and 6-23		
TRIG	6-30 and 6-31		
GATE	6-22 and 6-23		
BURST: CONT	6-32 and 6-33		
TRIG	6-32 and 6-33		
GATE	6-32 and 6-33		
PULSE/SQUARE OUTPUT:		6-19	
		6-19	
		6-19	
INV		6-19	
OUTPUT: PULSE/SQUARE OUT		6-19	
PULSE SYNC OUT		6-19	
FUNC OUT (FUNCTION:)		6-19	

Table 6-18. Circuit Block Figures

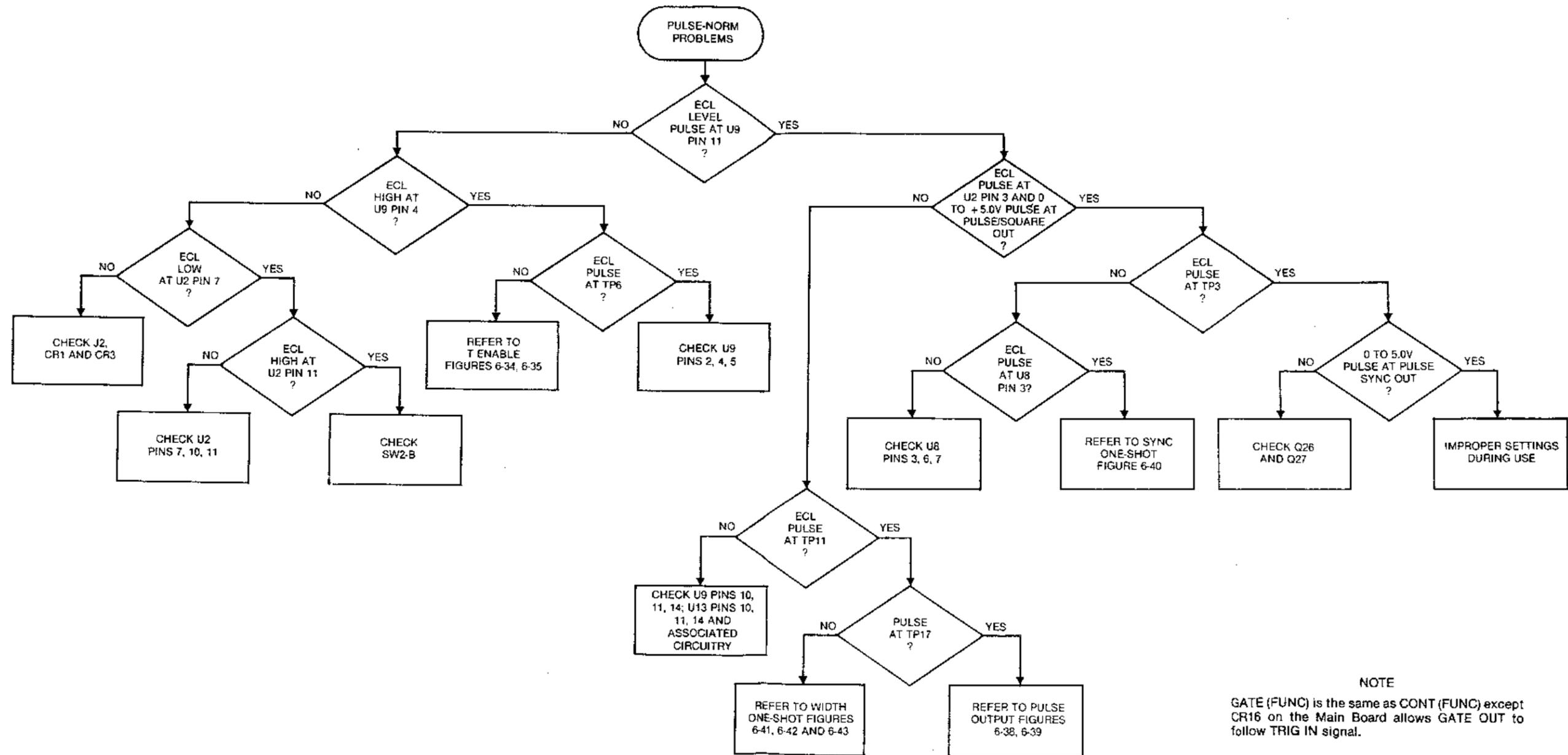
Title	Figure
T Enable Block Diagram	6-34
T Enable Troubleshooting	6-35
$\overline{\text{DLY}}$ Enable Block Diagram	6-36
$\overline{\text{DLY}}$ Enable Troubleshooting	6-37
Pulse Output Block Diagram	6-38
Pulse Output Troubleshooting	6-39
Sync One-Shot Troubleshooting	6-40
Width One-Shot Troubleshooting	6-41
Width One-Shot Current Source Troubleshooting	6-42
Width One-Shot Timing Diagram	6-43
Delay One-Shot Troubleshooting	6-44
Delay One-Shot Timing	6-45

Table 6-19. PULSE/SQUARE OUTPUT Checks

Before performing the following checks, set the controls as shown.

Control	Settings
Frequency	2.0
FREQ MULT	1K
SYM	Extended (off)
MODE	CONT (FUNC)
FUNCTION	\square or PULSE
PULSE/SQUARE OUTPUT	Set to position for malfunction. See table below.

Switch Position for Malfunction	Check
\square	SW9-A/B, J2 pin 9, See paragraph 6.4.12
\square	SW8-A/B, J1 pin 10, See paragraph 6.4.12
\square	SW10-A/B, J2 pins 9 and 10, See paragraph 6.4.12
INV (trigger on SYNC OUT)	SW7-A/B, CR13, U2 pins 3, 4, 5.
FUNCTION- \square	J2 pin 2, CR12.
FUNCTION-PULSE	J2 pin 1, CR11.



NOTE
 GATE (FUNC) is the same as CONT (FUNC) except CR16 on the Main Board allows GATE OUT to follow TRIG IN signal.

Figure 6-23. Pulse-Norm Troubleshooting

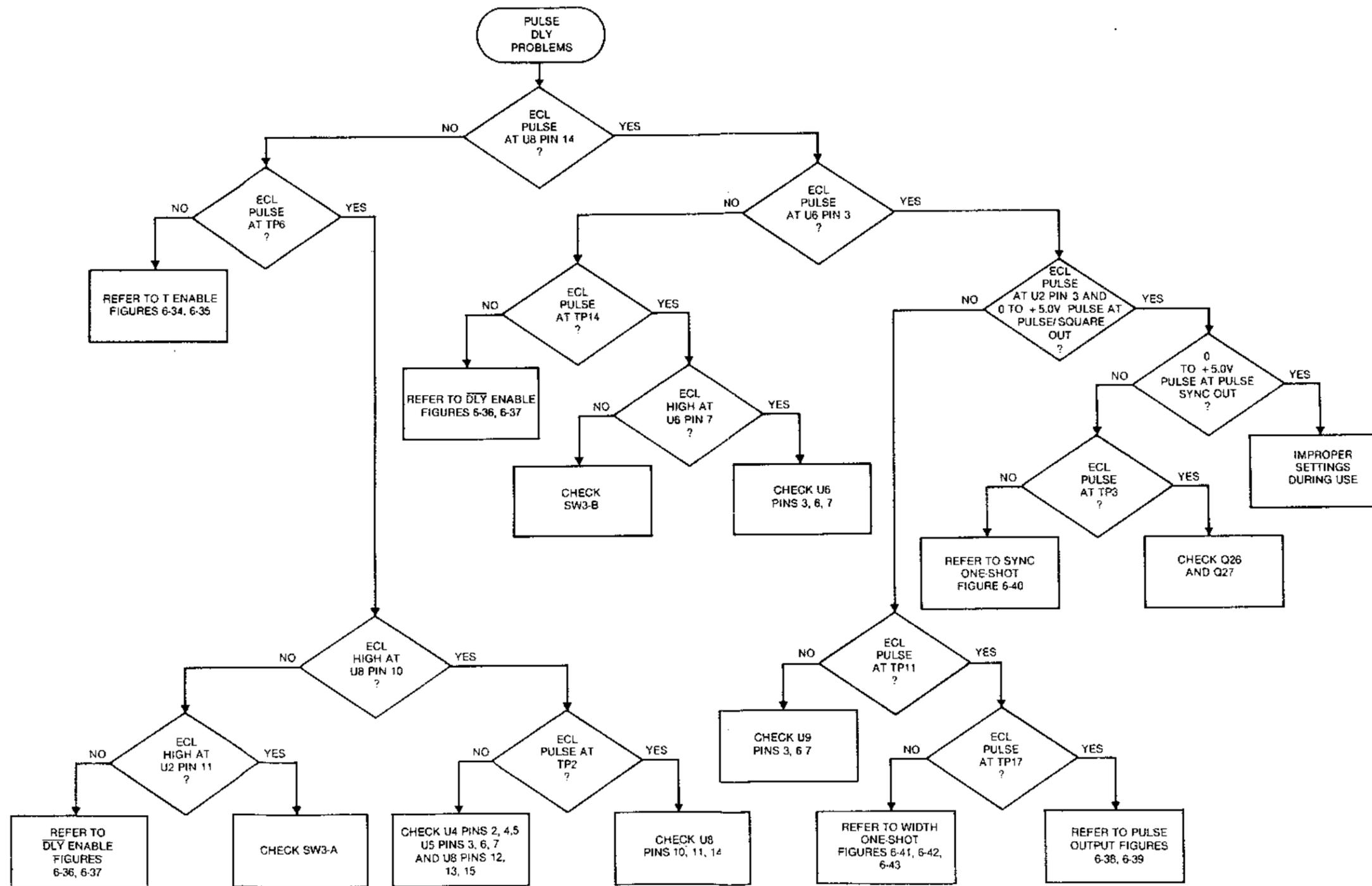


Figure 6-25. Pulse Dly Troubleshooting

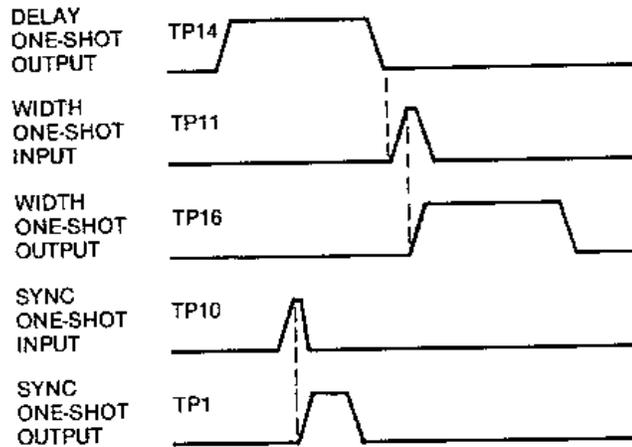
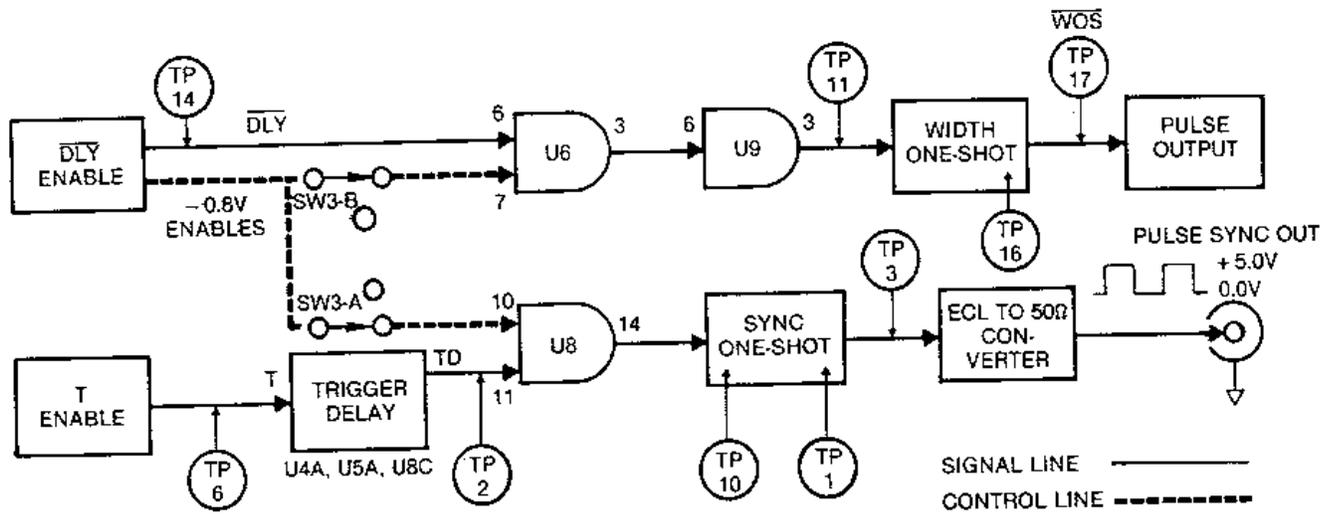


Figure 6-24. Pulse Dly Block and Timing Diagram

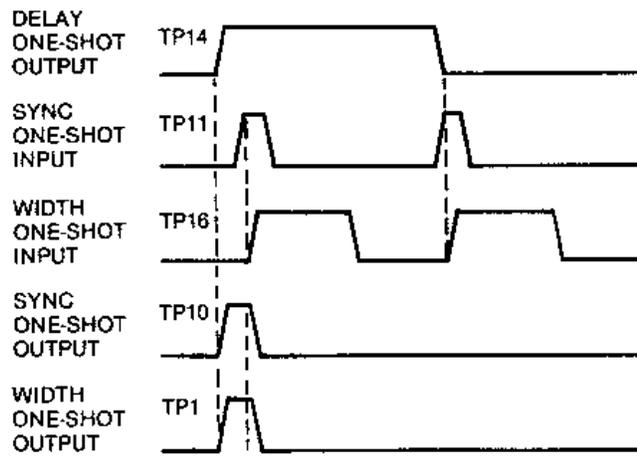
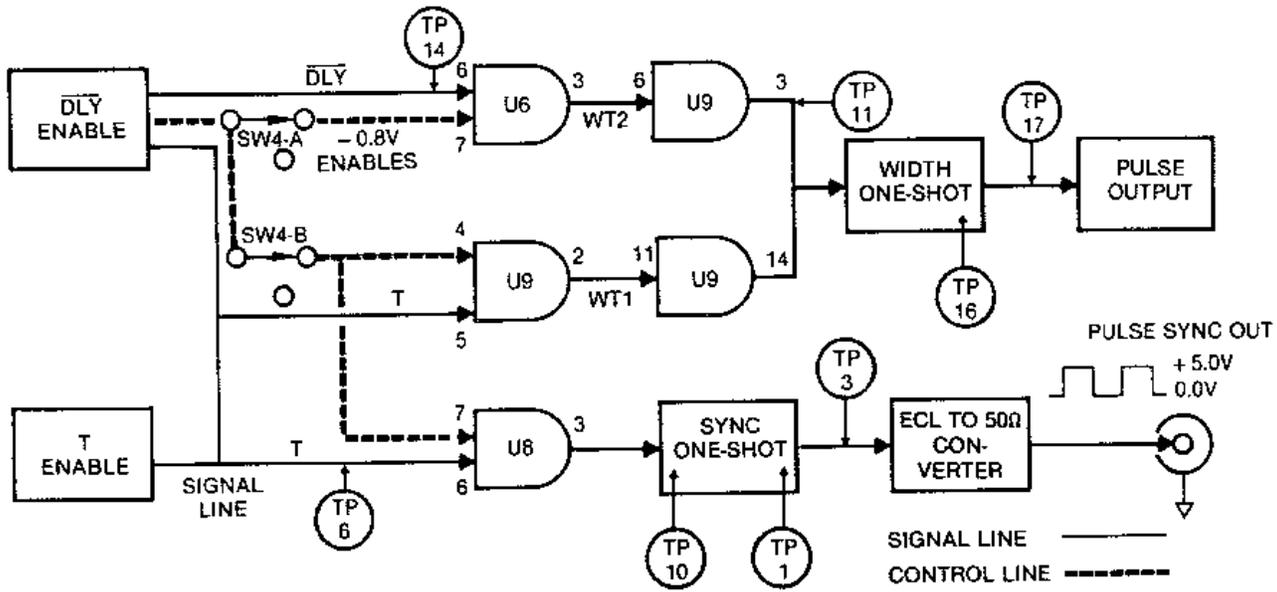


Figure 6-26. Dbl Pulse Block and Timing Diagram

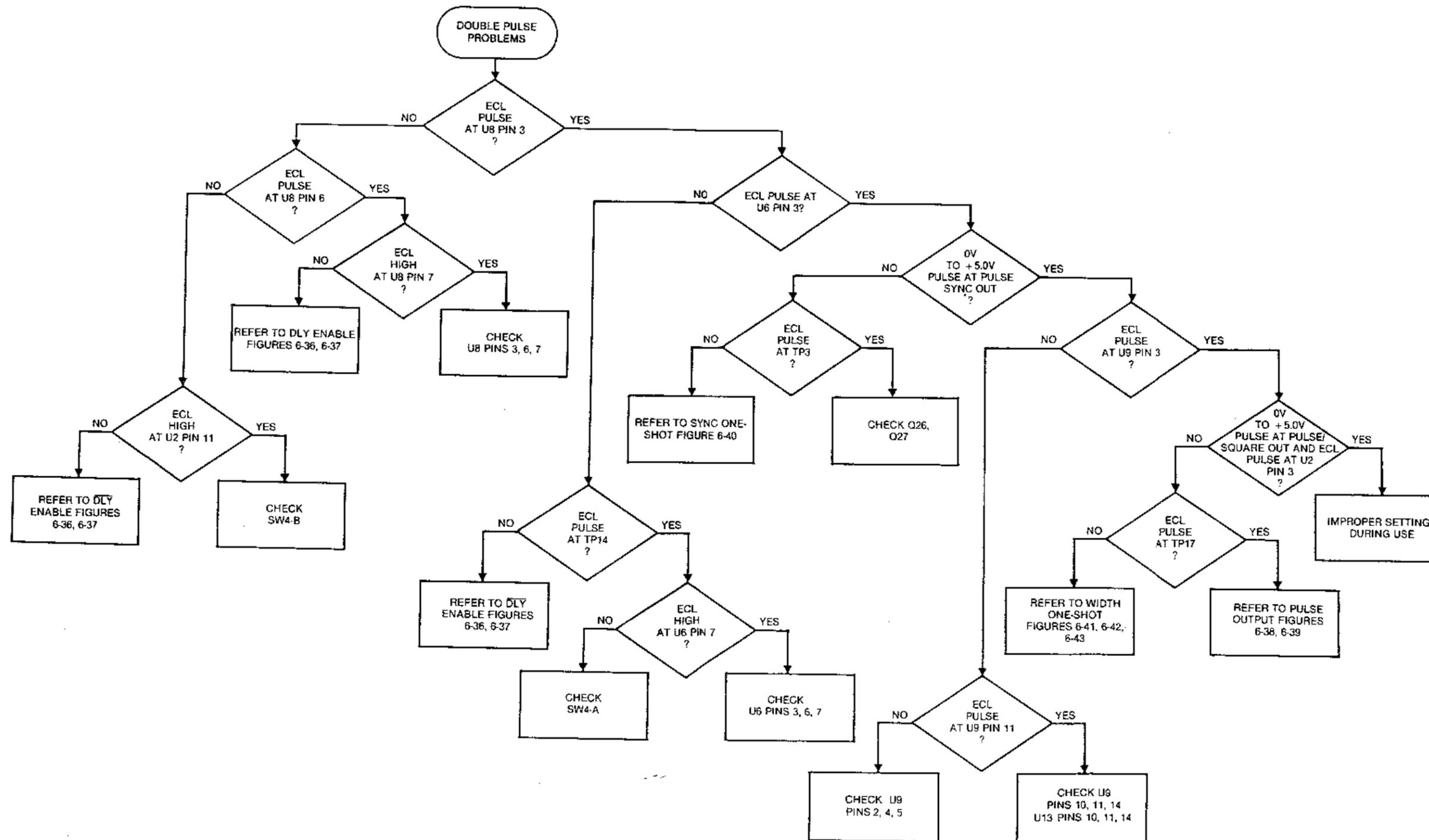


Figure 6-27. Dbl Pulse Troubleshooting

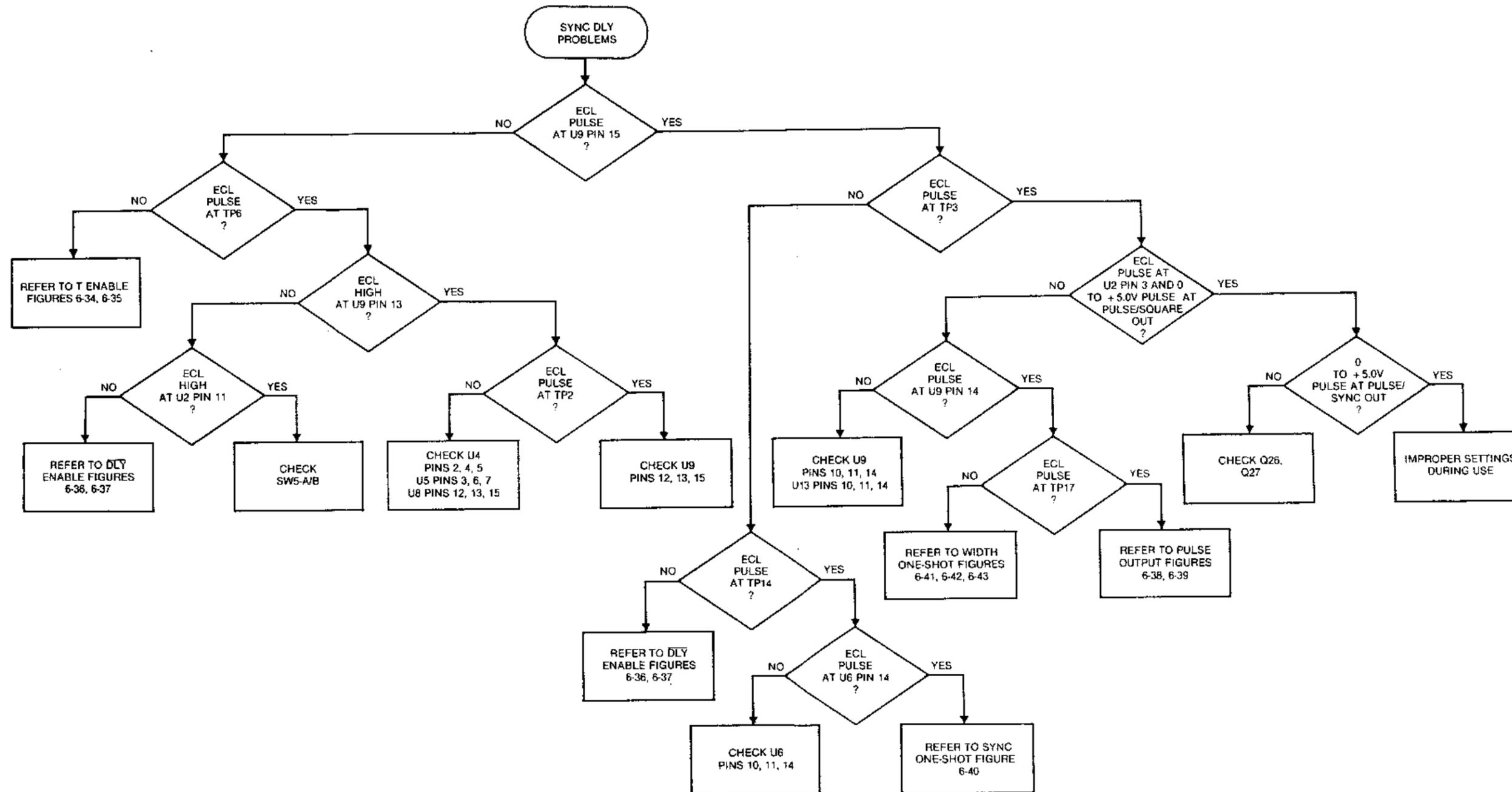


Figure 6-29. Sync Dly Troubleshooting

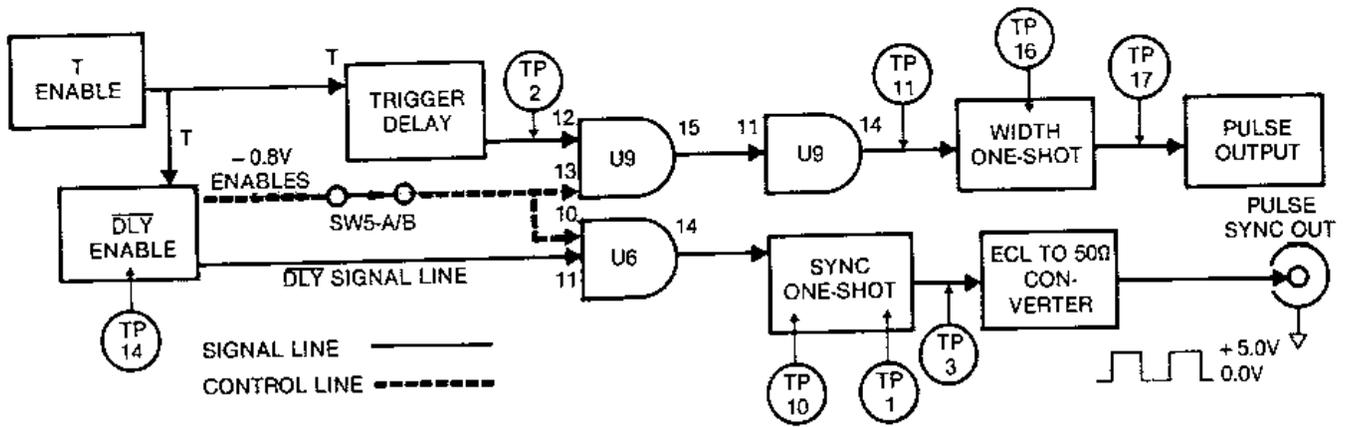


Figure 6-28. SYNC DLY Block and Timing Diagrams

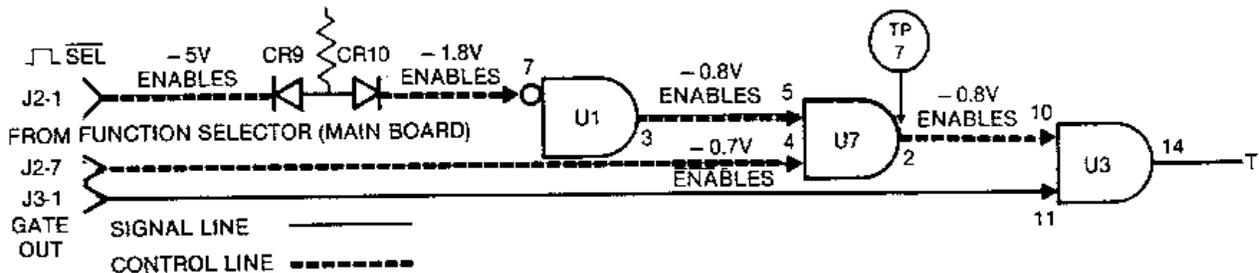


Figure 6-30. Trig (Func) Block Diagram

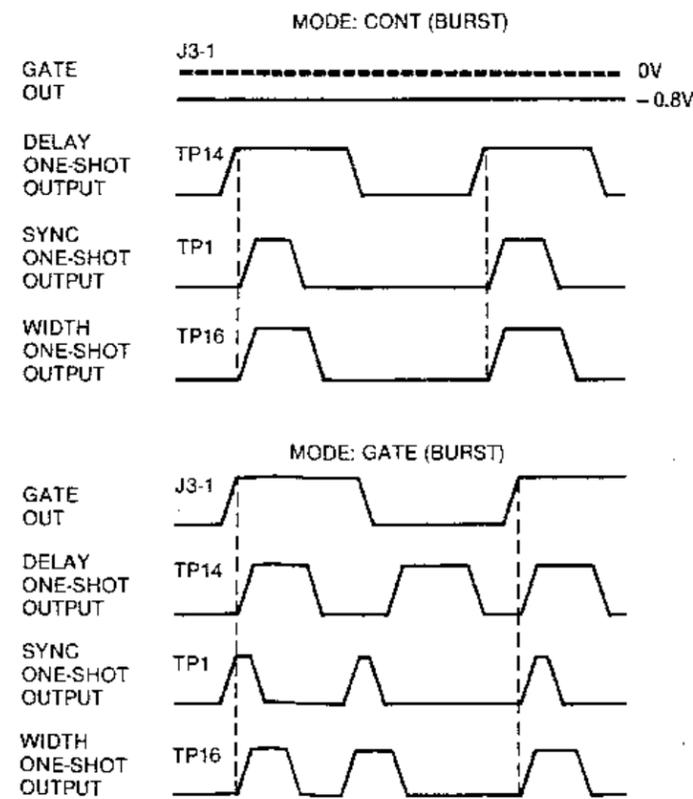
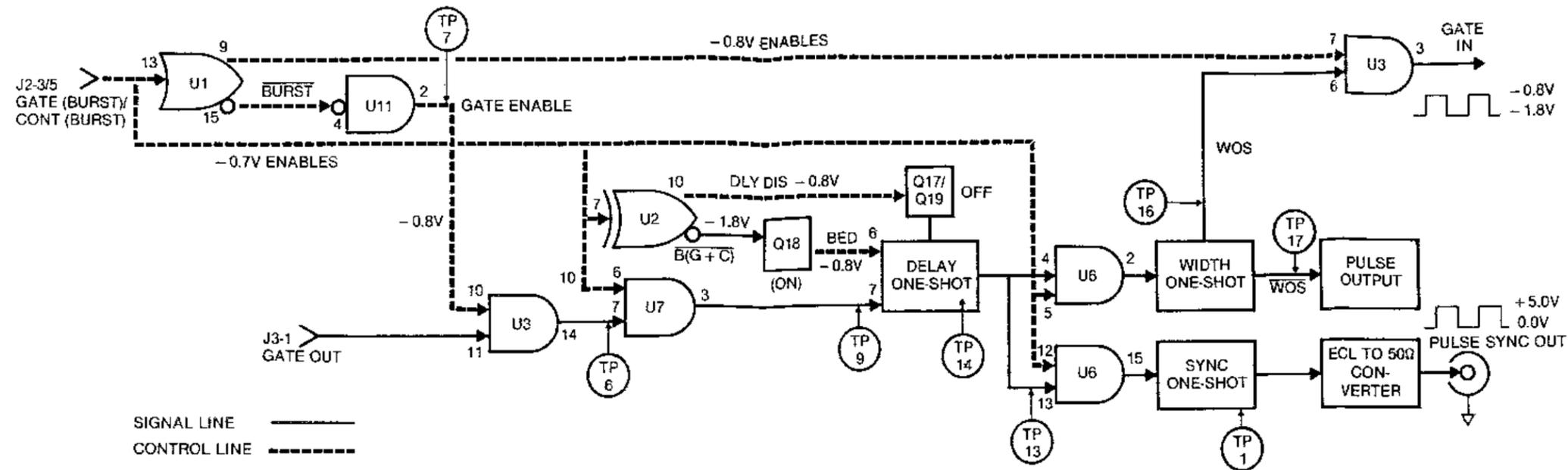
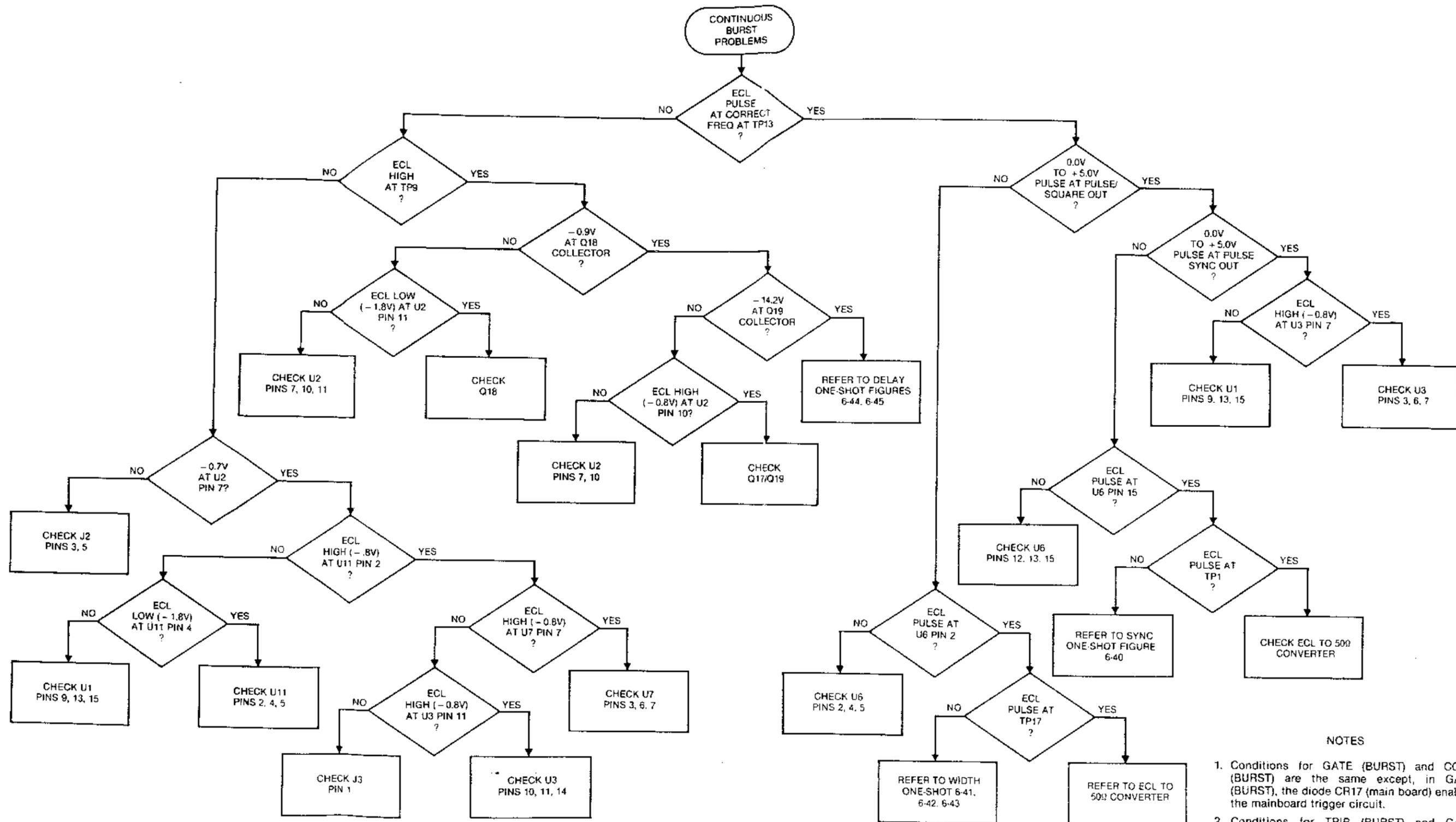


Figure 6-32. Cont (Burst)/Gate (Burst) Block and Timing Diagrams



- NOTES
1. Conditions for GATE (BURST) and CONT (BURST) are the same except, in GATE (BURST), the diode CR17 (main board) enables the mainboard trigger circuit.
 2. Conditions for TRIB (BURST) and GATE (BURST) are the same except, in TRIG (BURST), the GATE OUT is a 10 ns pulse.

Figure 6-33. Cont (Burst) Troubleshooting

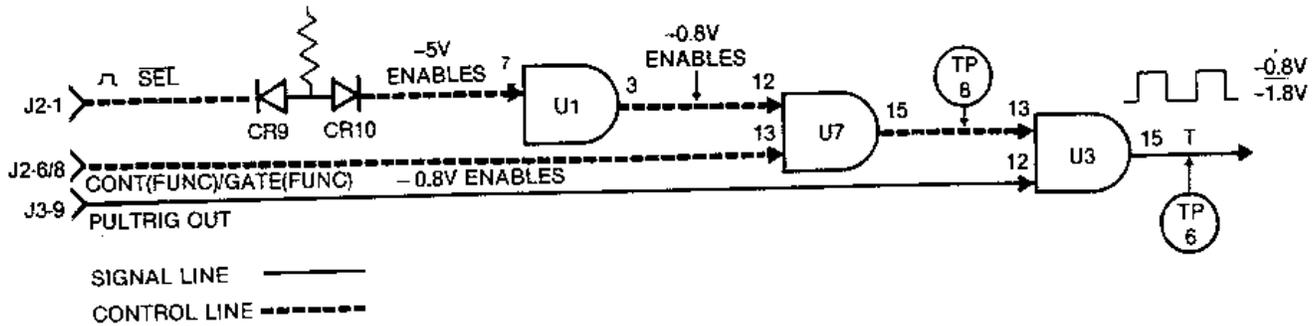


Figure 6-34. T Enable Block Diagram.

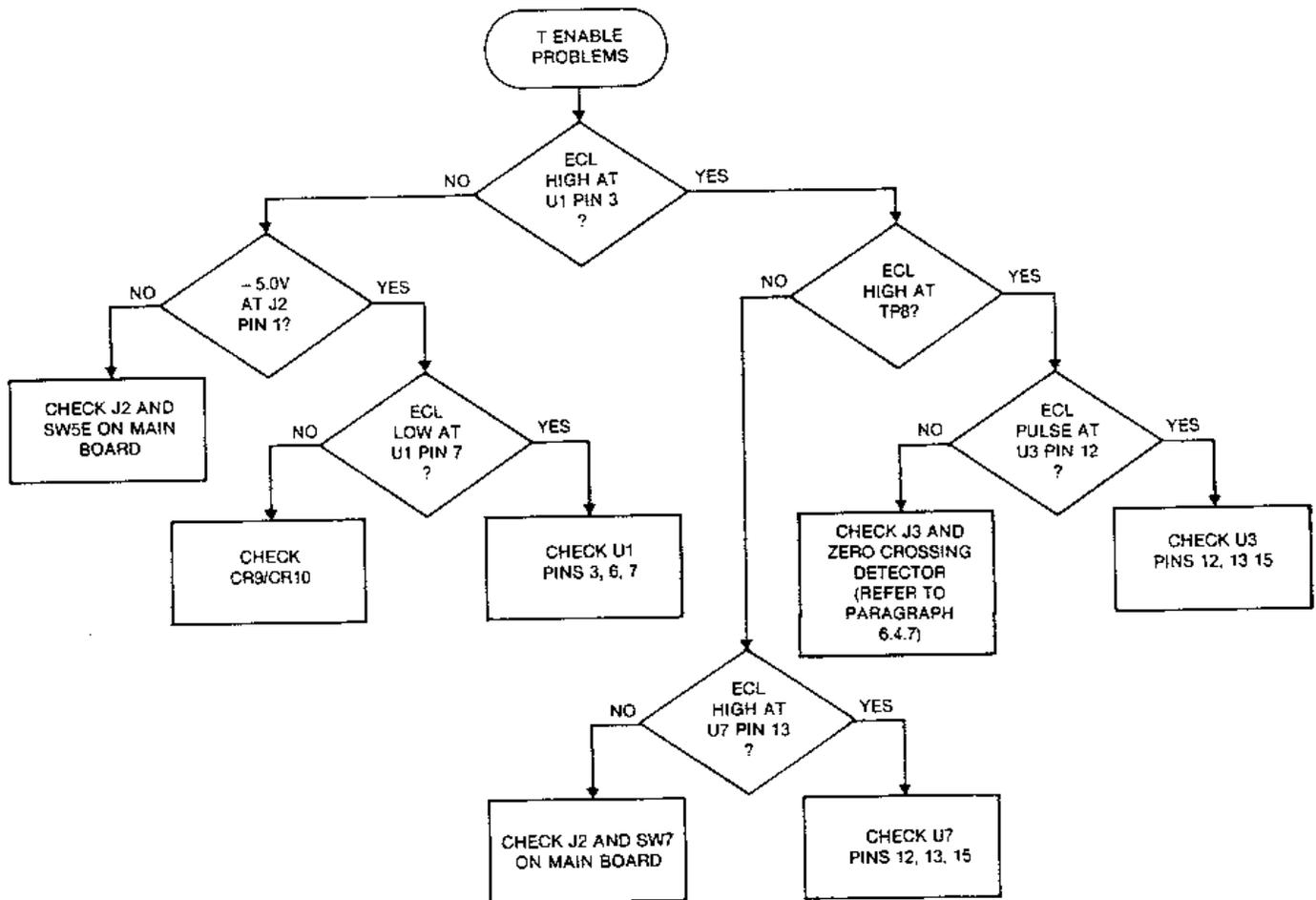


Figure 6-35. T Enable Troubleshooting

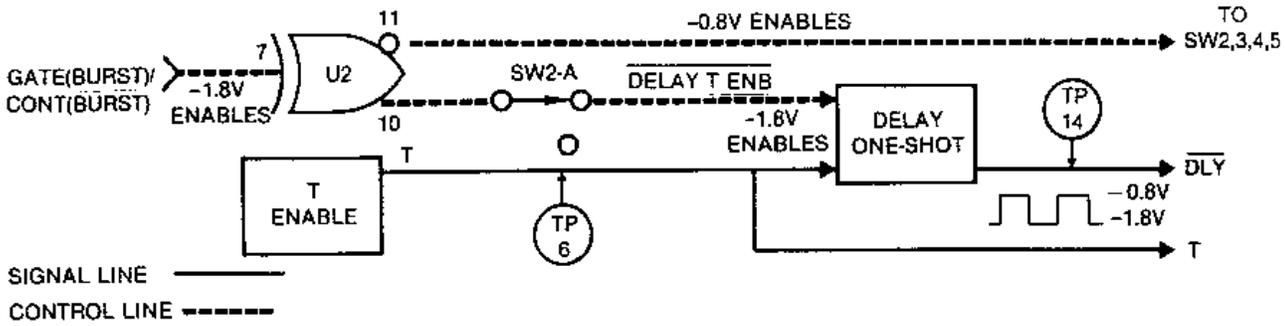


Figure 6-36. \overline{DLY} Enable Block Diagram.

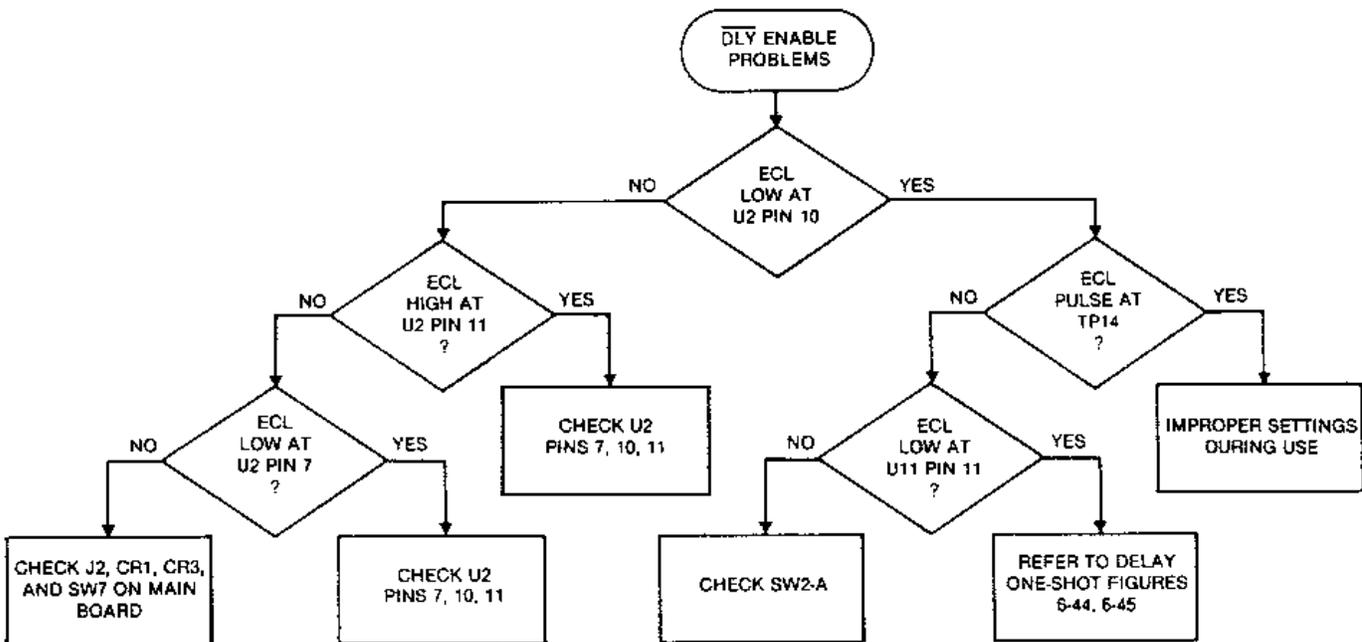


Figure 6-37. \overline{DLY} Enable Troubleshooting

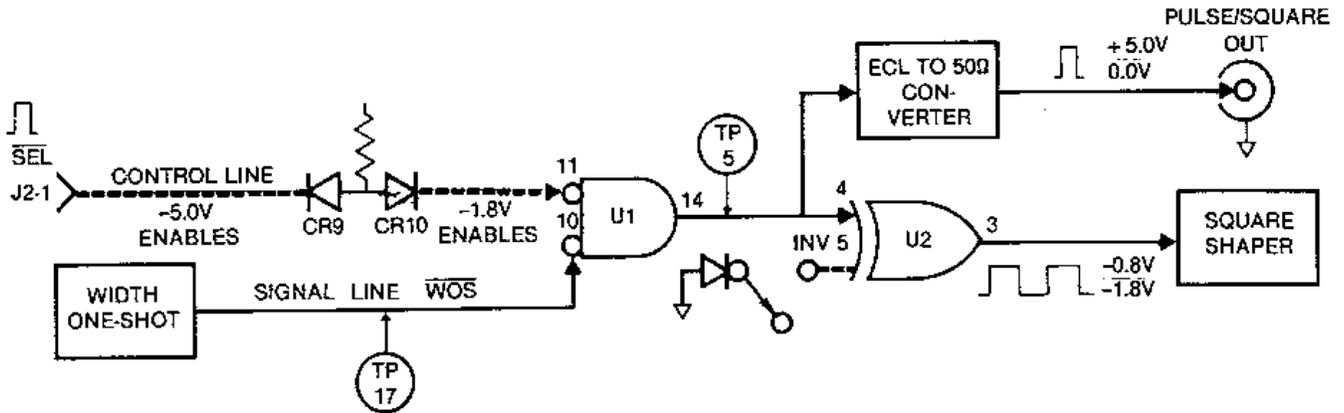


Figure 6-38. Pulse Output Block Diagram.

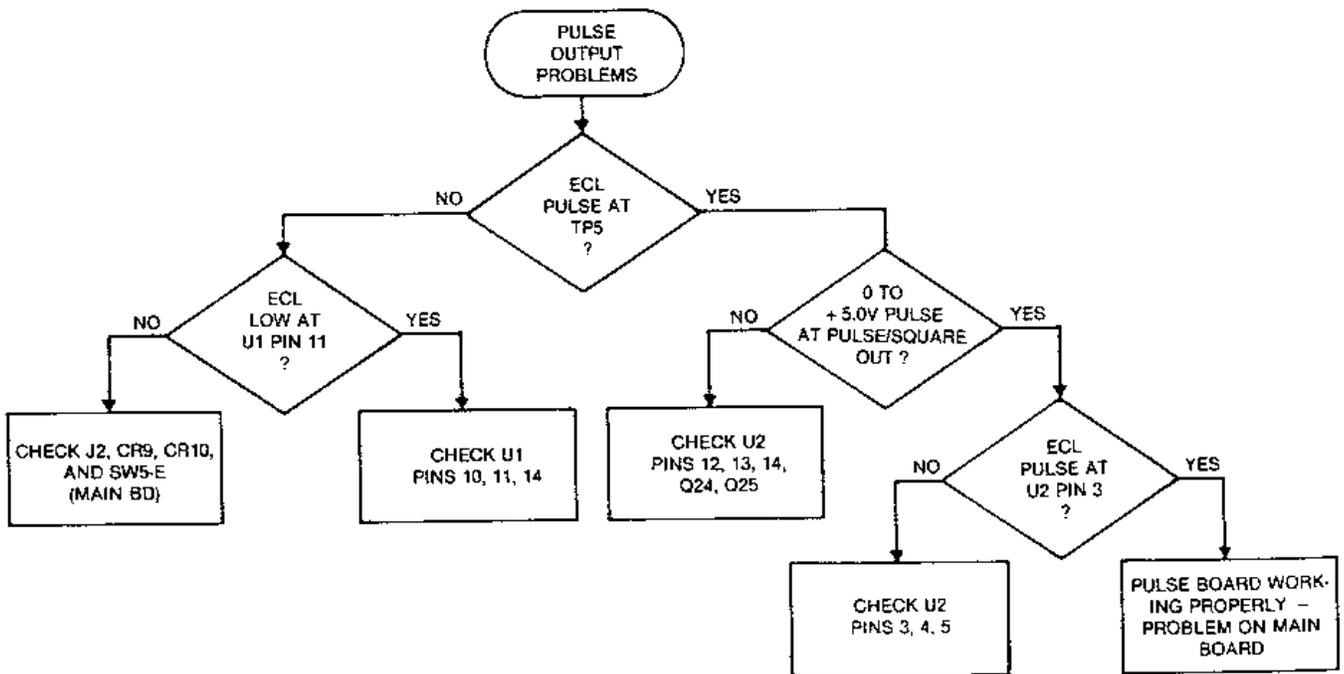


Figure 6-39. Pulse Output Troubleshooting

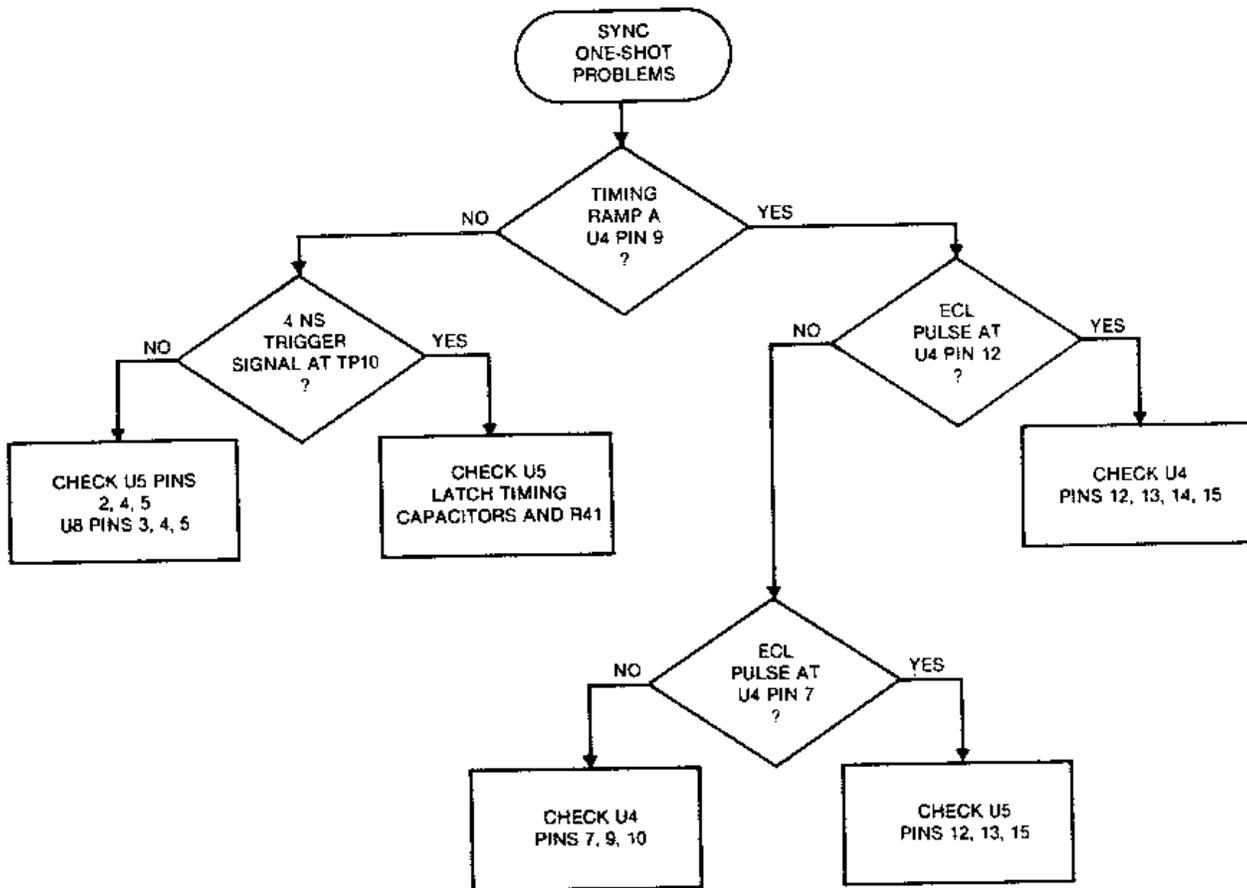


Figure 6-40. Sync One-shot Troubleshooting

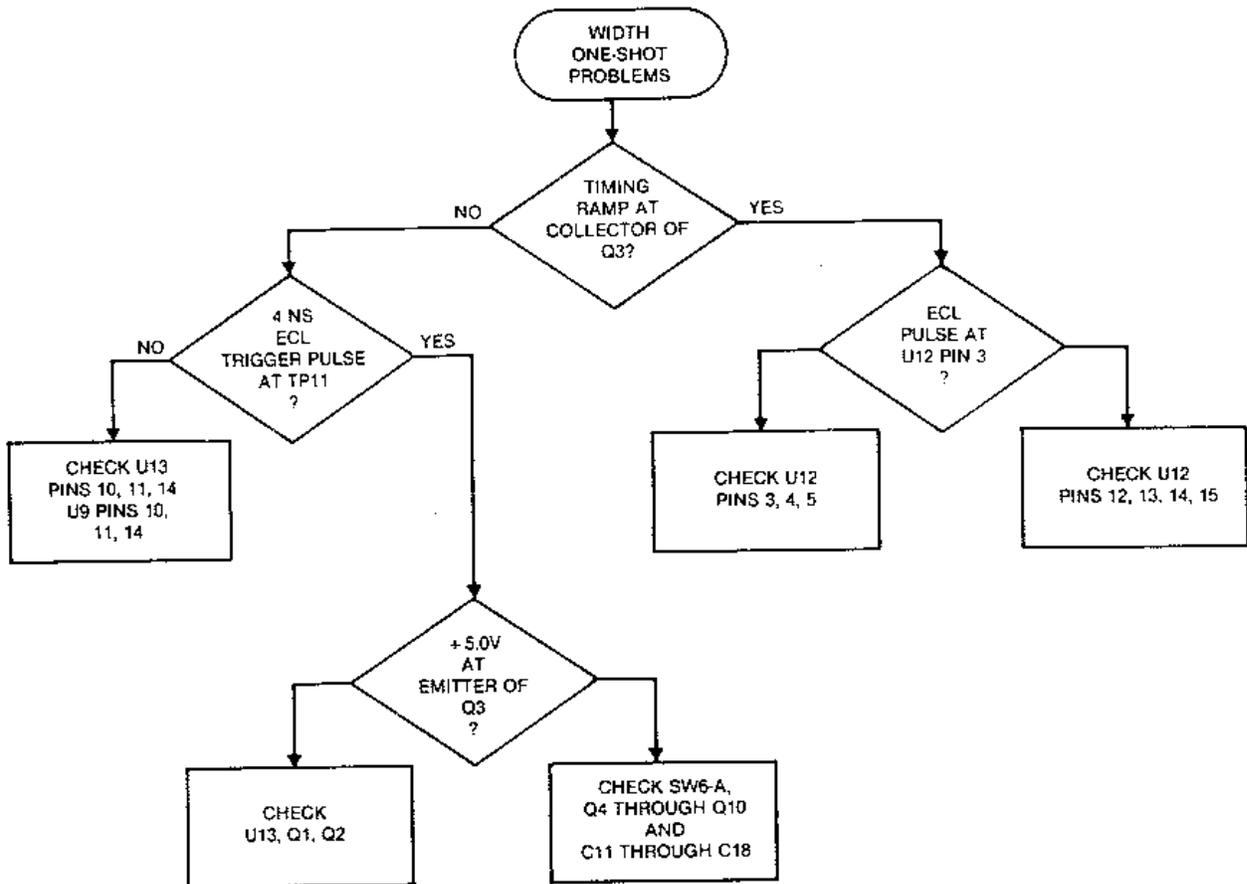


Figure 6-41. Width One-shot Troubleshooting

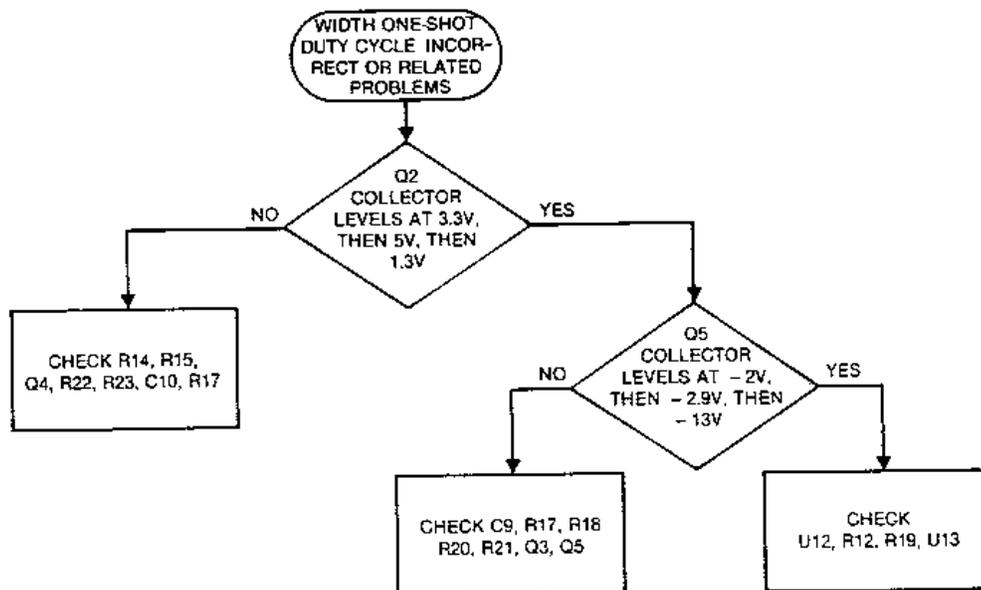


Figure 6-42. Width One-Shot Current Source Troubleshooting

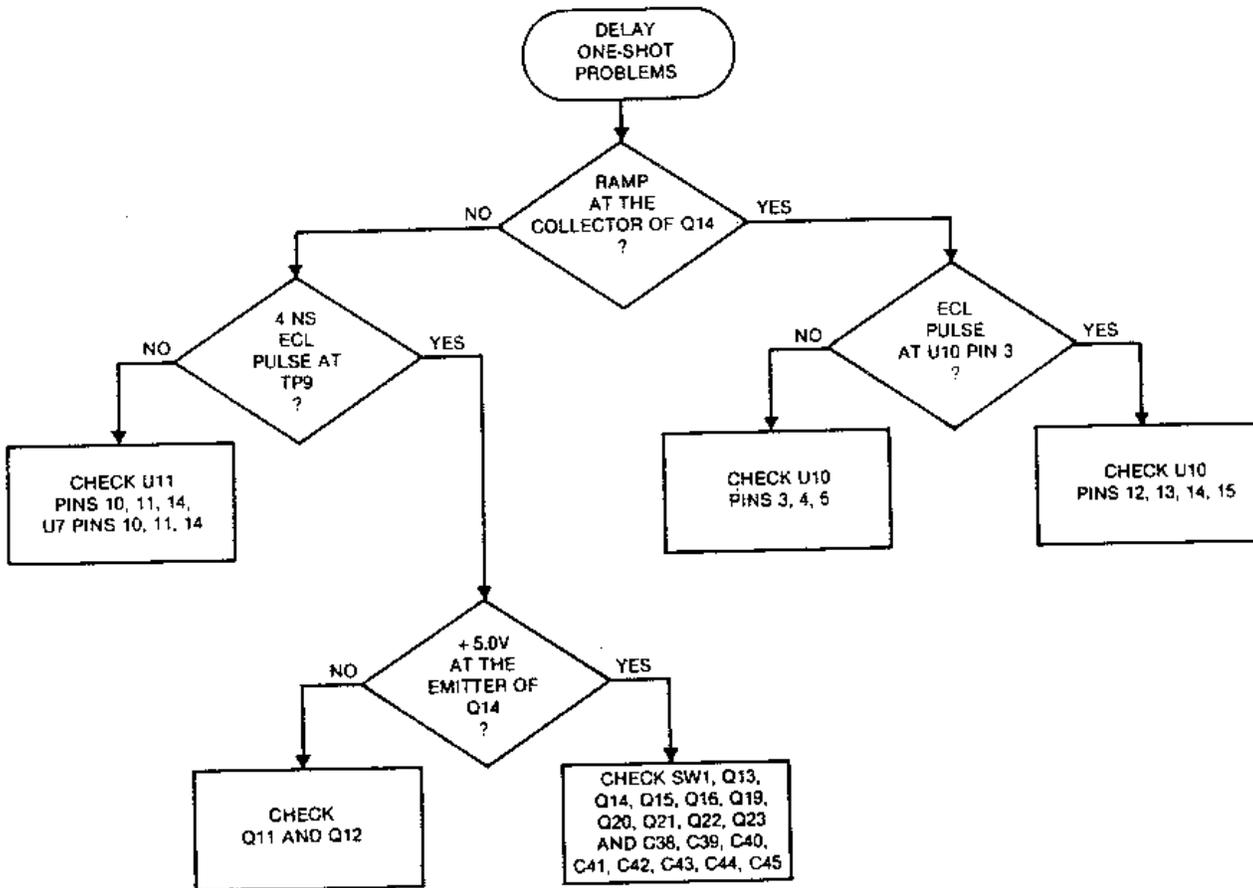


Figure 6-44. Delay One-shot Troubleshooting

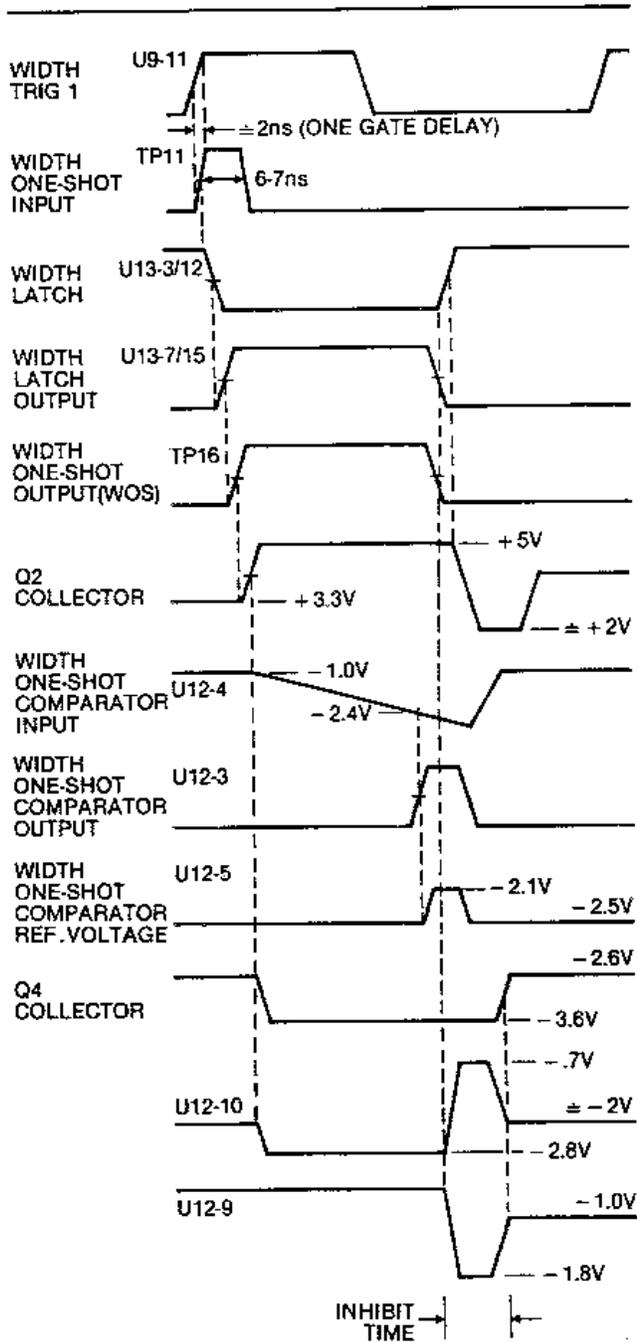


Figure 6-43. Width One-shot Timing Diagram.

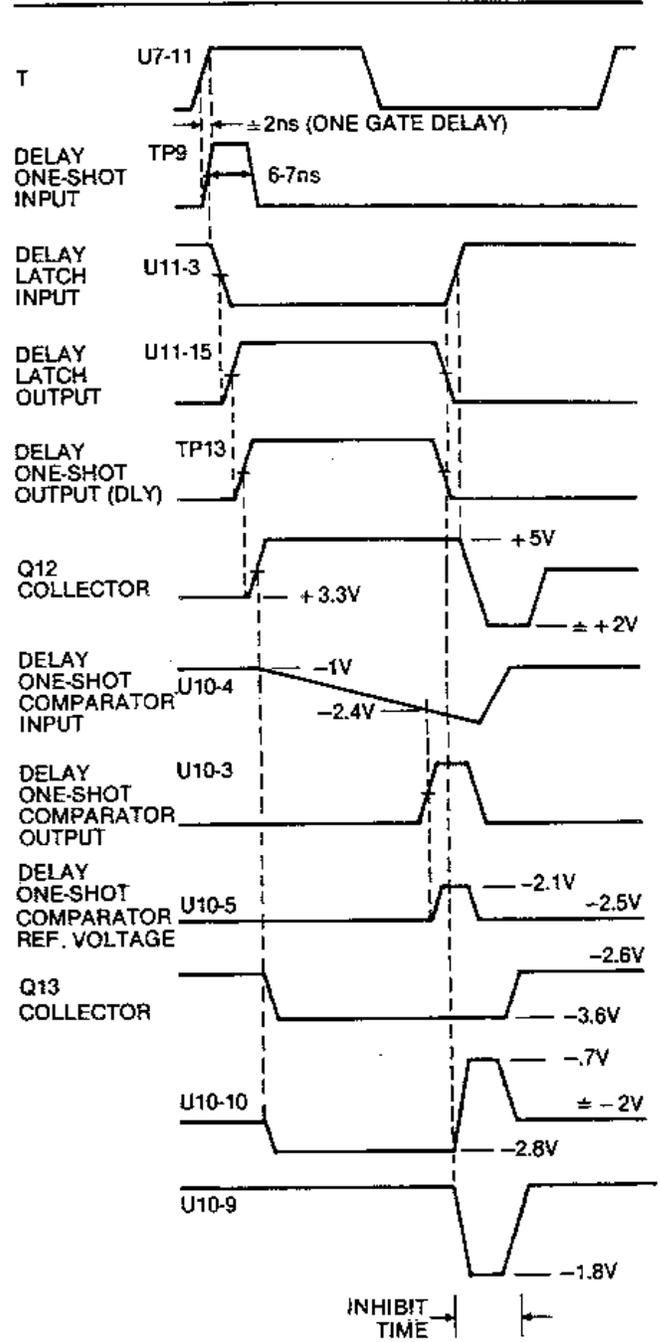


Figure 6-45. Delay One-shot Timing Diagram.

6.6 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.6.1 Transistor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.
2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.
3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage (or reversed bias), the transistor is defective.
4. A transistor is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).
5. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise, one of the transistors is defective.

6.6.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.6.3 Operational Amplifier

1. The "+" and "-" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "-" input (voltage follower connection), the

output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.

3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "-" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.6.4 FET Transistor

1. No gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective.
2. The gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485, and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.
3. If the device supplying gate voltage to an FET saturates, the FET has too large a V_{gs} (pinch off) for the circuit and should be replaced.

6.6.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

6.6.6 Digital ECL ICs

1. The device is operating correctly if the output high state is -0.81 to $-0.96V$ and low state is -1.65 to $-1.85V$.
2. The input must show the same two levels as in step 1.

SECTION 7

PARTS LIST AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, (with parts lists) and schematics are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, an errata is prepared to

summarize the changes made and is inserted in the shipping carton with this manual. If no errata exists, the manual is correct as printed.

7.2 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and the function performed.

NOTE

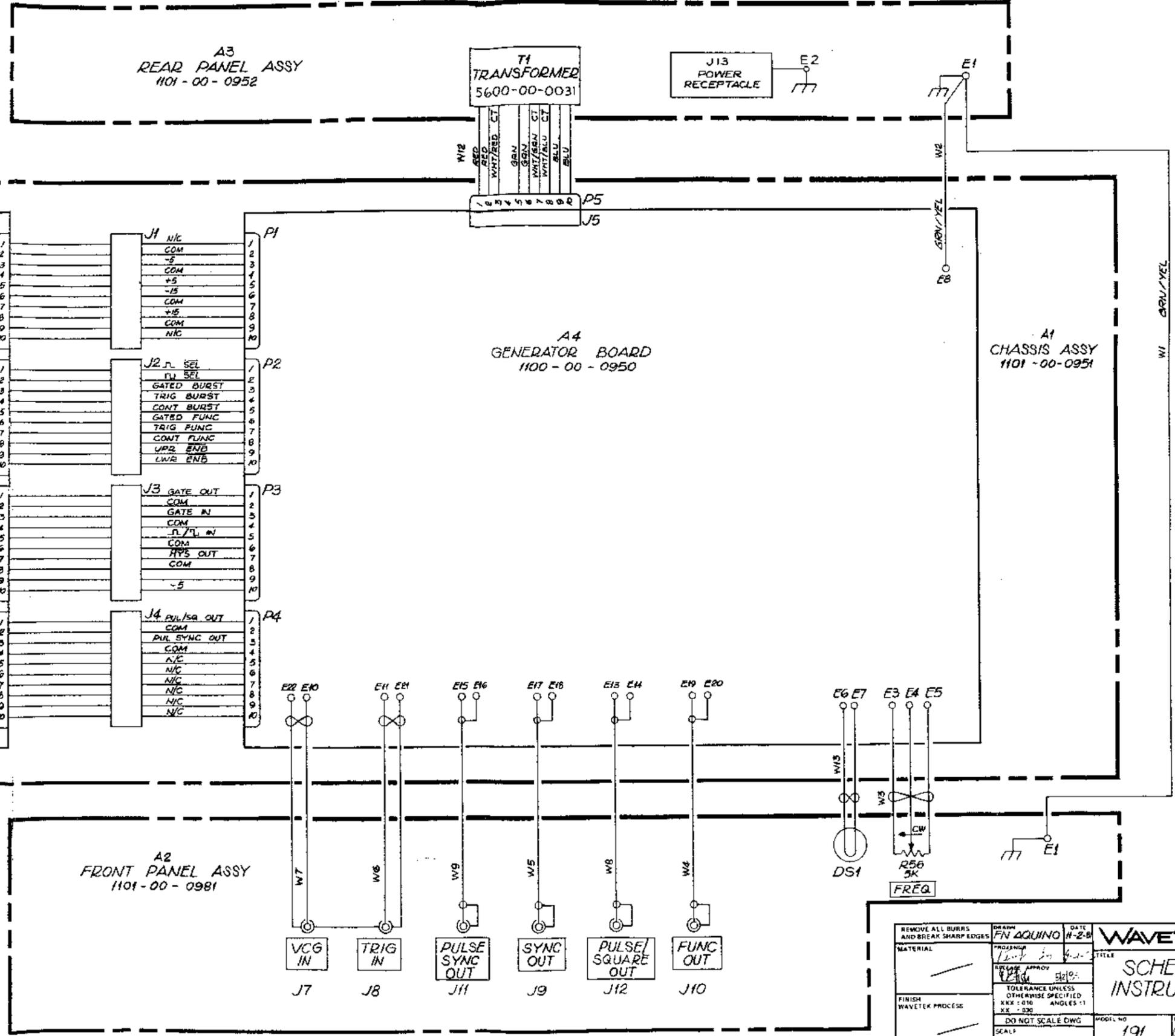
An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Instrument Schematic	0004-00-0181
Instrument Parts List	1000-00-0181
Chassis Assembly	0102-00-0951
Chassis Parts Lists	1101-00-0951
Generator Board Schematic	0103-00-2926
Generator Board Assembly	1100-00-2926
Generator Board Parts List	1100-00-2929
Generator Board Switch Assembly	0102-00-0953
Generator Board Switch Parts List	1202-00-0953
Pulse Board Schematic	0103-00-0946
Pulse Board Assembly	1100-00-0946
Pulse Board Parts List	1100-00-0946
Pulse Board Switch Assembly	0102-00-0966
Pulse Board Switch Parts List	1202-00-0966
Rear Panel Assembly	0102-00-0952
Rear Panel Parts List	1101-00-0952
Front Panel Assembly	0102-00-0981
Front Panel Parts List	1101-00-0981

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B
A

C
F
E
D
C
B
A



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FN AQUINO	DATE 11-2-66	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJENR 1207 in 4-2	TITLE SCHEMATIC INSTRUMENT	
FINISH WAVETEK PROCESS	DESIGN APPROV [Signature]	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 016 ANGLES 1:1 XX - 030	MODEL NO 191
	DO NOT SCALE DWG	SCALE	DWG NO 0004-00-0181
			REV A
			CODING 23338
			SHEET / OF /

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REV	EDN	BY	DATE	APP
-----	-----	----	------	-----

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO	QTY/PT
NONE	SCHEMATIC INSTRUMENT	0004-00-0181	WVTK	0004-00-0181	1
NONE	FINAL CAL PROCEDURE	0006-00-0181	WVTK	0006-00-0181	1
NONE	QA ACCEPTANCE	0007-00-0181	WVTK	0007-00-0181	1
NONE	PCA PULSE	191-0946	WVTK	1100-00-0946	1
NONE	ASSY. PCA GENERATOR BD 191-0950	1100-00-2929	WVTK	1100-00-2929	1
NONE	ASSY. CHASSIS	191-0951	WVTK	1101-00-0951	1
NONE	ASSY. REAR PANEL	191-0952	WVTK	1101-00-0952	1
NONE	ASSY. FRONT PANEL	190-0981	WVTK	1101-00-0981	1
NONE	INSTRUCTION MANUAL	MANUAL-191	WVTK	1300-00-0181	1
NONE	INSERT	101-7	WVTK	3300-00-0003	1
NONE	CARTON	101-7A	WVTK	3300-01-0003	1
NONE	PWR CORD	6001-80-0005	WVTK	6001-80-0005	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 191 20MHZ PULSE/FUNCTION GENERATOR	1000-00-0181	F
	PAGE 1		

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROF/ENGR		
FINISH WAVETEK PROCESS	RELEASE APPROV		TITLE PARTS LIST INSTRUMENT
	TOLERANCE UNLESS OTHERWISE SPECIFIED		
	X.XX : 010 ANGLES : 1 X.X : 030		
DO NOT SCALE DWG	MODEL NO	DWG NO	REV
SCALE	191	1000-00-0181	F
	CORE DIN 1	23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

DATE	
REV	
BY	
CHKD	

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GENERATOR BD(A4)
(REF: P/N 1100-00-0950)
ATTACH TO SHIELD PLATE
AND FRONT PANEL ASSEMBLIES
USING NO. 4-40 x 1/4" SELF LOCKING
SCREWS (10 REQ'D)

FRONT PANEL(A2)
(REF: P/N 1101-00-0981)

NO. 8-32 x 2" PAN HEAD
SCREW (4 PLCS.)

REAR PANEL(A3)
(REF: P/N 1101-00-0952)

NO. 4-40 x 3/8" PAN HEAD SELF LOCKING
SCREW WITH FLAT
WASHER (4 PLCS.)

APPLY THERMAL CONDUCTIVE
TO SURFACE OF BOARD MTC ANGLE
WHICH CONTACTS REAR PANEL
(TYP 2 PLCS)

SEE DETAIL "A"

9 (2) SEE DETAIL "A"

PULSE BOARD(A5)
(REF: P/N 1100-00-0946)
ATTACH TO SHIELD PLATE
ASSY USING NO. 4-40 x 1/4"
SELF LOCKING SCREWS
(6 REQ'D)

ADHESIVE BOND ITEM
NO. 5 TO ITEM NO. 3

DETAIL "A"
CONNECTOR/GUIDE PIN INSTALLATION

NO. 4-40 x 1/4" SELF
LOCKING SCREW
(2 REQ'D)

GEN. BD.
(COMPONENT
SIDE)

PULSE BD.
(SOLDER
SIDE)

NOTE OR!

1. AFTER INSTALLATION OF FRONT PANEL PLEASE APPLY
1" CHORD OF LOCATOR A14 (OR EQUIV) TO FULLY ENGAGE
(6) ALL 1/4" HR PIN TO DOW (FEET 118).

2. THIS SHEET IS INTENDED TO SHOW MECHANICAL
ASSEMBLY ONLY, REFERENCE SHEET 2 FOR WIRING.

1. SEE PARTS LIST NO: 1101-00-0951.

NOTE: UNLESS OTHERWISE SPECIFIED

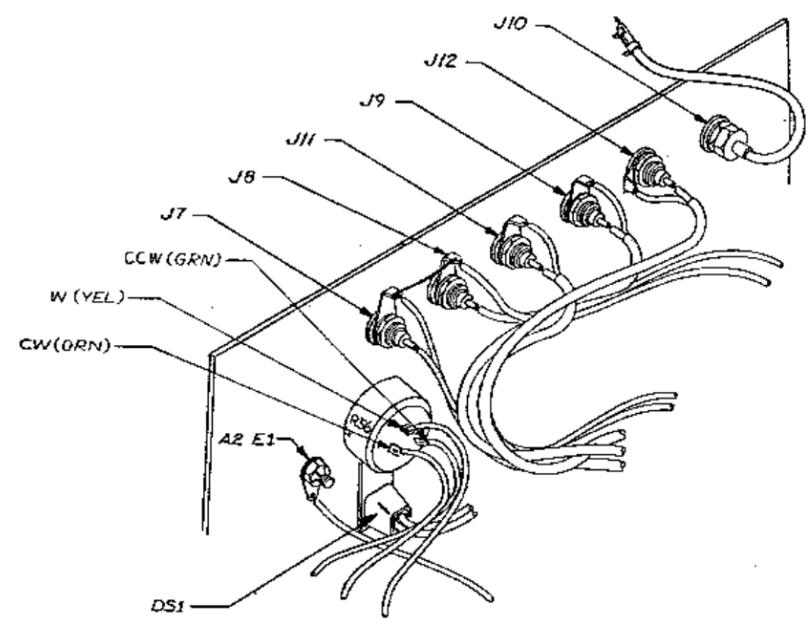
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN DCC	DATE 09-80	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	PROJ. NO.		TITLE ASSEMBLY, CHASSIS (A1)	
FINISH WAVETEK PROCESS	RELEASE APPROV.		MODEL NO. 191	REV C
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: 010 ANGLES: 1: XX: 030		OWG NO. 0102-00-0951	
	DO NOT SCALE DWG		SCALE	
			EDD 23338	SHEET 1 OF 2

7 6 5 4 3 2 1

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REV	ECN	BY	DATE	APP

CHASSIS ASSEMBLY WIRE & CABLE HOOK-UP			
REF DES	FROM	TO	COLOR
W1	REAR PANEL - A3 E1	FRONT PANEL - A2 E1	GRN/YEL
W2	REAR PANEL - A3 E1	GEN BD - A4 E8	GRN/YEL
W3	GEN BD - E3	FRONT PANEL - R56-CW	ORN
	GEN BD - E4	FRONT PANEL - R56-W	YEL
	GEN BD - E5	FRONT PANEL - R56-CCW	GRN
W4	GEN BD - E19	FRONT PANEL - J10	BLK
	GEN BD - E20	FRONT PANEL - J10	BLK
W5	GEN BD - E17	FRONT PANEL - J9	BLK
	GEN BD - E18	FRONT PANEL - J9	BLK
W6	GEN BD - E11	FRONT PANEL - J8	WHT/BRN
	GEN BD - E21	FRONT PANEL - J8	BLK
W7	GEN BD - E10	FRONT PANEL - J7	WHT/BLK
	GEN BD - E22	FRONT PANEL - J7	BLK
W8	GEN BD - E13	FRONT PANEL - J12	BLK
	GEN BD - E14	FRONT PANEL - J12	BLK
W9	GEN BD - E15	FRONT PANEL - J11	BLK
	GEN BD - E16	FRONT PANEL - J11	BLK
W12	REAR PANEL - A3	GEN BD - J5	N/A
W13	GEN BD - A4 E6	FRONT PANEL - DS1	N/A
	GEN BD - A4 E7	FRONT PANEL - DS1	N/A



FRONT PANEL WIRING AND ROUTING (SEE WIRE LIST)

1. THIS SHEET IS INTENDED TO LIST WIRING HOOK UP. SEE SHEET 1 FOR MECHANICAL ASSEMBLY.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: CHERMACK	DATE: 2-2-82	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	PROJ: 191	DATE: 2/2/82	TITLE: ASSEMBLY, CHASSIS (A1)	
FINISH WAVETEK PROCESS	WAVE APPROV: [Signature]	DATE: 2/2/82	TOLERANCE UNLESS OTHERWISE SPECIFIED: XX.X .010 ANGLES 1:1	
SCALE	DO NOT SCALE DWG	MODEL NO: 191	DWG NO: 0102-00-0951	REV: C
	CODE IDENT: 23338	SHEET 2 OF 2		

0102-00-0951 C

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-PFOR-PART-NO	PFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. CHASSIS	0102-00-0951	WVTK	0102-00-0951	1
1	ASSY. SHIELD PLATE	191-0955	WVTK	1206-00-0955	1
2	SPK ASSY. POWER ROD	190-0956	WVTK	1206-00-0956	1
NONE	CHASSIS CABLE KIT	191-0954	WVTK	1207-00-0954	1
NONE	PLATE, NAME	139-303	WVTK	1400-00-2180	1
NONE	COVER, TOP	180-300-1	WVTK	1400-00-5000	1
5	EXPANDER	180-301	WVTK	1400-00-5010	2
NONE	COVER, BOTTOM	180-300-2	WVTK	1400-00-5030	1
9	GUIDE PIN	191-4882	WVTK	1400-01-4882	2
7	COAX KNOB SET	RB-67-1-SB+0-W-9	ROGAN	2400-01-0009	5
8	KNOB, SMALL	0-W-9	ROGAN	2400-01-0010	1
10	STANDOFF, MALE/FEMALE 1.750 H., 250 HEX8-32	1475-M03-F05-832	UNICP	2800-02-0010	4
NONE	BAIL ASSY W/FT	180-500	WVTK	2800-06-0010	1
NONE	SPEEDNUT, SELF RETAIN	C7494-632-4	TENN	2800-09-0003	6

WAVETEK PARTS LIST	TITLE ASSY. CHASSIS	ASSEMBLY NO 1101-00-0951	REV A
	PAGE 1		

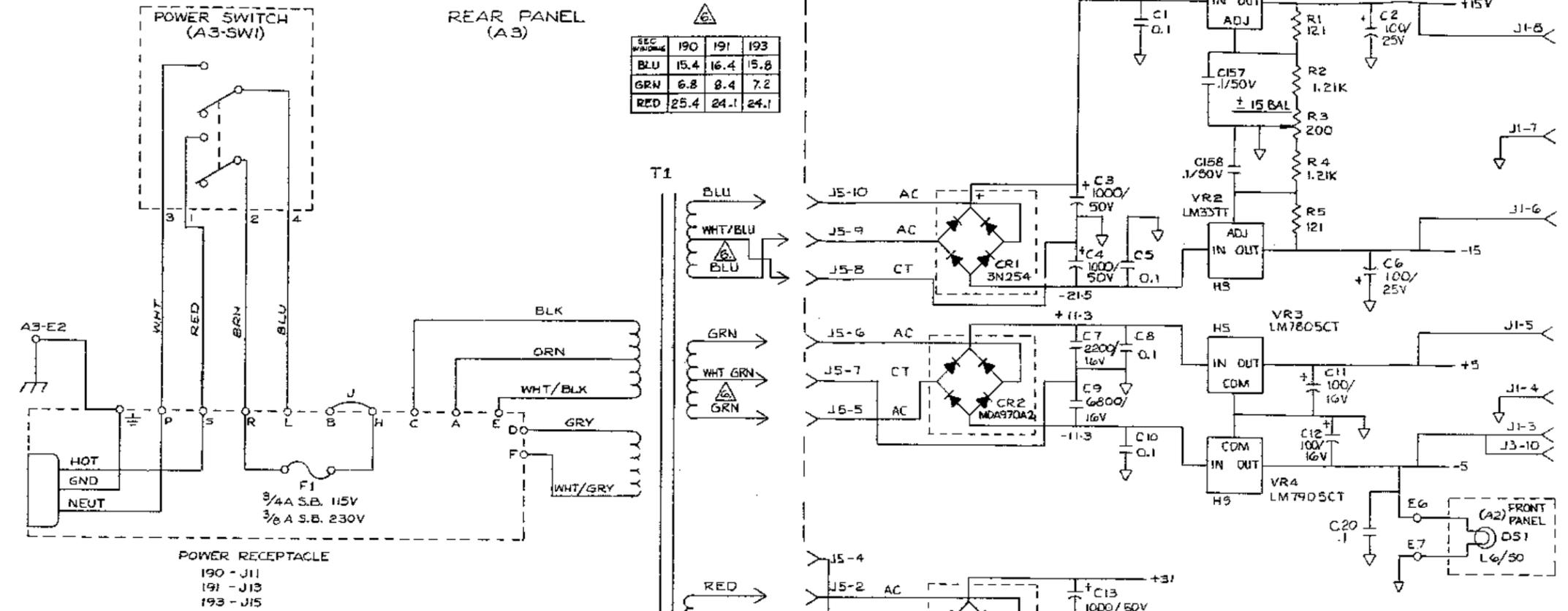
REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	PROV ENGR	TITLE PARTS LIST ASSY. CHASSIS	
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : DIM ANGLES : 1 XX : .030	
	DO NOT SCALE DWG	MODEL NO 191	DWG NO 1101-00-0951
SCALE		CODE 2333B	REV A
		SHEET 1 OF 1	

NOTE: UNLESS OTHERWISE SPECIFIED

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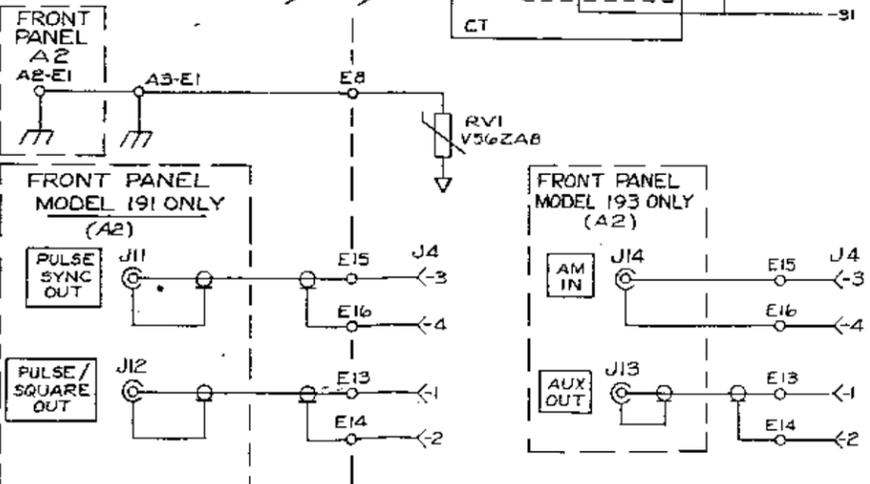
REV	ECN	BY	DATE	APP
A	ECN # 4633	JT	7/1/87	LET
B	#81-474	EG	10/29/89	KA
C	ECN # 174	WA	8/1/91	

POWER SUPPLY



SEC WINDING	190	191	193
BLU	15.4	16.4	15.8
GRN	6.8	8.4	7.2
RED	25.4	24.1	24.1

POWER RECEPTACLE
190 - J11
191 - J13
193 - J15



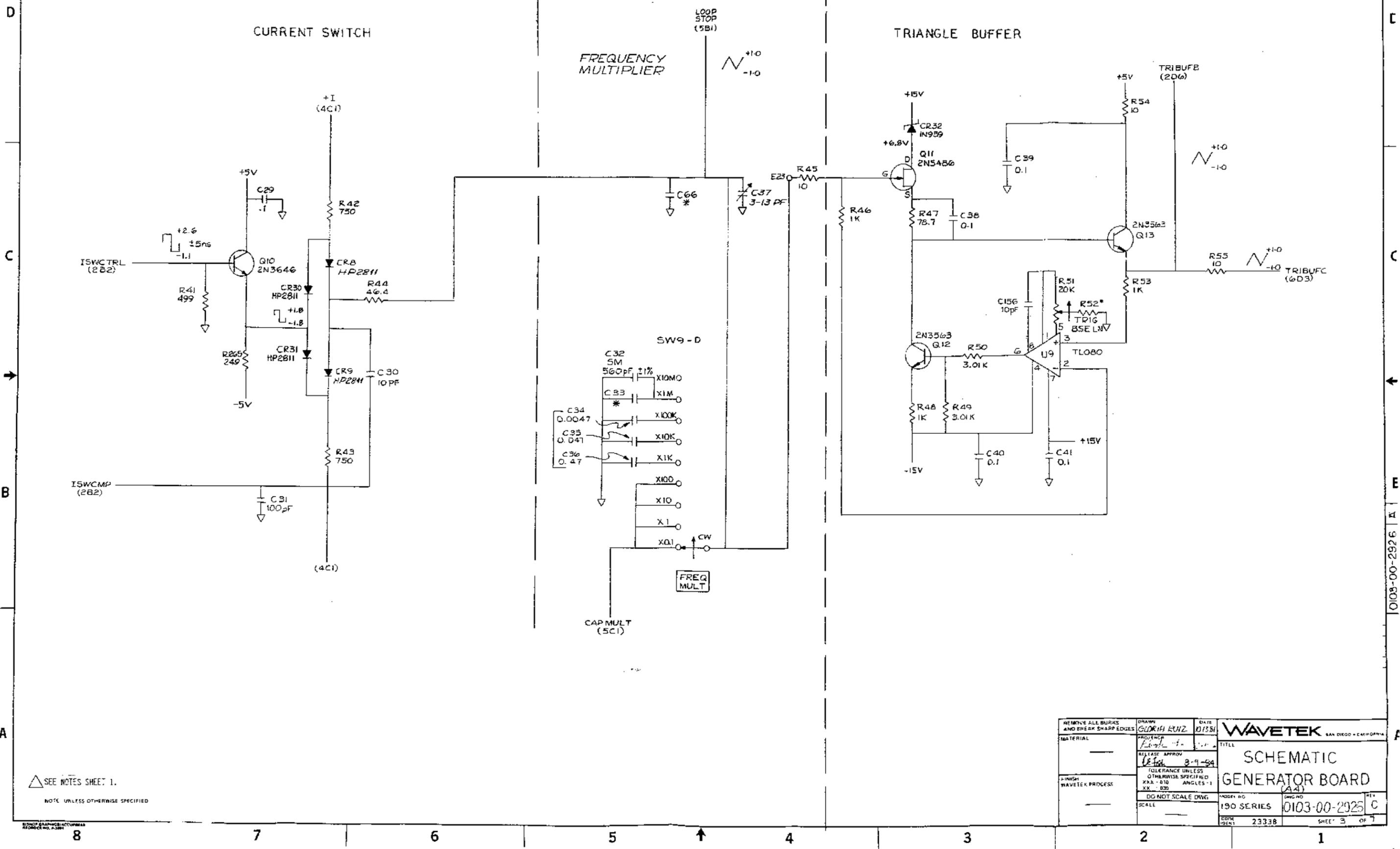
- 17. *NOMINAL VALUE-CALLED OUT ON PARTS LIST.
- 16. VOLTAGES VALID THRU X 100K ONLY (2 PLCS).
- 14. USED ON 192 ONLY.
- 13. NOT USED ON 193
- 12. NOT USED ON 191
- 11. NOT USED ON MODEL 192 (3 PLCS).
- 10. MODEL 193 ONLY (5 PLCS)
- 9. MODEL 191 ONLY (10 PLCS)
- 8. SELECTED 2N3866 FOR $V_{CE0} = 40V$ (3 PLCS)
- 7. P/N 4807-02-0777 (MATCHED PAIR FD777)
- 6. VOLTS AC WITH: $V_{LINE RMS} = 115$, CORCOM TAB = 120
- 5. SIP'S ARE: R12 = 470, R24 = 680, R124 = 680.
- 4. ALL DIODES ARE FD666
- 3. ALL CAPACITORS ARE IN MICROFARADS.
- 2. ALL RESISTORS ARE 1/8W AND ARE IN OHMS.
- 1. PARTIAL REFERENCE DESIGNATORS SHOWN, USE ASSEMBLY REF. DES. PREFIX A4 (EXAMPLE A4R1)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: GIORIA RUIZ	DATE: 10-13-81	
MATERIAL	PROJ. ENGR: Keith A. Korte	TITLE: SCHEMATIC GENERATOR BOARD (A4)	
FINISH WAVETEK PROCESS	APPROVE: [Signature]	DATE: 9-1-84	TOLERANCE UNLESS OTHERWISE SPECIFIED: .XXX - .010 ANGLES - 1° .XX - .030
DO NOT SCALE DWG	SCALE	MODEL NO: 190 SERIES	DWG NO: 0103-00-2926, C
		CODE: 23338	SHEET 1 OF 7

0103-00-2926

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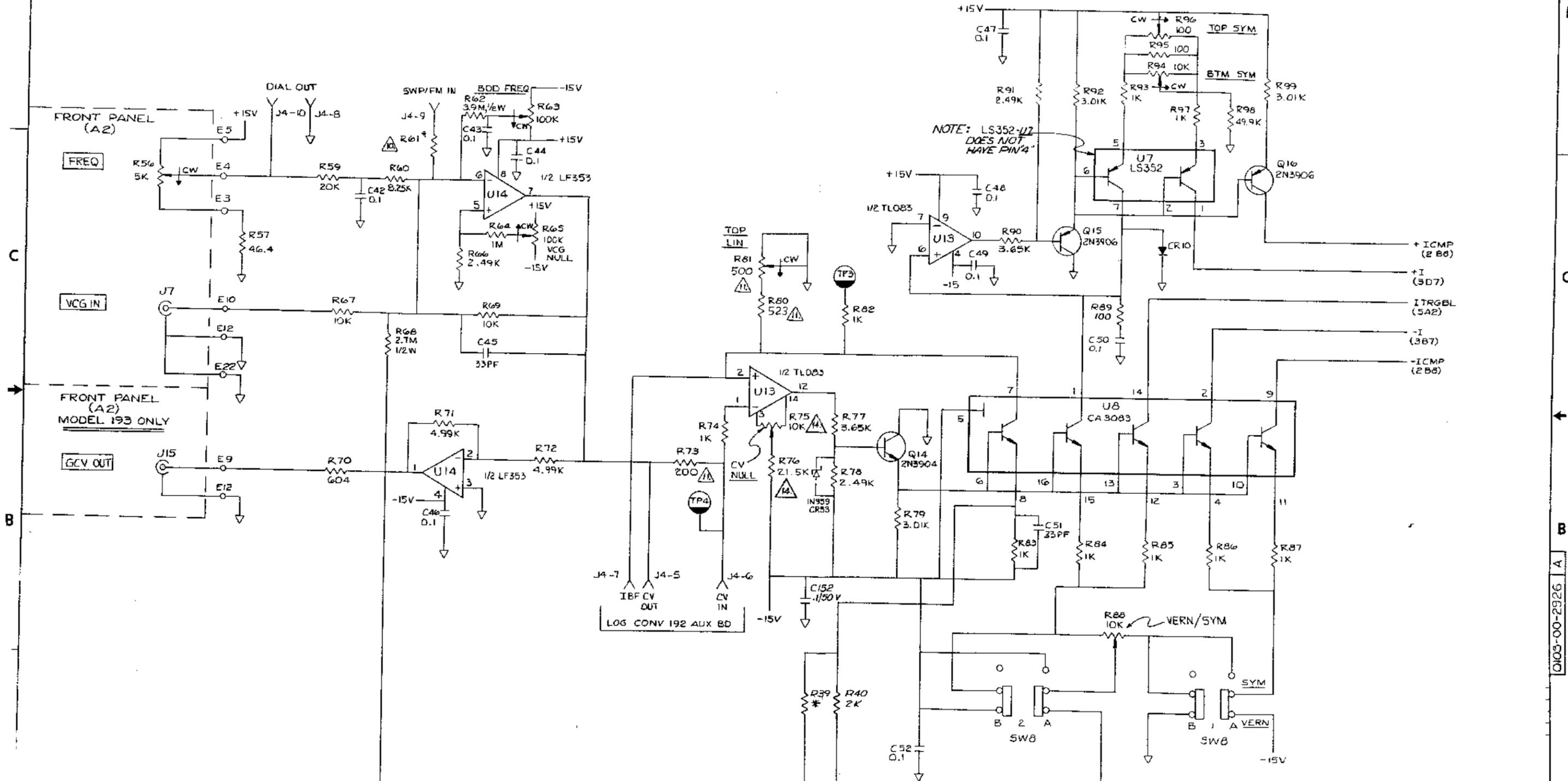
SEE NOTES SHEET 1.
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: GLORIA RUIZ	DATE: 10/15/81	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJECT: <i>Gen 1</i>	TITLE: SCHEMATIC GENERATOR BOARD	
FINISH: WAVETEK PROCESS	RELEASE APPROV: <i>[Signature]</i>	DATE: 3-9-84	REV: (24)
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 010 ANGLES - 1 XX - 030		MODEL NO: 190 SERIES
	DO NOT SCALE DWG		DWG NO: 0103-00-2925
	SCALE		REV: C
			CON: 23338
			SHEET 3 OF 7

0103-00-2926

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CURRENT SOURCES



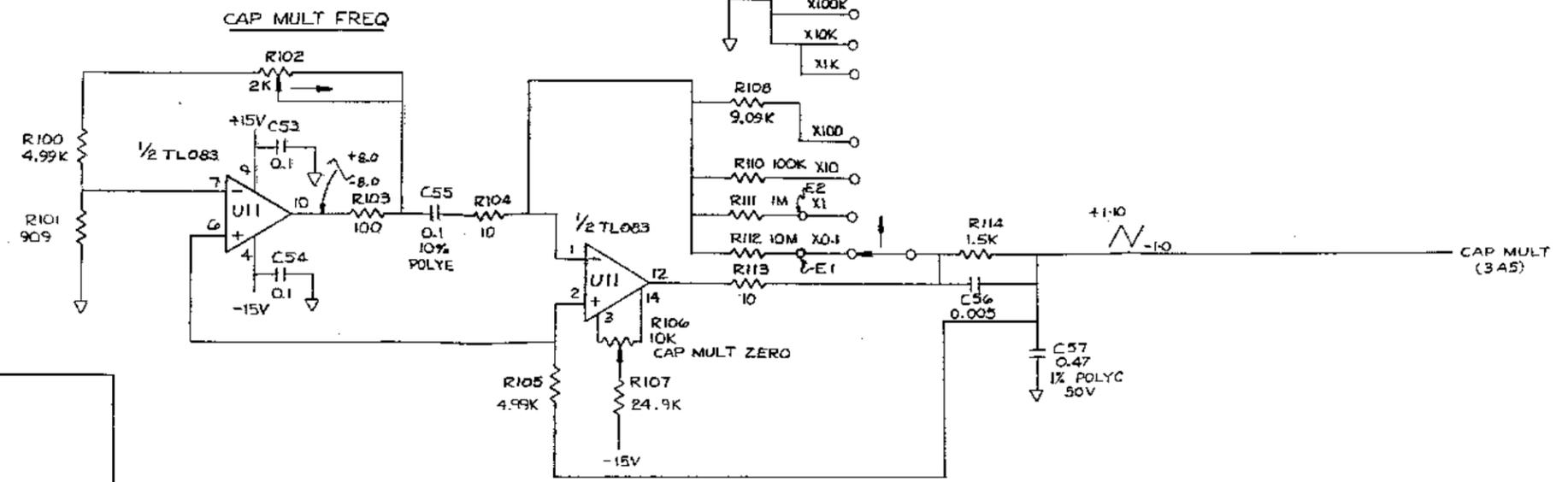
△ SEE NOTES SHEET 1.
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: <i>Chokin KUTZ</i>	DATE: 10-1988	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJECT: <i>Gen 190</i>	DATE: 8-9-84	
FINISH: WAVETEK PROCESS	RELEASE APPROV: <i>W. J. ...</i>	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX - STD ANGLES: 1:2, 1:3, 1:5	TITLE: SCHEMATIC GENERATOR BOARD (44)
SCALE: _____	DO NOT SCALE DWG	MODEL NO: 190 SERIES	FIG NO: 0103-00-2926
		CODE: 23338	REV: C

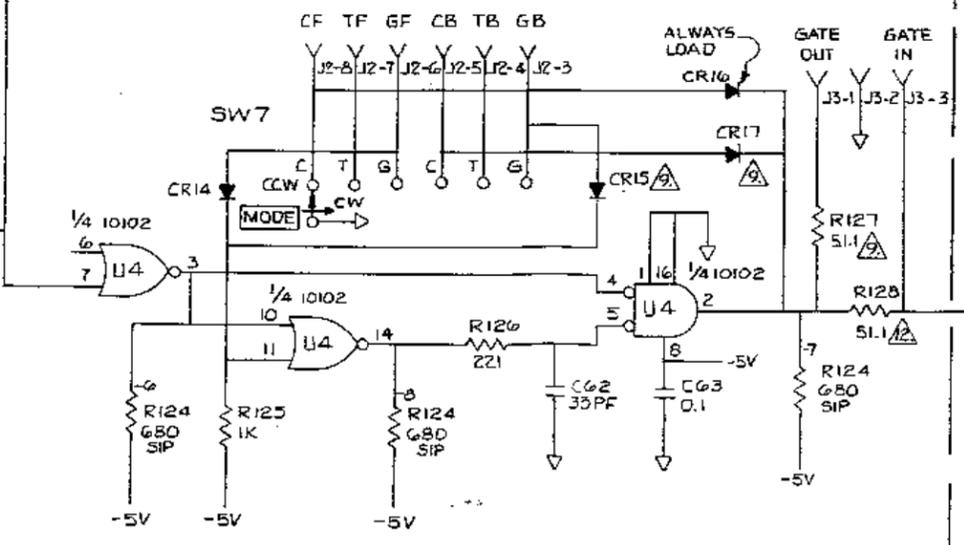
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FREQ MULT SW9-A

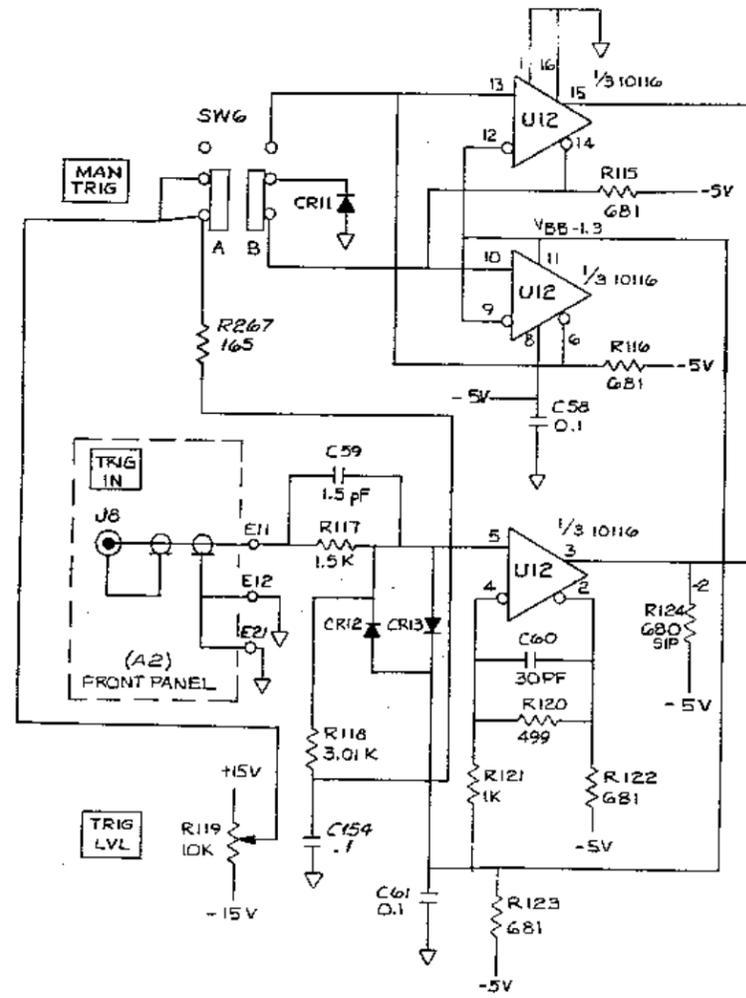
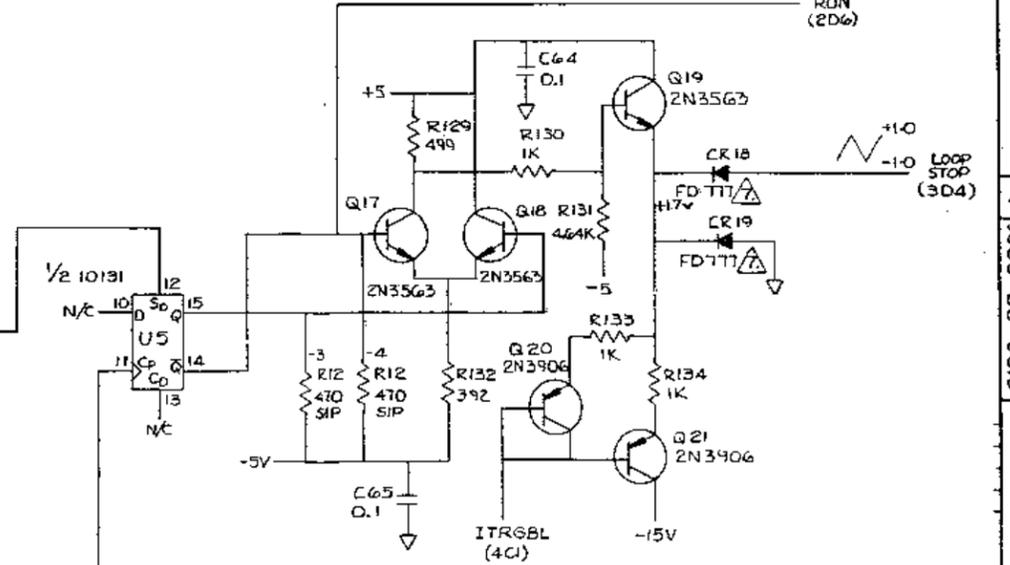
CAPACITANCE MULTIPLIER



TRIGGER



TRIG BASELINE



SEE NOTES SHEET 1.

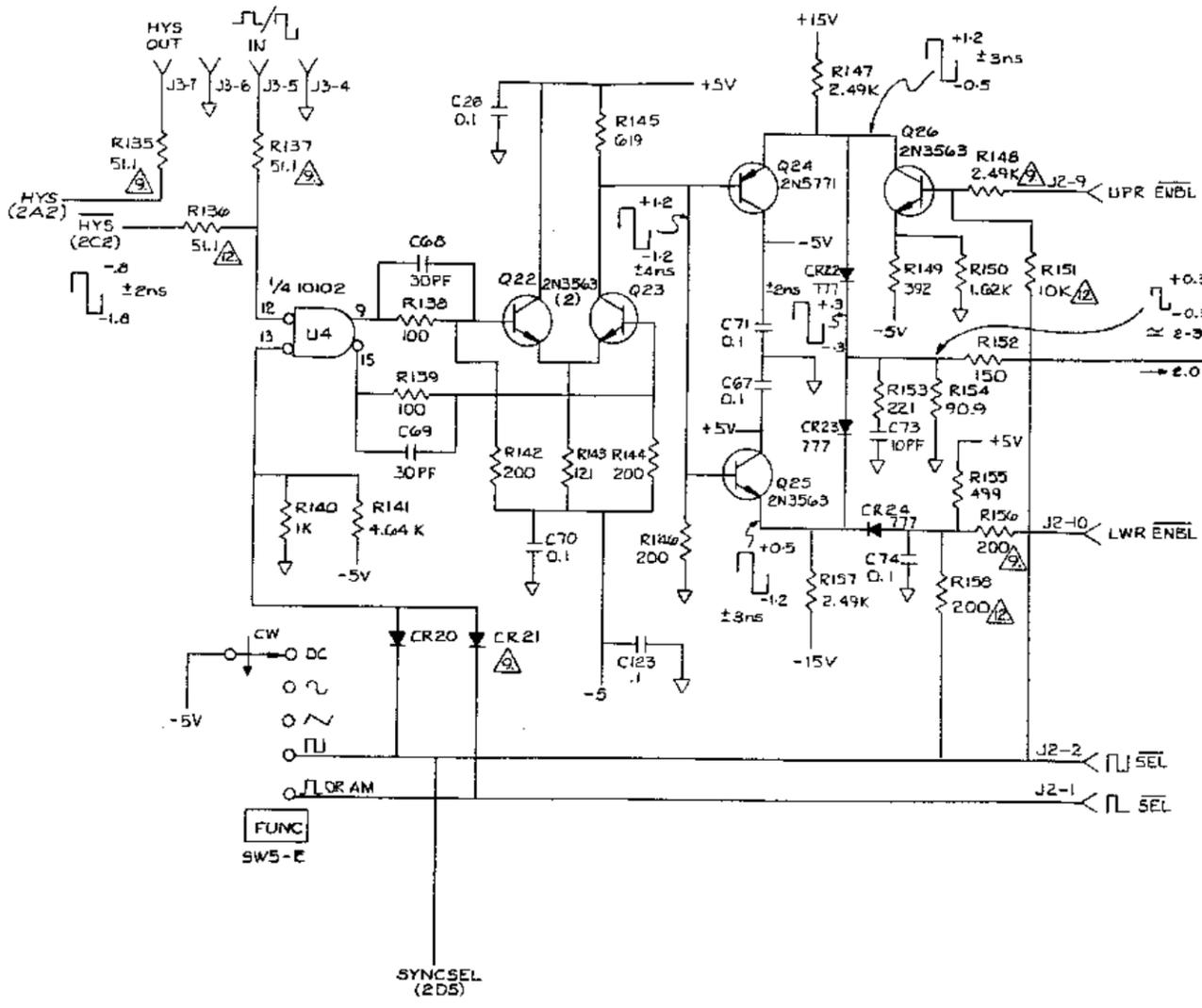
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES		DRAWN J. SHOPPER	DATE
MATERIAL		WORK IN PROGRESS	8-9-84
FINISH WAVE TEK PROCESS		TOLERANCE UNLESS OTHERWISE SPECIFIED	XXX: .010 ANGLES: 1:1
SCALE		DO NOT SCALE DWG	
TITLE SCHEMATIC GENERATOR BOARD (A4)		MODEL NO 130 SERIES	DWG NO 0103-00-2926 C
CODE IDENT 23338		SHEET 5 OF 7	

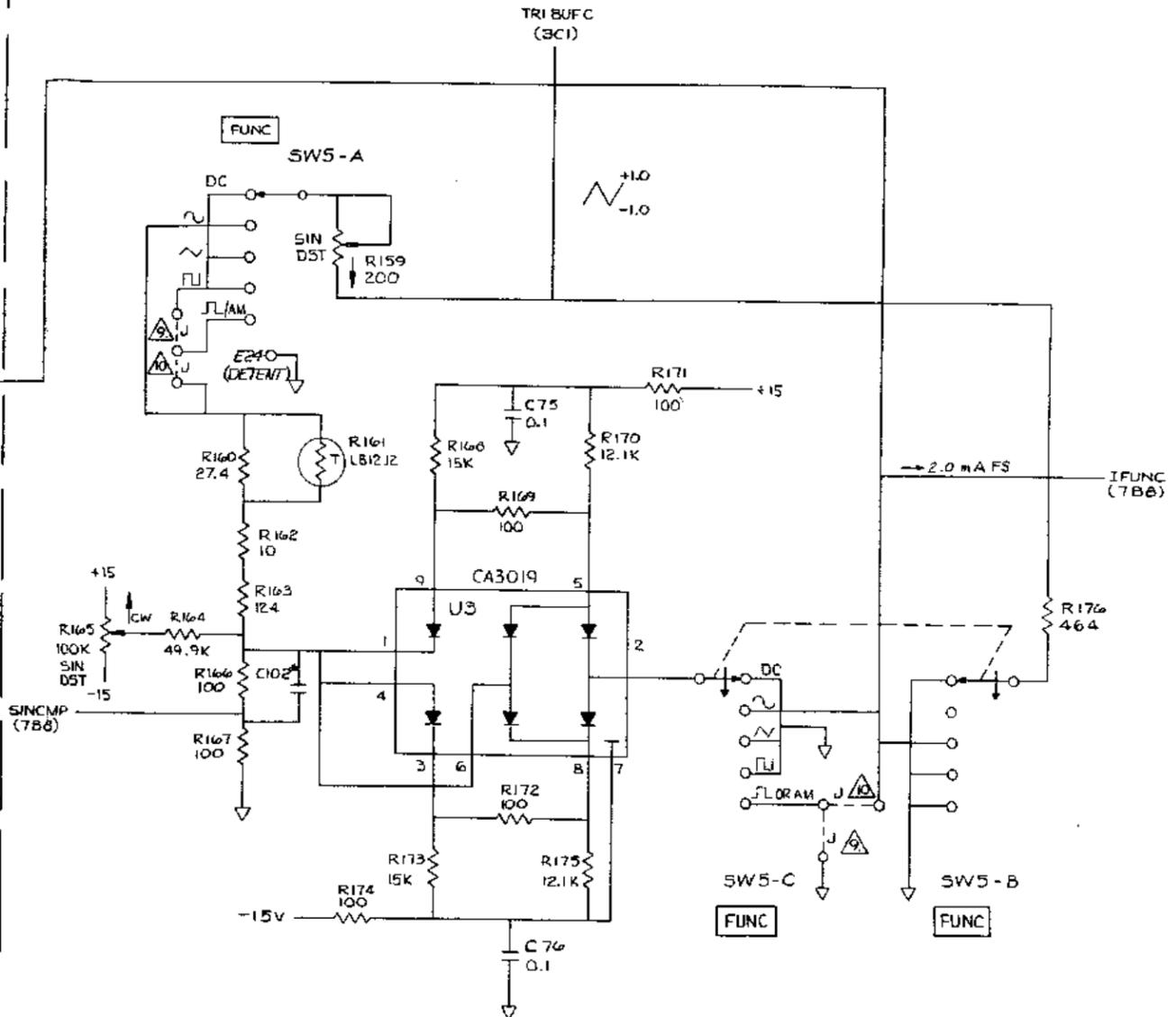
0103-00-2926 A

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SQUARE SHAPER



SINE CONVERTER



△ SEE NOTES SHEET I.
NOTE UNLESS OTHERWISE SPECIFIED

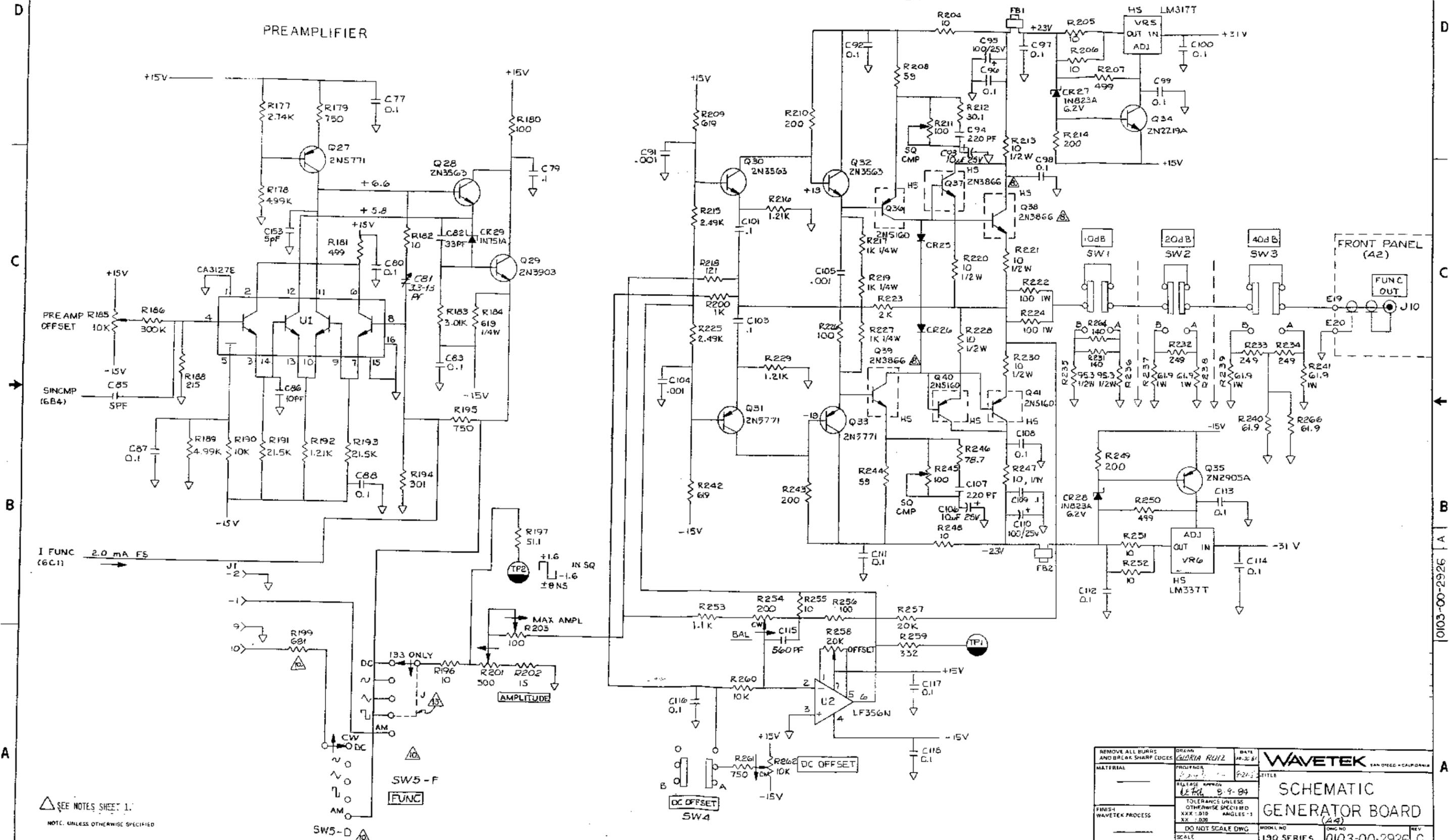
REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE: 10-1381	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	DESIGNED BY: GLORIA KUIZ	TITLE: SCHEMATIC GENERATOR BOARD (A2)
FINISH: WAVETEK PROCESS	RELEASE APPROV: [Signature]	MODEL NO: 150 SERIES
	DATE: 8-9-84	DWG NO: 0103-00-2926
	SCALE: DO NOT SCALE DWG	REV: C
	SCALE: [Blank]	CODE IDENT: 23338
		SHEET 6 OF 7

0103-00-2926

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OUTPUT AMPLIFIER

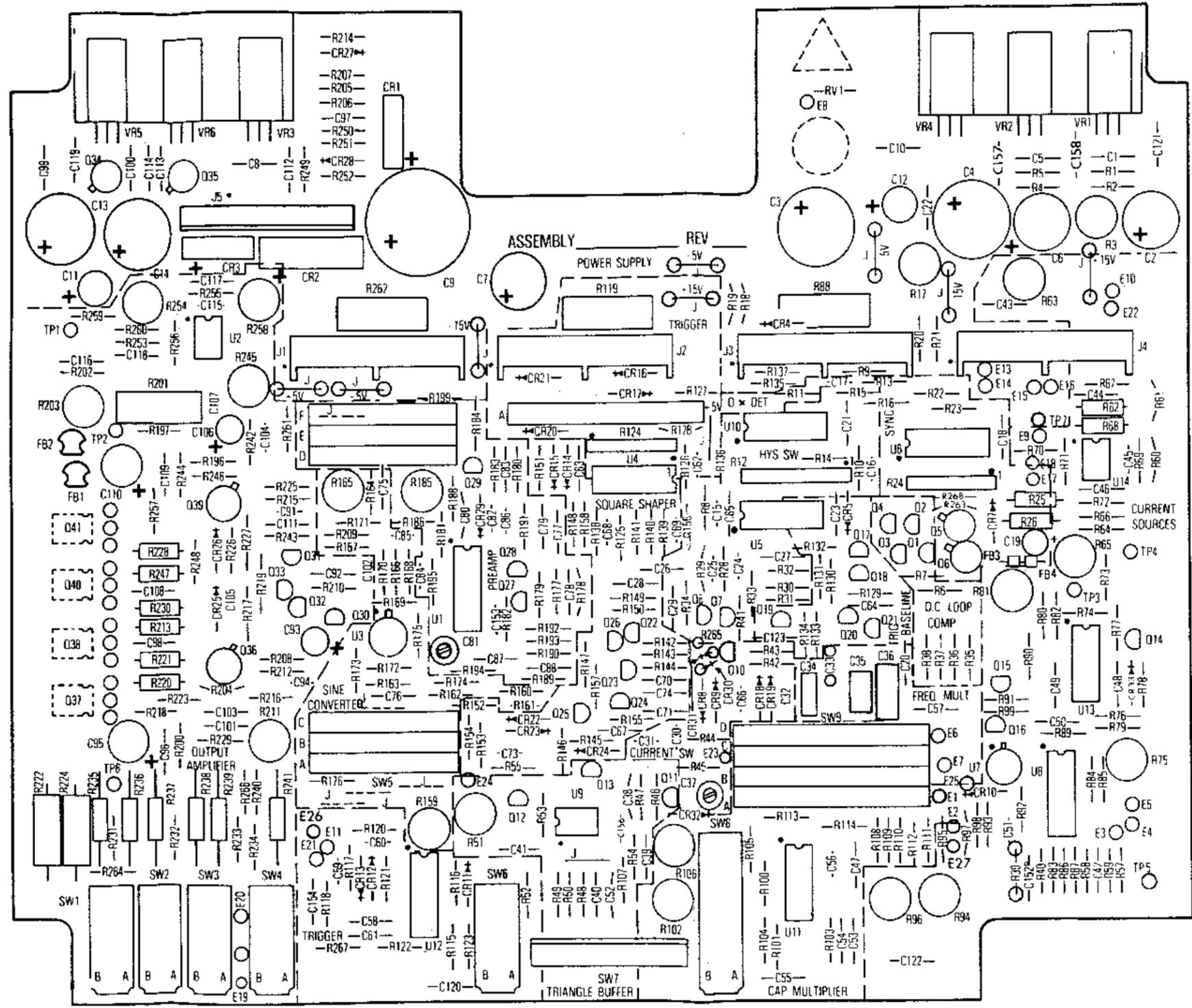
PREAMPLIFIER



SEE NOTES SHEET 1. NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DESIGN: GLORIA RUIZ	DATE: 10-2-81	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJ: 190	REV: 2	
FINISH: WAVETEK PROCESS	RELEASE: 8-9-84	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX: .010 ANGLES: 1 XX: .020	SCHEMATIC GENERATOR BOARD (42)
DO NOT SCALE DWG	SCALE	MOD: 190 SERIES	
		LOG: 23338	SHEET 7 OF 7

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See separate parts list 1100-00-2929

MADE FROM 0100-00-0834-3H

<p>WAVETEK</p>	
<p>PCA GENERATOR BOARD</p>	
<p>191</p>	<p>1100-00-2926</p>
<p>23338</p>	<p>SHEET 11</p>

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REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFOR-PART-NO	WFOR	WAVETEK NO.	QTY/PT
NONE	ASSY DRAWING			0101-00-2929	1
NONE	SCHEMATIC			0103-00-2926	1
NONE	SPK ASSY, XISTER MNTG BRACKET	190-0996	WVTK	1206-00-0996	1
NONE	SPK ASSY, BOARD MNTG ANGLE	190-1024	WVTK	1206-00-1024	1
NONE	ASSY, KIT PREWAVE LOAD 191-0950 REF #: 1208-00-1720	1208-00-2930	WVTK	1208-00-2930	1
C122	CAP. CER. NON. 1MF. 50V. AXIAL	CAC0325U104Z050A	CORNO	1500-01-0405	1
C33T	CAP. MICA. 56PF. 500V	DM15-560J	ARCO	1500-15-6000	1
C13	CAP. ELECT. 1000PF/50V RADIAL LEAD. SP .30	NRE102M50V16X25	NIC	1500-31-0203	1
J5	CONN. HEADER	1-640386-0	AMP	2100-02-0079	1
J1 J2 J3 J4	CONN. BOTTOM ENTRY, PC	09-32-3102	MOLEX	2100-02-0126	4
NONE	SOCKET, PIN	NS-430-25	ROBNU	2100-03-0064	4
TP1 TP2 TP3 TP4 TP5 TP6 TP7	BUSS BAR STANDOFF	2110-001	ARTMR	2100-03-0024	7
NONE	LAMP	L6750 LAMP	MURA	2400-02-0914	1
NONE	SUPER KIT	2500-0191-02	WVTK	2500-0191-02	1

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFOR-PART-NO	WFOR	WAVETEK NO.	QTY/PT
NONE	ASSY DRAWING			0101-00-2929	1
NONE	ASSY, PC BD PREPRED 191-0950 REF #: 1208-00-1721	1208-00-2931	WVTK	1208-00-2931	1
C153 C66T C85	CAP. CER. DISK. 3PF. 1KV. 10%	0311-0001B	WVTK	1500-00-3011	3
C156 C30 C73 C86	CAP. CER. 10PF. 1KV	DD-100	CRL	1500-01-0011	4
C31	CAP. CER. 100PF. 1KV	DD-101	CRL	1500-01-0111	1
C104 C105 C91	CAP. CER. .001UF. 1KV	DD-102	CRL	1500-01-0211	3
C1 C10 C100 C101 C103 C106 C109 C111 C112 C113 C114 C116 C117 C118 C119 C120 C121 C123 C152 C154 C157 C159 C18 C20 C21 C22 C23 C24 C27 C28 C29 C38 C39 C40 C41 C42 C43 C44 C46 C47 C48 C49 C5 C50 C52 C53 C54 C58 C61 C63 C64 C65 C67 C70 C71 C74 C75 C76 C77 C79 C8 C80 C83 C87 C88 C92 C94 C97 C99 C99	CAP. CER. NON. 1MF. 50V. AXIAL	CAC0325U104Z050A	CORNO	1500-01-0405	70
C102T	CAP. CER. 150PF. 1KV	DD-151	CRL	1500-01-3111	1
C59	CAP. CER. DISK. 1. 3PF. 1KV. TEMP COMP	NCD1. 3PF1KV750-CR	NIC	1500-01-5507	1

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFOR-PART-NO	WFOR	WAVETEK NO.	QTY/PT
C34	CAP. MYLAR. .0047MF. 50V	C58472F	ELPAC	1500-44-7203	1
C35	CAP. MYLAR. .047MF. 50V	C58473F	ELPAC	1500-44-7303	1
C36 C37	CAP. MYLAR. .47MF. 50V	C58474F	ELPAC	1500-44-7403	2
C37 C81	CAP VAR CER 3. 5/13PF 160V REF: 108. 0130	75-TRIND-02 3. 5/13PF(D	TRIKO	1500-51-3000	2
NONE	TRANSIPAD	10123N(OBS)	METRS	2800-11-0003	2
NONE	TRANSIPAD	531-218	DIVAR	2800-11-0004	2
F83 F84	FERRITE BEAD	56-590-63/39	FERRX	3100-00-0001	2
F81 F82	BALUN CORE	2873000902	FARIT	3100-00-0002	2
R17 R203 R211 R245 R96	POT. TRIM. 100	91AR100	BECK	4600-01-0103	5
R106 R185 R94	POT. TRIM. 10K	91AR10K	BECK	4600-01-0315	3
R165 R63 R65	POT. TRIM. 100K	91AR100K	BECK	4600-01-0402	3
R159 R254 R3	POT. TRIM. 200	91AR200	BECK	4600-02-0101	3
R102	POT. TRIM. 2K	91AR2K	BECK	4600-02-0201	1
R258 R51	POT. TRIM. 20K	91AR20K	BECK	4600-02-0301	2
R81	POT. TRIM. 300	91AR300	BECK	4600-05-0104	1
R213 R220 R221 R228 R230	RES. C. 1/2W. 5%. 10	RC-1/2-10J	STKPL	4700-23-0100	6

WAVETEK PARTS LIST
 TITLE: ASSY, PCA GENERATOR BD 191-0950
 ASSEMBLY NO. 1100-00-2929
 REV C
 PAGE 1

WAVETEK PARTS LIST
 TITLE: ASSY, KIT PREWAVE LOAD 191-0950
 ASSEMBLY NO. 1208-00-2930
 REV B
 PAGE 1

WAVETEK PARTS LIST
 TITLE: ASSY, KIT PREWAVE LOAD 191-0950
 ASSEMBLY NO. 1208-00-2930
 REV B
 PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFOR-PART-NO	WFOR	WAVETEK NO.	QTY/PT
NONE	SUPER KIT	2500-0191-03	WVTK	2500-0191-03	1
2	STANDOFF, SMADE .187L 2500DIA. 4-40, KNURL	BR6711SPB-0. 187-34	LYNTR	2800-06-0018	6
NONE	HEATSINK	209	WAVE	2800-11-0008	2
R201	POT. CONT. 500 FROM: 4600-05-0105	4609-75-0106	WVTK	4609-75-0106	1
R39T	RES. MF. 1/8W. 1%. 2. 21K	RN550-2211F	TRW	4701-03-2211	1
R222	RES. MF. 1W. 1%. 100	RN700-1000F	TRW	4701-03-1000	1
Q40 Q41	TRANS	2N5160-18(OBS)	NOT	4901-05-1600	2
Q37 Q38	TRANS. SEL. 2N3866 QTY: 1: 4901-03-5660	4998-00-0051	WVTK	4998-00-0051	2
SW1 SW2 SW3 SW4	SWITCH	5102-00-0009	WVTK	5102-00-0009	4
SW6	SWITCH, 2PDT. MOM.	5102-00-0010	WVTK	5102-00-0010	1
SW8	SWITCH, 4PDT. P-P	5102-00-0011	WVTK	5102-00-0011	1
NONE	BUTTON, CONICAL	F01-01(BLACK)	SHADM	5103-04-0006	6
R161	THERMISTOR 18. 6 OHMS +/-25% CUST COATED	155-180FAK-801	FENAL	5300-00-0002	1

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFOR-PART-NO	WFOR	WAVETEK NO.	QTY/PT
C17	CAP. CER. 22PF. 1KV	DD-220	CRL	1500-02-2011	1
C107 C94	CAP. CER. 220PF. 1KV	DD-221	CRL	1500-02-2111	2
C16 C24 C25 C60 C68 C69	CAP. CER. 30PF. 1KV	DD-300	CRL	1500-03-0001	6
C45 C51 C62 C82	CAP. CER. 33PF. 1KV	DD-330	CRL	1500-03-3011	4
C56	CAP. CER. .005MF. 50V	CK-302	CRL	1500-05-0210	1
C115	CAP. CER. 560PF. 1KV	DD-561SLL	CRL	1500-05-6101	1
C13	CAP. MICA. 150PF. 300V	DM15-151J	ARCO	1500-11-3100	1
C32	CAP. MICA. 560PF. 300V	CD15FC561F03	CDE	1500-15-6102	1
C106 C19 C93	CAP. ELECT. 10MF/25V RADIAL LEAD. SP .10	NRE 10/63	NIC	1500-31-0002	3
C11 C110 C12 C2 C6 C95	CAP. ELECT. 100MF. 35V RADIAL LEAD. SP .20	NRE101M33V10X12. 5	NIC	1500-31-0102	6
C14 C3 C4	CAP. ELECT. 1000MF/30V RADIAL LEAD. SP .30	NRE102M50V16X25	NIC	1500-31-0203	3
C7	CAP. ELECT. 2200PF. 16V RADIAL LEAD. SP .30	ECEA1CV2228C	PANAS	1500-32-2201	1
C9	CAP. ELECT. 16V RADIAL LS .40	NRE682M16V22Y41	NIC	1500-36-8201	1
C55	CAP. MYLAR. 1MF. 100V	225P10491WDS	SPRAQ	1500-41-0444	1

REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFOR-PART-NO	WFOR	WAVETEK NO.	QTY/PT
R247	RES. C. 1/2W. 5%. 2. 7M	RC-1/2-275J	STKPL	4700-23-2704	1
R68	RES. C. 1/2W. 5%. 3. 9M	RC-1/2-395J	STKPL	4700-23-3904	1
R62	RES. MF. 1/8W. 1%. 100	RN350-1000F	TRW	4701-03-1000	16
R103 R138 R139 R166 R167 R169 R171 R172 R174 R180 R226 R296 R28 R29 R89 R95	RES. MF. 1/8W. 1%. 10K	RN550-1001F	TRW	4701-03-1001	24
R10 R121 R125 R130 R133 R134 R14 R140 R15 R200 R23 R46 R48 R53 R6 R74 R82 R83 R84 R85 R86 R87 R93 R97	RES. MF. 1/8W. 1%. 10K	RN550-1002F	TRW	4701-03-1002	5
R190 R260 R36 R67 R69	RES. MF. 1/8W. 1%. 100K	RN550-1003F	TRW	4701-03-1003	1
R110	RES. MF. 1/8W. 1%. 1M	RN550-1004F	TRW	4701-03-1004	3
R111 R52T R64	RES. MF. 1/8W. 1%. 10	5043ED10R100F	MEPCO	4701-03-1009	15
R104 R113 R162 R182 R196 R204 R205 R206 R248 R251 R252 R255 R45 R54 R55	RES. MF. 1/8W. 1%. 1. 1K	RN550-1101F	TRW	4701-03-1101	2
R21 R253	RES. MF. 1/8W. 1%. 121	RN550-1210F	TRW	4701-03-1210	4
R1 R143 R218 R5	RES. MF. 1/8W. 1%. 1. 21K	RN550-1211F	TRW	4701-03-1211	6
R16 R192 R2 R216 R229 R4	RES. MF. 1/8W. 1%. 12. 1K	RN550-1212F	TRW	4701-03-1212	2
R170 R175					

WAVETEK PARTS LIST
 TITLE: ASSY, PCA GENERATOR BD 191-0950
 ASSEMBLY NO. 1100-00-2929
 REV C
 PAGE 2

WAVETEK PARTS LIST
 TITLE: ASSY, KIT PREWAVE LOAD 191-0950
 ASSEMBLY NO. 1208-00-2930
 REV B
 PAGE 2

WAVETEK PARTS LIST
 TITLE: ASSY, KIT PREWAVE LOAD 191-0950
 ASSEMBLY NO. 1208-00-2930
 REV B
 PAGE 4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	
MATERIAL	PROJECTOR		
FINISH WAVETEK PROCESS	RELEASE APPROV		
SCALE	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: 010 ANGLES: 1 XX: 1:30 DO NOT SCALE DWG		
TITLE: PARTS LIST PCA, GENERATOR			
MODEL NO. 191	DWG NO. 1100-00-2929	REV. C	
CODE 23338	SHEET 1	OF 3	

NOTE: UNLESS OTHERWISE SPECIFIED

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REV EGN BY DATE APP

Table with columns: REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFGOR-PART-NO, MFGOR, WAVETEK NO., QTY/PT. Rows include R163 R31, R38, R231 R264, R152, R114 R117, R168 R173, R202 R34, R150, R267, R8, R142 R144 R146 R156 R210, R214 R243 R249 R30 R32 R73, R223 R35T R40, R257 R59, R188, R191 R193, R126 R153.

Table with columns: REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFGOR-PART-NO, MFGOR, WAVETEK NO., QTY/PT. Rows include R131 R141 R22, R44 R57, R120 R129 R155 R181 R207, R250 R41, R100 R109 R178 R189 R71 R72, R164 R98, R127 R135 R137 R197 R9, R80, R200 R244, R70, R145 R209 R242, R240 R266, R115 R116 R122 R123, R13, R263 R268, R179 R195 R261 R42 R43, R246 R47.

Table with columns: REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFGOR-PART-NO, MFGOR, WAVETEK NO., QTY/PT. Rows include 1N823, CR32 CR33, CR7, CR1 CR3, CR22 CR23 CR24, CR10 CR11 CR12 CR13 CR14, CR15 CR16 CR17 CR20 CR21, CR25 CR26 CR4 CR5, CR30 CR31 CR8 CR9, CR18 19, CR2, RV1, G34, G5 G6.

WAVETEK PARTS LIST, TITLE: ASSY. KIT PREHAME LOAD 191-0950, ASSEMBLY NO. 1208-00-2930, REV B, PAGE 5

WAVETEK PARTS LIST, TITLE: ASSY. KIT PREHAME LOAD 191-0950, ASSEMBLY NO. 1208-00-2930, REV B, PAGE 7

WAVETEK PARTS LIST, TITLE: ASSY. KIT PREHAME LOAD 191-0950, ASSEMBLY NO. 1208-00-2930, REV B, PAGE 9

Table with columns: REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFGOR-PART-NO, MFGOR, WAVETEK NO., QTY/PT. Rows include R11 R37T, R18, R20 R232 R233 R234 R265, R147 R148 R157 R215 R225, R66 R78 R91, R107, R177, R140, R194, R118 R183 R49 R50 R7 R79, R92 R99, R186, R212, R259, R19, R77 R90, R132 R149, R176 R33.

Table with columns: REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFGOR-PART-NO, MFGOR, WAVETEK NO., QTY/PT. Rows include R60, R101, R108, R154, R217 R219 R227, R25 R26, R184, R235 R236, R224, R237 R238 R239 R241, R12, R124 R24, R112, CR29, CR27 CR28.

Table with columns: REFERENCE DESIGNATORS, PART DESCRIPTION, ORIG-MFGOR-PART-NO, MFGOR, WAVETEK NO., QTY/PT. Rows include G35, G12 G13 G17 G18 G19 G22 G23, G29 G26 G28 G3 G30 G32 G4, G7 G8, G10, G29, G14, G15 G16 G20 G21, G36, G11, G1 G2 G24 G27 G31 G33, G7, G39, G9.

WAVETEK PARTS LIST, TITLE: ASSY. KIT PREHAME LOAD 191-0950, ASSEMBLY NO. 1208-00-2930, REV B, PAGE 6

WAVETEK PARTS LIST, TITLE: ASSY. KIT PREHAME LOAD 191-0950, ASSEMBLY NO. 1208-00-2930, REV B, PAGE 8

WAVETEK PARTS LIST, TITLE: ASSY. KIT PREHAME LOAD 191-0950, ASSEMBLY NO. 1208-00-2930, REV B, PAGE 10

NOTE UNLESS OTHERWISE SPECIFIED

WAVETEK SAN DIEGO - CALIFORNIA. PARTS LIST PCA, GENERATOR. DRAWN, DATE, PROJ/ENGR, RELEASE APPROV, TOLERANCE UNLESS OTHERWISE SPECIFIED, DO NOT SCALE DWG, SCALE, MODIFY NO, DWG NO, REV, CORD IDENT, SHEET 2 OF 3.

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REV	ECO	BY	DATE	APP
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
U11 U13	OP AMP. DUAL JFET INPUT	TL082CN	TI	7000-00-8300	2
U14	OP AMP. WIDE BANDWIDTH DUAL JFET INPUT	LF353N	NSC	7000-03-5300	1
U2	OP-AMP	LF356N	NSC	7000-03-5600	1
U3	DIODE ULTRA FAST LD CAPAC "08S 4/19/91"	CA3019(08S)	HARRIS	7000-30-1900	1
U8	TRANS ARRAY, GENERAL PURPOSE, NPN	CA3083	RCA	7000-30-8300	1
U1	TRANS ARRAY, HIGH FREQ. NPN	CA3127E	RCA	7000-31-2700	1
U4 U6	GATE, NOR, QUAD 2 IMP, ECL	MC10102	MTI	8001-01-0200	2
U10 U12	RCVR, TRI LINE, ECL	MC10116P	MTI	8001-01-1600	2
U5	FLIP-FLOP DUAL, ECL	MC10131	MTI	8001-01-3100	1

WAVETEK PARTS LIST
 TITLE: ASSY. KIT PREWAVE LOAD 191-0950
 ASSEMBLY NO. 1200-00-2930
 PAGE 11
 REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
NONE	ASSY. SWITCH SW3-0950	191-1723	WVTK	1202-00-1723	1
NONE	ASSY. SWITCH SW7-0950	191-1724	WVTK	1202-00-1724	1
NONE	ASSY. SWITCH SW9-0950	191-1725	WVTK	1202-00-1725	1

WAVETEK PARTS LIST
 TITLE: SUPER KIT
 ASSEMBLY NO. 2500-0191-02
 PAGE 1
 REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFR-PART-NO	MFR	WAVETEK NO.	QTY/PT
NONE	CHASSIS CABLE KIT	191-0954	WVTK	1207-00-0954	1
NONE	KIT, WIRE/HARNES-191	191-1722	WVTK	1207-00-1722	1

WAVETEK PARTS LIST
 TITLE: SUPER KIT
 ASSEMBLY NO. 2500-0191-03
 PAGE 1
 REV

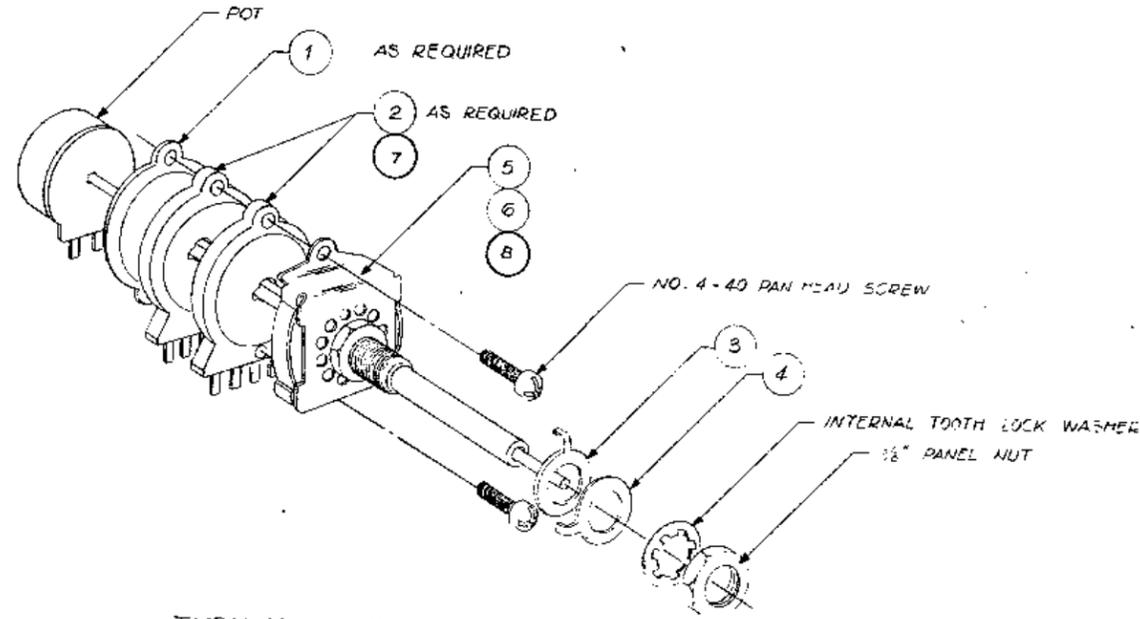
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK <small>1340000 • CALIFORNIA</small>	
MATERIAL	CHECKED		TITLE	
	PROJ ENGR		PARTS LIST	
	RELEASE APPROV		PCA, GENERATOR	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TO 3 DECIMALS ARE FRACTIONS DECIMALS ANGLES XX' XX"		SIZE	DWG. NO.
DO NOT SCALE DRAWING	SCALE	MODEL	191	1100-00-2929
		SHEET	3	OF 3

NOTE: UNLESS OTHERWISE SPECIFIED

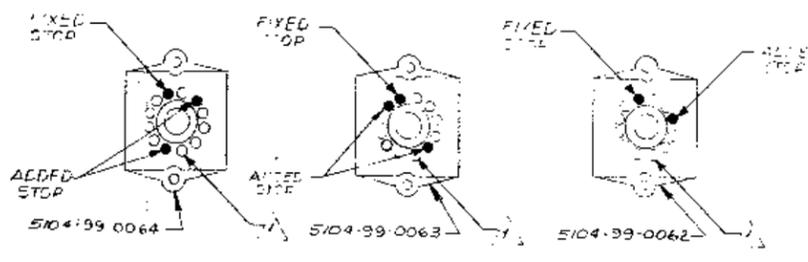
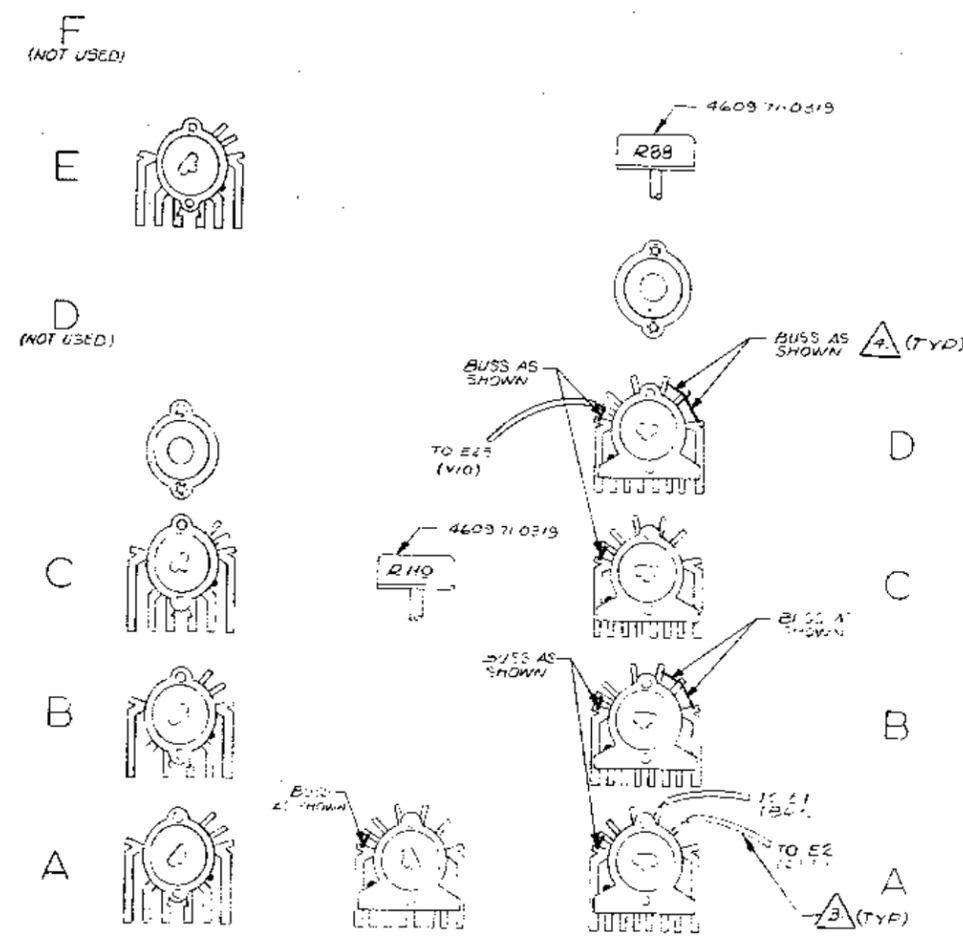
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4609-71-0319
R262

REV	EN	BY	DATE	APP



TYPICAL SWITCH HARDWARE STACK-UP



SW 5
WIRING DETAIL
WAFER A,B,C
4-40 X 3/4\"/>

SW 7
WIRING DETAIL

SW 9
WIRING DETAIL
WAFER A,B,C,E
4-40 X 7/8\"/>

- 1. ALL BUS WIRE #24 AWG
- 2. WIRES OBTAINED FROM CHASSIS CABLE KIT 1207-00-0954.
- 3. ALL WAFERS SHOWN IN CCW POSITION.
- 4. PLACE DETENT 6 POSITIONS AS SHOWN FROM CCW FIXED STOP BEFORE INSTALLING ADDED STOP.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARPEDEDGES	DRW: FN ALJINC	DATE: 10/2/81	WAVETEK SAN DIEGO, CA, U.S.A.
MATERIAL	PROJ: 102	REV: 1	
FINISH: WAVETEK PROCESS	RELEASE APPROV: [Signature]	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX - .010 ANGLES: XX - .030	TITLE: ASSEMBLY SWITCH DETENT GENERATOR BOARD
SCALE	DO NOT SCALE DWG	MORTEL NO: 191	DWG NO: 0102 00-0001 COOK: 23338 SHEET: 1 OF 1

REV	ECN	BY	DATE	APP
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REFERENCE DESIGNATORS	PART DESCRIPTION	DR10-WFOR-PART-NO	WFOR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. GENERATOR SWITCHES	0102-00-0953	WVTK	0102-00-0953	1
NONE	BRKT	133-305	WVTK	1400-00-1673	1
1	PLATE, SW	008-004	WVTK	1400-00-2130	2
R119 R262 R88	PDT. CONT. 1DK FROM: 4600-01-0312	4609-71-0319	WVTK	4609-71-0319	3
2	WAFER	133-SW1-1	WVTK	5104-02-0008	4
7	WAFER	147-400	WVTK	5104-02-0015	5
3	SWITCH STOP	211-33-001	CTS	5104-07-0001	3
4	SWITCH STOP	212-33-006	CTS	5104-07-0002	3
5	DETENT, MOD FROM: 5104-01-0010	5104-99-0062	WVTK	5104-99-0062	1
6	DETENT, MOD FROM: 5104-01-0010	5104-99-0063	WVTK	5104-99-0063	1
8	DETENT, MOD FROM: 5104-01-0010	5104-99-0064	WVTK	5104-99-0064	1

WAVETEK PARTS LIST
 TITLE: ASSY. GENERATOR SWITCHES
 ASSEMBLY NO. 1202-00-0953
 REV A
 PAGE 1

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA TITLE PARTS LIST ASSY. GENERATOR SWITCHES
MATERIAL	PROJ ENGR		
	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - .010 ANGLES - 1 .XX - .000		
FINISH WAVETEK PROCESS	DO NOT SCALE DWG	MODEL NO	
	SCALE	191	DWG NO 1202-00-0953
		CODE 23338	REV A
			SHEET 1 OF 1

NOTE: UNLESS OTHERWISE SPECIFIED

D
C
B
A

D
C
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A

8 7 6 5 4 3 2

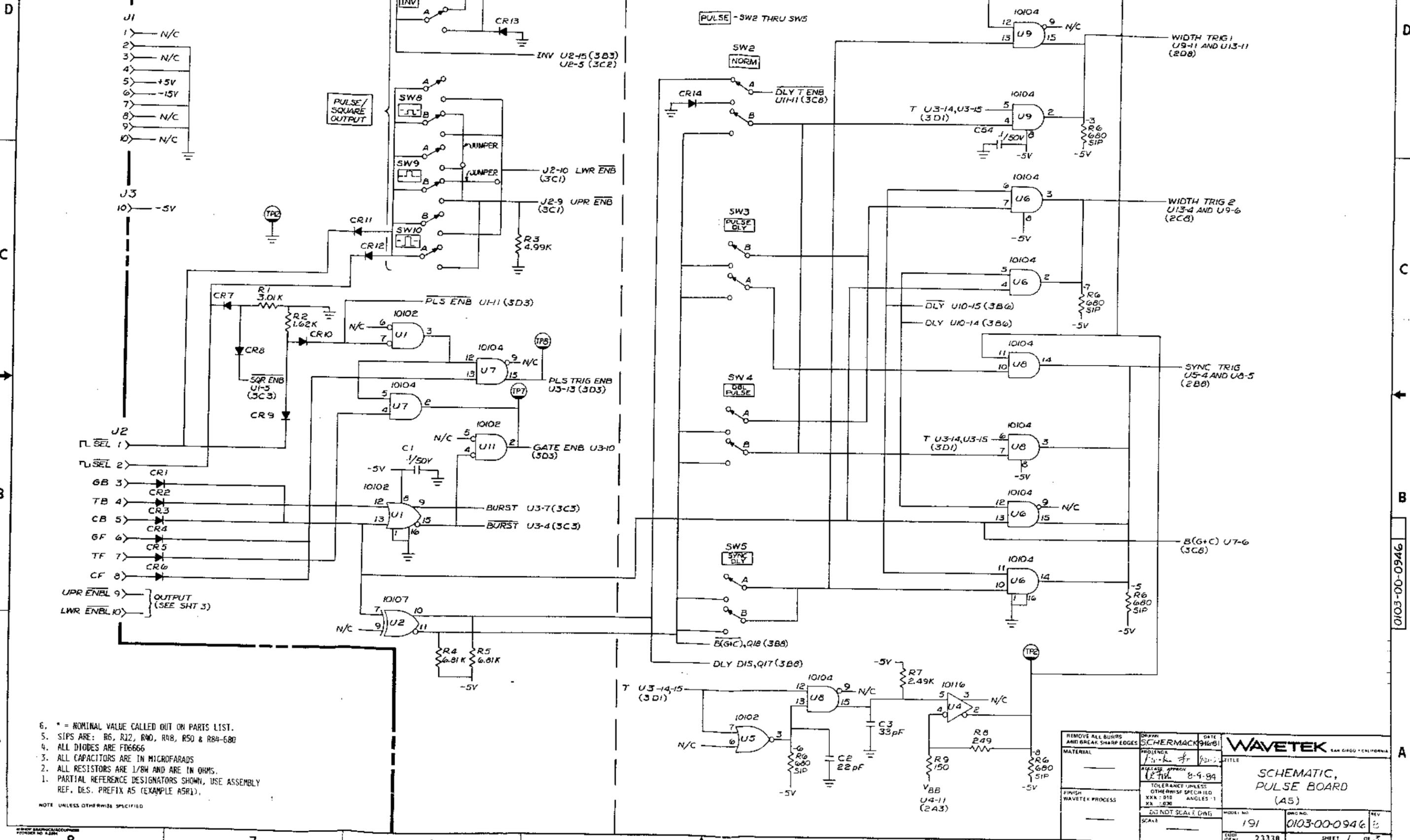
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REV	ECN	BY	DATE	APP
A	ECA# 3391	RD	10/27/87	
B	*7553	DAV	1/28/88	JRE

SWITCH POSITION DECODING LOGIC

ONE SHOT TRIGGER STEERING LOGIC

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- 6. * = NOMINAL VALUE CALLED OUT ON PARTS LIST.
 - 5. SIPS ARE: R6, R12, R40, R48, R50 & R84-680
 - 4. ALL DIODES ARE FD6666
 - 3. ALL CAPACITORS ARE IN MICROFARADS
 - 2. ALL RESISTORS ARE 1/8W AND ARE IN OHMS.
 - 1. PARTIAL REFERENCE DESIGNATORS SHOWN, USE ASSEMBLY REF. DES. PREFIX AS (EXAMPLE ASR1).
- NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE: 8-9-84					
MATERIAL	TITLE: SCHEMATIC, PULSE BOARD (A5)					
FINISH WAVETEK PROCESS	SCALE: 1:1	<table border="1"> <tr> <td>MODEL NO: 191</td> <td>REV: 2</td> </tr> <tr> <td>ECN: 23338</td> <td>SHEET 1 OF 3</td> </tr> </table>	MODEL NO: 191	REV: 2	ECN: 23338	SHEET 1 OF 3
MODEL NO: 191	REV: 2					
ECN: 23338	SHEET 1 OF 3					

0103-00-0946

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REV ECN BY DATE APP

WIDTH ONE SHOT

WIDTH TRIG 1
U9-2, U9-15
(1 D2)

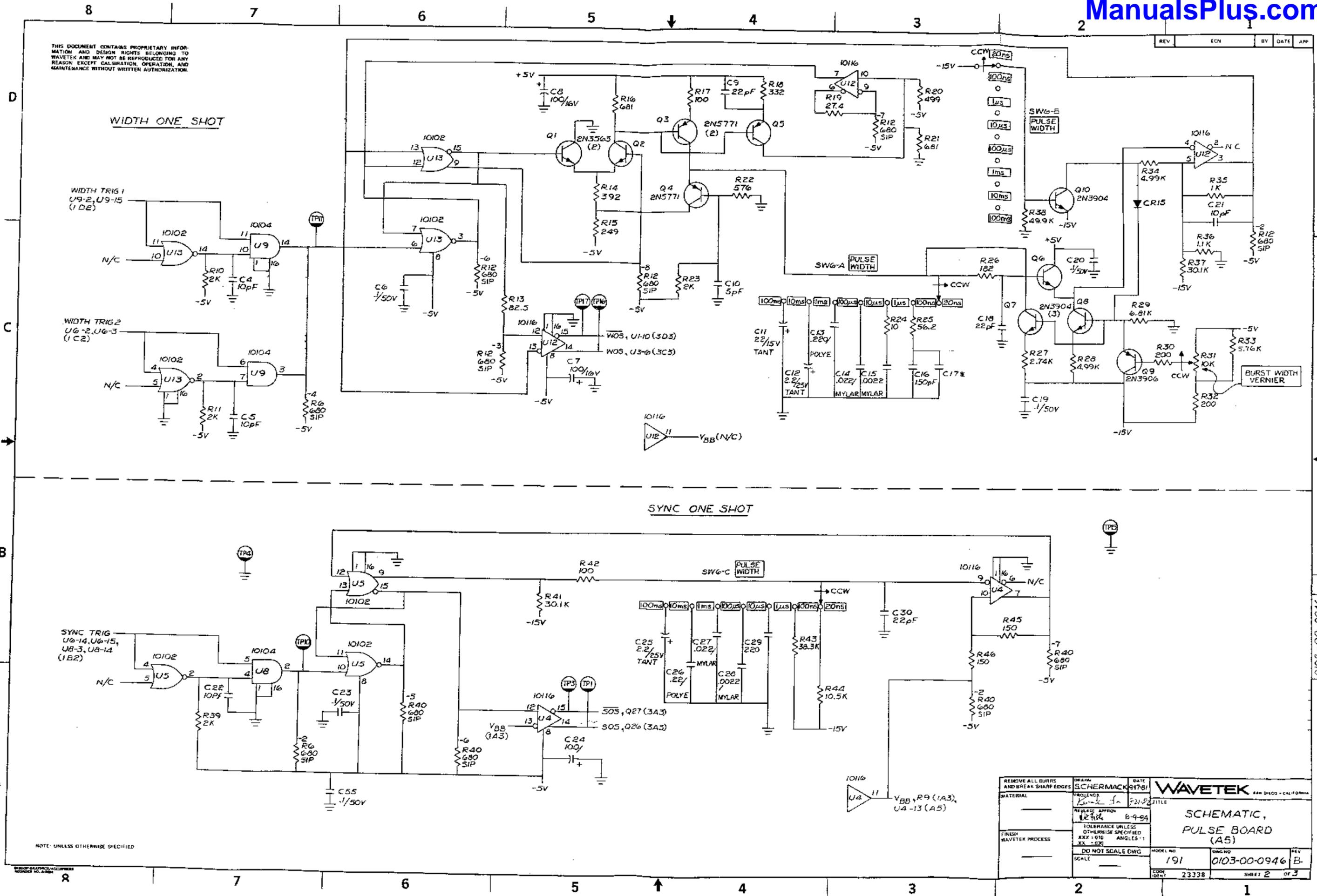
WIDTH TRIG 2
U6-2, U6-3
(1 C2)

SYNC ONE SHOT

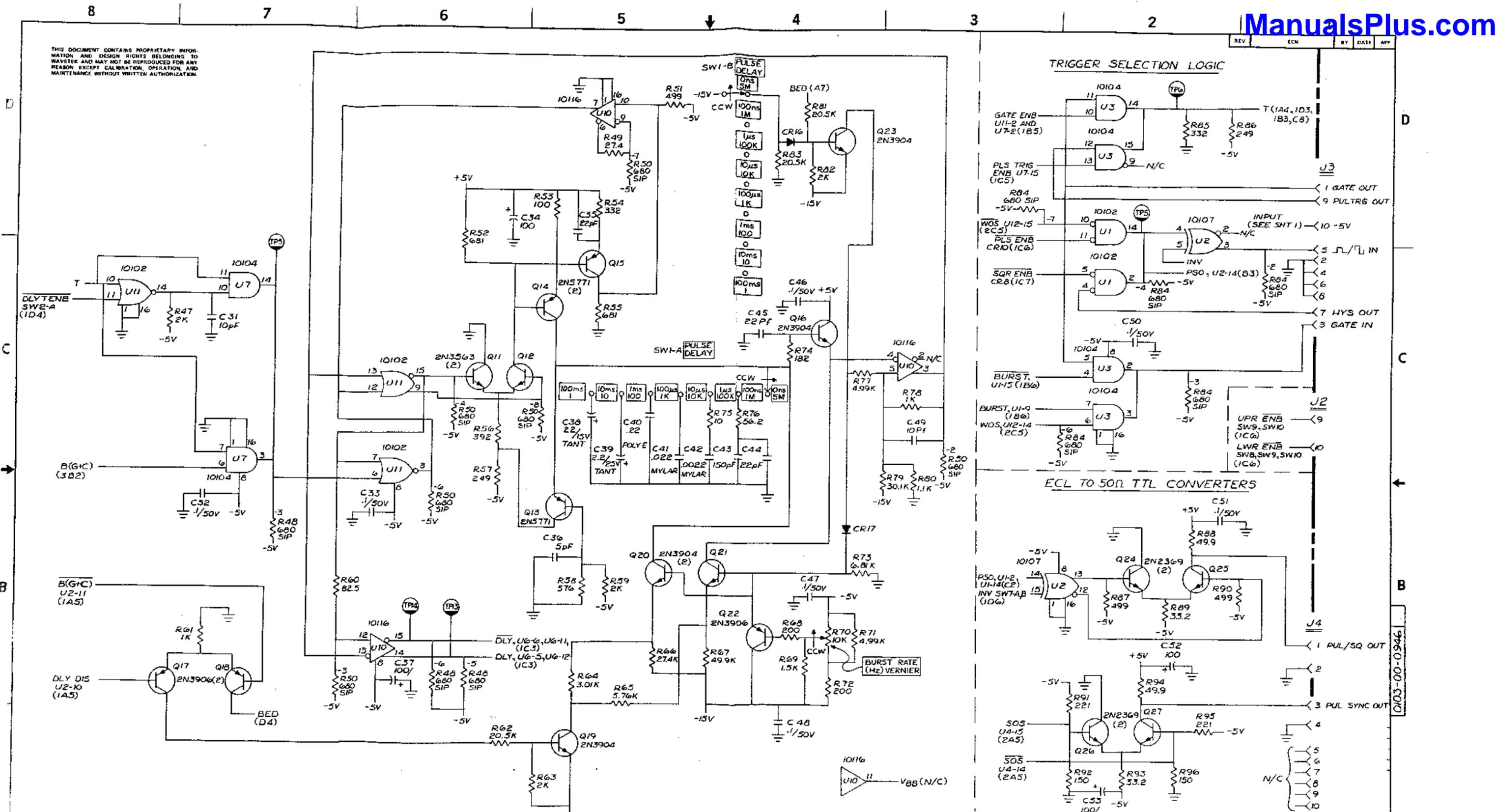
SYNC TRIG
U6-14, U6-15,
U8-3, U8-14
(1 B2)

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN SCHEMACK	DATE 9/7/81	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJECT Kornel In	DATE 8-9-81	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES - 1 XX : 030		SCHEMATIC, PULSE BOARD (A5)
SCALE	DO NOT SCALE DWG	MODEL NO 191	
		DWG NO 0103-00-0946	REV B.
		CODE 23338	SHEET 2 OF 3

NOTE: UNLESS OTHERWISE SPECIFIED



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DELAY ONE SHOT BURST OSCILLATOR

TRIGGER SELECTION LOGIC

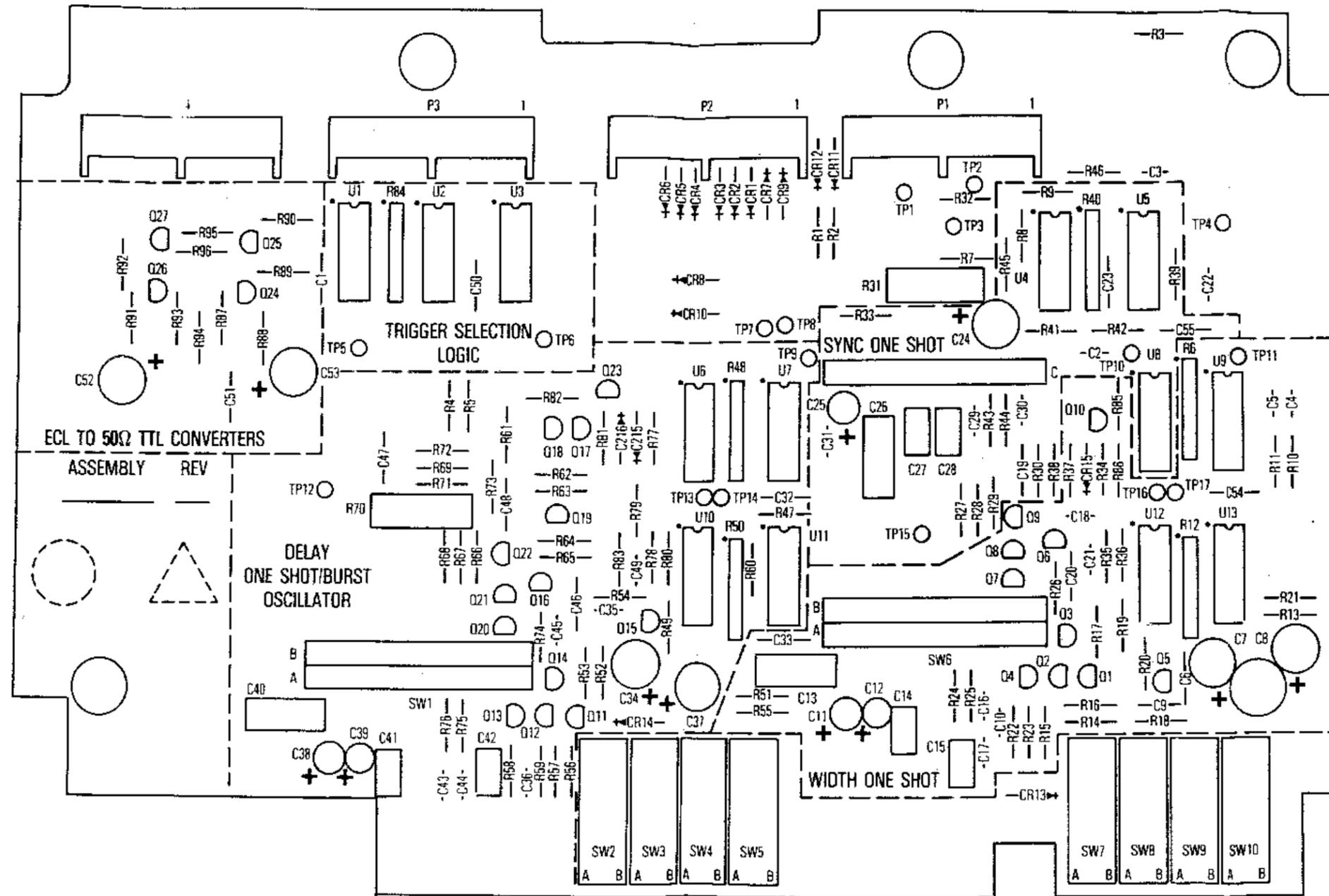
ECL TO 50 Ohm TTL CONVERTERS

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES		DATE	8/1/81	
DRAWN		SCHERMACK	8-9-81	
MATERIAL		PREPARED BY	8-9-81	TITLE
FINISH		WAVETEK PROCESS	DO NOT SCALE DWG	SCHEMATIC PULSE BOARD (A5)
SCALE	191	MODEL NO	0103-00-0946	REV
SCALE	23338	CODE IDENT	SHEET 3	OF 3

0103-00-0946

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



MADE FROM 0100-00-0946 REV. B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA	
	PROJENGR			
FINISH WAVETEK PROCESS	RELEASE APPROV		TITLE PULSE BOARD	
	SCALE		TOLERANCE UNLESS OTHERWISE SPECIFIED KX - .10 A.L. - .00	
	DO NOT SCALE DWG	MODEL NO 191	DWG NO 1100-00-0946	REV
		COOR IDENT	23338	SHEET 1 OF 1

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REV	ECN	BY	DATE	APP
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REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-REFR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. PULSE BD	0101-00-0946	WVTK	0101-00-0946	1
NONE	SCHEMATIC, PULSE BD	0103-00-0946	WVTK	0103-00-0946	1
NONE	ASSY, SWITCHES PULSE	191-0966	WVTK	1202-00-0966	1
NONE	ASSY, SWITCH BRKT	190-0984	WVTK	1206-00-0984	2
C10 C36	CAP, CER, 5PF, 1KV	00-030	ERL	1500-00-5011	2
C21 C22 C31 C4 C49 C5	CAP, CER, 10PF, 1KV	00-100	ERL	1500-01-0011	6
C1 C19 C20 C23 C32 C33 C46 C47 C48 C50 C51 C54 C55 C6	CAP, CER, MON., 1MF, 50V	CAC0325UL04Z050A	CORNG	1500-01-0405	14
C16 C43	CAP, CER, 150PF, 1KV	00-151	ERL	1500-01-5111	2
C18 C2 C30 C35 C44 C45 C9	CAP, CER, 22PF, 1KV	00-220	ERL	1500-02-2011	7
C29	CAP, CER, 220PF, 1KV	00-221	ERL	1500-02-2111	1
C177 C3	CAP, CER, 33PF, 1KV	00-330	ERL	1500-03-3011	2
C24 C24 C37 C32 C53 C7 C8	CAP, ELECT, 100WF, 25V RADIAL LEAD, SF, 20	ULB1V101M	NICH	1500-31-0102	7
C15 C28 C42	CAP, MYLAR, .0022MF100V	22P22291M03	SPRAO	1500-42-2214	3
C14 C27 C41	CAP, MYLAR, .022MF100V	22P22391M03	SPRAO	1500-42-2314	3
C13 C26 C40	CAP, POLYE., 22MF, 80V	192P2249M8	SPRAO	1500-42-2403	3
C12 C20 C39	CAP, TANT, 2.2MF, 25V	196D225X9025M41	SPRAO	1500-72-2502	3

REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-REFR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
R91 R95	RES, MF, 1/8W, 1%, 221	RN550-2210F	TRW	4701-03-2210	2
R15 R57 R8 R86	RES, MF, 1/8W, 1%, 249	RN550-2490F	TRW	4701-03-2490	4
R7	RES, MF, 1/8W, 1%, 2.49K	RN550-2491F	TRW	4701-03-2491	1
R27	RES, MF, 1/8W, 1%, 2.74K	RN550-2741F	TRW	4701-03-2741	1
R66	RES, MF, 1/8W, 1%, 27.4K	RN550-2742F	TRW	4701-03-2742	1
R19 R49	RES, MF, 1/8W, 1%, 27.4	RN550-2784F	TRW	4701-03-2749	2
R1 R64	RES, MF, 1/8W, 1%, 3.01K	RN550-3011F	TRW	4701-03-3011	2
R37 R41 R79	RES, MF, 1/8W, 1%, 30.1K	RN550-3012F	TRW	4701-03-3012	3
R18 R34 R85	RES, MF, 1/8W, 1%, 332	RN550-3320F	TRW	4701-03-3320	3
R89 R93	RES, MF, 1/8W, 1%, 33.2	RN550-3322F	TRW	4701-03-3329	2
R43	RES, MF, 1/8W, 1%, 33.3K	RN550-3332F	TRW	4701-03-3332	1
R14 R56	RES, MF, 1/8W, 1%, 392	RN550-3920F	TRW	4701-03-3920	2
R20 R31 R87 R90	RES, MF, 1/8, 1%, 499	RN550-4990F	TRW	4701-03-4990	4
R28 R3 R34 R71 R77	RES, MF, 1/8W, 1%, 4.99K	RN550-4991F	TRW	4701-03-4991	5
R38 R67	RES, MF, 1/8W, 1%, 49.9K	RN550-4992F	TRW	4701-03-4992	2
R25 R76	RES, MF, 1/8W, 1%, 56.2	RN550-5622F	TRW	4701-03-5629	2

REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-REFR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
NONE	BUTTON, CONICAL	F01-01 (BLACK)	SHADW	5103-04-0006	8
U1 U11 U13 U5	IC	MC10102	NOT	8001-01-0200	4
U3 U6 U7 U8 U9	IC	MC10104	NOT	8001-01-0400	5
U2	IC	MC10107	NOT	8001-01-0700	1
U10 U12 U4	IC	MC10116P	NOT	8001-01-1600	3

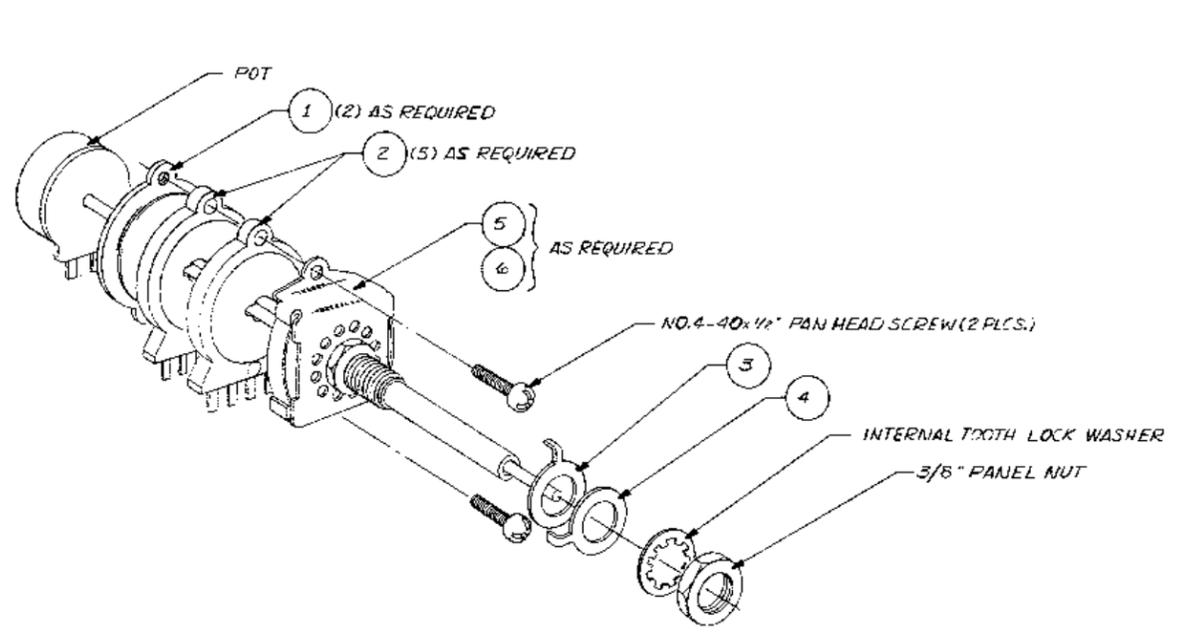
REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-REFR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
C11 C38	CAP, TANT, 22PF, 20V	202A200222M43	RATSD	1500-72-2621	2
NONE	PULSE BOARD	191-0946	WVTK	1700-00-0946	1
P1 P2 P3 P4	CONN, BOTTOM ENTRY, PC	09-52-3102	MOLEX	2100-02-0128	4
NONE	BUBB BAR STANDOFF	2110-001	ARTWR	2100-05-0024	17
R17 R42 R53	RES, MF, 1/8W, 1%, 100	RN550-1000F	TRW	4701-03-1000	3
R30 R61 R78	RES, MF, 1/8W, 1%, 1K	RN550-1001F	TRW	4701-03-1001	3
R24 R75	RES, MF, 1/8W, 1%, 10	RN550-1000F	TRW	4701-03-1009	2
R44	RES, MF, 1/8W, 1%, 10.2K	RN550-1032F	TRW	4701-03-1032	1
R36 R80	RES, MF, 1/8W, 1%, 1.1K	RN550-1101F	TRW	4701-03-1101	2
R45 R46 R9 R92 R96	RES, MF, 1/8W, 1%, 150	RN550-1500F	TRW	4701-03-1500	5
R69	RES, MF, 1/8W, 1%, 1.5K	RN550-1501F	TRW	4701-03-1501	3
R2	RES, MF, 1/8W, 1%, 1.62K	RN550-1621F	TRW	4701-03-1621	1
R26 R74	RES, MF, 1/8W, 1%, 182	RN550-1820F	TRW	4701-03-1820	2
R30 R32 R48 R72	RES, MF, 1/8W, 1%, 200	RN550-2000F	TRW	4701-03-2000	4
R10 R11 R23 R39 R47 R59 R63 R82	RES, MF, 1/8W, 1%, 2K	RN550-2001F	TRW	4701-03-2001	8
R62 R81 R83	RES, MF, 1/8W, 1%, 20.2K	RN550-2032F	TRW	4701-03-2032	3

REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-REFR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
R22 R58	RES, MF, 1/8W, 1%, 576	RN550-5760F	TRW	4701-03-5760	2
R33 R65	RES, MF, 1/8W, 1%, 5.76K	RN550-5761F	TRW	4701-03-5761	2
R16 R21 R52 R55	RES, MF, 1/8W, 1%, 681	RN550-6810F	TRW	4701-03-6810	4
R29 R4 R5 R73	RES, MF, 1/8W, 1%, 6.81K	RN550-6811F	TRW	4701-03-6811	4
R13 R60	RES, MF, 1/8W, 1%, 68.2	RN550-6820F	TRW	4701-03-6820	2
R88 R94	RES, MF, 1/8W, 1%, 49.9	RN600-4999F	TRW	4701-13-4999	2
R12 R40 R48 R50 R6 R84	RES MODULE	4308R-101-681	BOURN	4770-00-0031	6
CR1 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9	DIODE	1M4148	FAIR	4807-02-6666	17
Q24 Q25 Q26 Q27	TRANS	2N2369A	NOT	4901-02-3691	4
Q1 Q11 Q12 Q2	TRANS	2N3563	FAIR	4901-03-5630	4
Q10 Q16 Q19 Q20 Q21 Q23 Q6 Q7 Q8	TRANS	2N3904	FAIR	4901-03-9040	9
Q17 Q18 Q22 Q9	TRANS	2N3906	FAIR	4901-03-9060	4
Q13 Q14 Q15 Q3 Q4 Q5	TRANS	2N5771	NBC	4901-05-7710	6
NA	SWITCH ASSY, PB	5103-00-0042	WVTK	5103-00-0042	1
NA	SWITCH ASSY, PB	5103-00-0043	WVTK	5103-00-0043	1

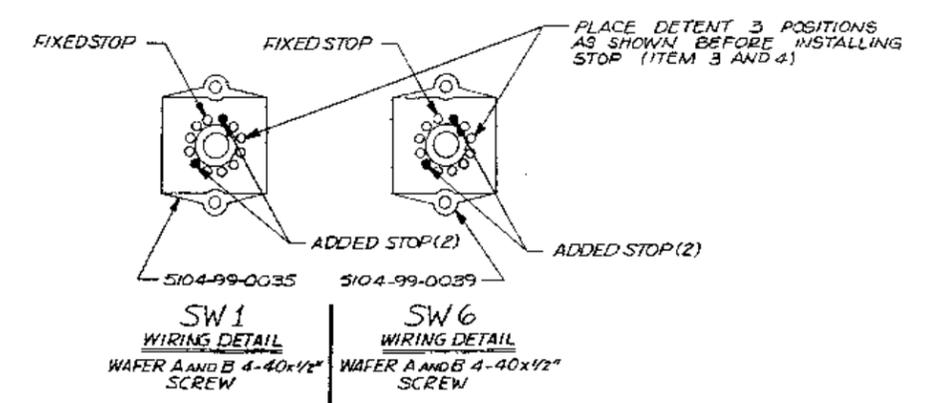
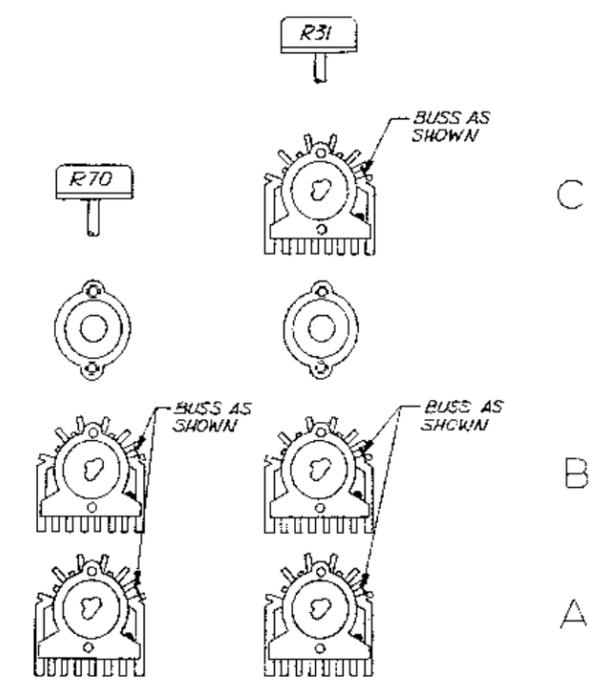
WAVETEK PARTS LIST TITLE: PCA, PULSE ASSEMBLY NO: 1100-00-0946 REV:	WAVETEK PARTS LIST TITLE: PCA, PULSE ASSEMBLY NO: 1100-00-0946 REV:	REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN:	DATE:	WAVETEK SAN DIEGO - CALIF 92161 TITLE: PARTS LIST PCA, PULSE TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: DIM ANGLES: 1 XX: 030 DO NOT SCALE DWG SCALE:	
		MATERIAL:	PROF: EACH	RELEASE APPROV:		MODEL NO: 191
		FINISH: WAVETEK PROCESS				DWG NO: 1100-00-0946
						REV: A
NOTE: UNLESS OTHERWISE SPECIFIED		CODE: 23338	SHEET 1 OF 1			

REV	ECN	BY	DATE	APP

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TYPICAL SWITCH
HARDWARE STACK-UP



2. #24 AWG BUSS WIRE.
1. ALL WAFERS SHOWN IN FULL CCW POSITION.
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: D. COOPER	DATE: 9/25/84	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJECT: R-1000	REV: 1	TITLE: ASSEMBLY DETENT, PULSE BOARD	
FINISH: WAVETEK PROCESS	RELEASE APPROX: 12/83	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX: 0.10 ANGLES: 1:2X: 0.25	MODEL NO: 191	DWG NO: 0102-00-0966
SCALE	DO NOT SCALE DWG	CODE: 23338	SHEET: 1	OF: 1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-REFOR-PART-NO	REFOR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG PULSE SWITCHES	0102-00-0966	WVTK	0102-00-0966	1
NONE	PLATE SW	00B-004	WVTK	1400-00-2130	2
NONE	POT. CONT. 10K FROM 4600-01-0312	4609-71-0307	WVTK	4609-71-0307	1
NONE	POT. CONT. 10K FROM 4600-01-0312	4609-71-0320	WVTK	4609-71-0320	1
NONE	WAFER	147-400	WVTK	5104-02-0015	3
NONE	SWITCH STOP	211-33-001	CTS	5104-07-0001	2
NONE	SWITCH STOP	212-33-006	CTS	5104-07-0002	2
NONE	DETENT MOD FROM 5104-01-0010	5104-99-0035	WVTK	5104-99-0035	1
NONE	DETENT MOD FROM 5104-01-0010	5104-99-0039	WVTK	5104-99-0039	1

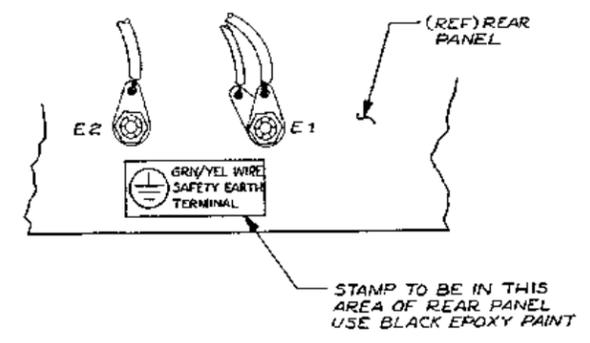
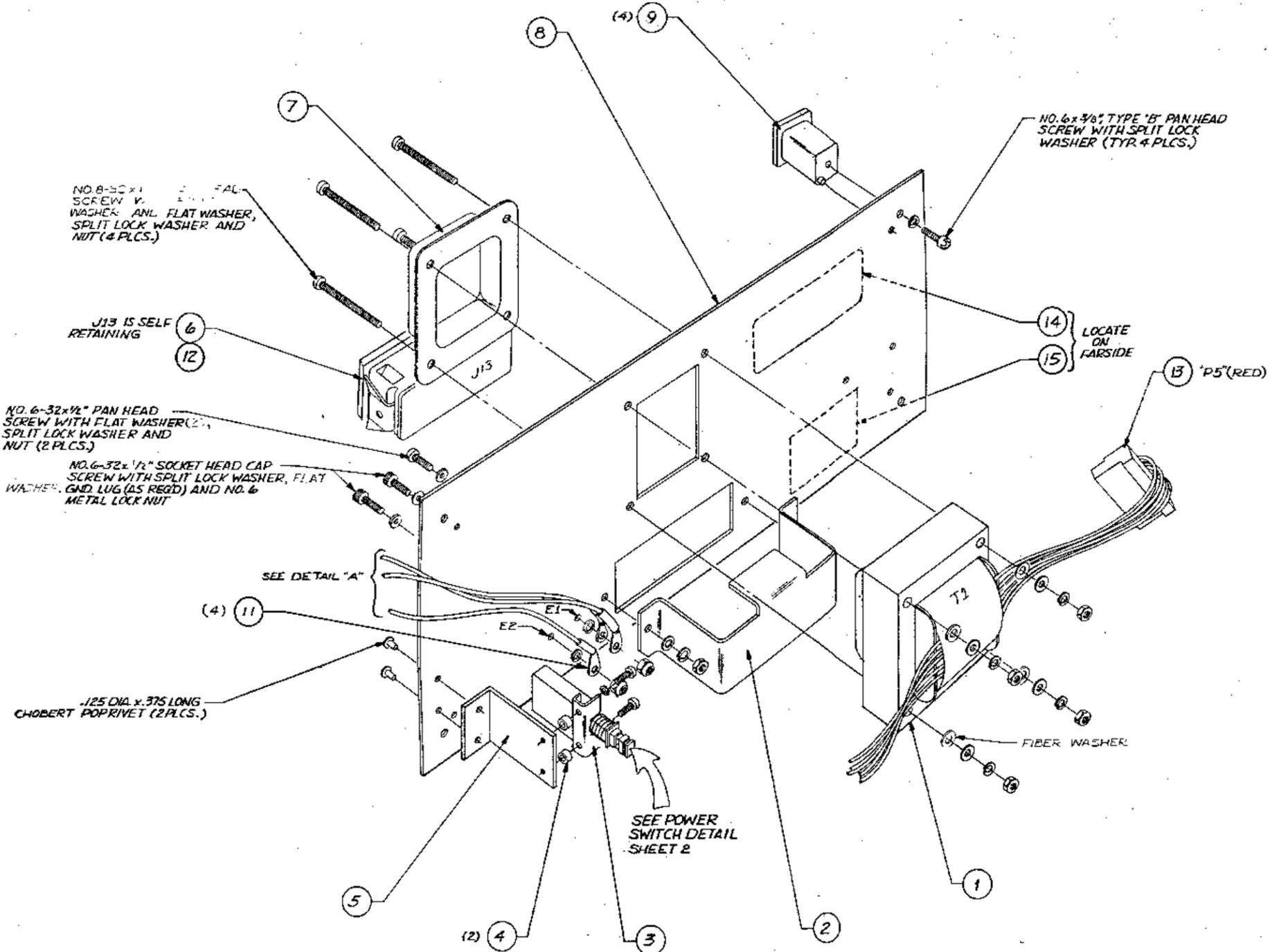
WAVETEK PARTS LIST	TITLE ASSY. SWITCHES PULSE	ASSEMBLY NO 1202-00-0966	REV
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REMOVE ALL BURRS AND BREAK SHARP EDGES	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ. FILE	
FINISH WAVETEK PROCESS	RELEASE APPROV.	TITLE PULSE BOARD SWITCH PARTS LIST
	DO NOT SCALE DWG	SCALE
SCALE	MODEL NO 191	DWG NO 1202-00-0966
	CODE 23338	SHEET 1 OF 1

NOTE: UNLESS OTHERWISE SPECIFIED

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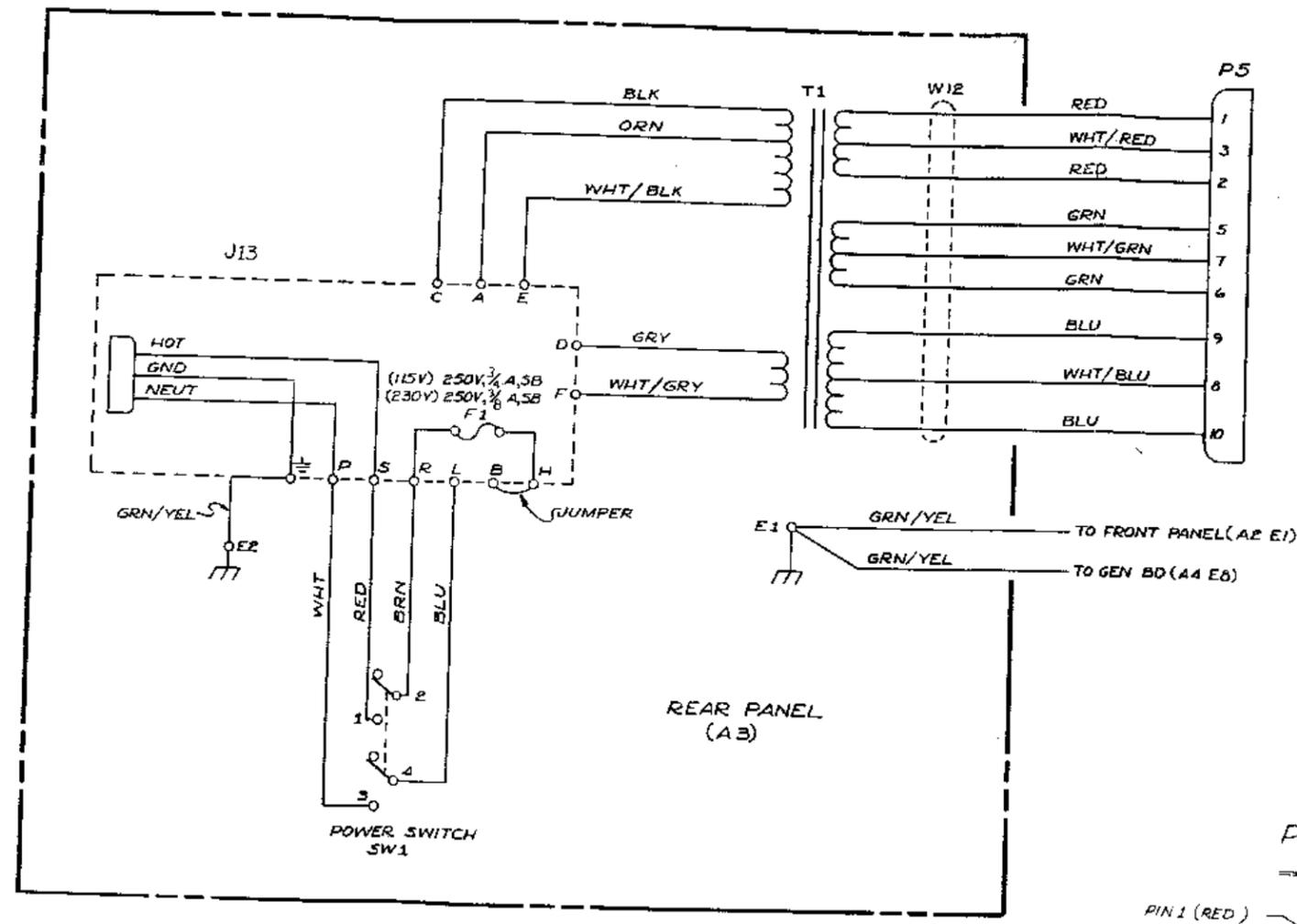
- 2. THIS SHEET IS INTENDED TO SHOW MECHANICAL ASSEMBLY ONLY - REFERENCE SHEET 1 OF 2 FOR WIRING.
- 1. SEE PARTS LIST NO: 1101-00-0952

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES MATERIAL	DESIGNER D. COOPER	DATE 2/4/81	WAVETEK 900 OREGON - CALIFORNIA	
FINISH WAVETEK PROCESS	RELEASE APPROV 1.	TOLERANCE UNLESS OTHERWISE SPECIFIED XX ± .010 ANGLES 1:1 DO NOT SCALE DWG	MOBYL NO 191	FORM NO 0102-00-0952
	SCALE	CDWG POINT 23338	REV D	SHEET 1 OF 2

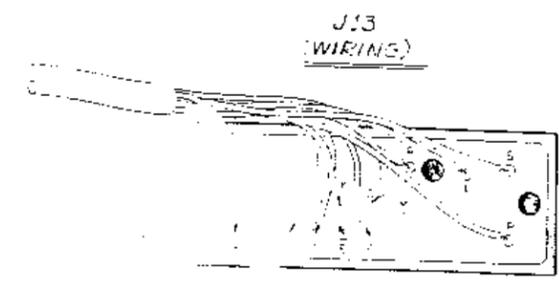
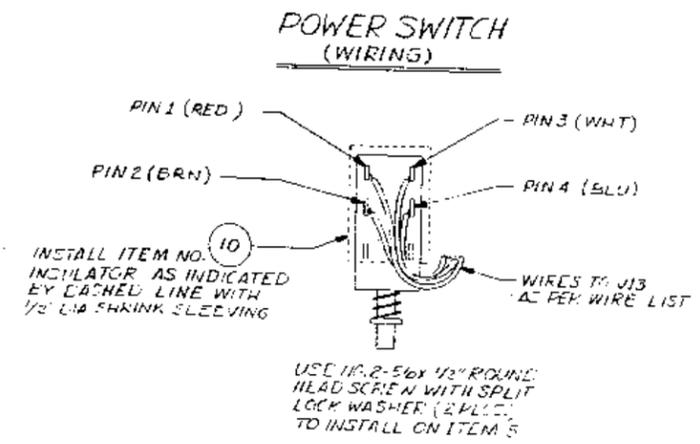
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REV	ECN	BY	DATE	APP



WIRE LIST				
AWG	COLOR	LENGTH	DEST. FROM	TO
22	RED	5"	T1	1
22	RED	5"	T1	3
22	WHT/RED	5"	T1	3-2
22	WHT/RED	5"	T1	3-3
22	GRN	5"	T1	P5-4
22	GRN	5"	T1	P5-5
22	WHT/GRN	5"	T1	P5-6
22	WHT/GRN	5"	T1	P5-7
22	WHT/BLU	5"	T1	P5-8
22	BLU	5"	T1	P5-9
22	BLU	5"	T1	P5-10
24	BLK	4 3/4"	T1	J13-C
24	ORN	4 3/4"	T1	J13-A
24	WHT/BLK	4 3/4"	T1	J13-E
24	GRY	4 3/4"	T1	J13-D
24	WHT/GRY	4 3/4"	T1	J13-F
22	WHT	3 1/4"	J13-P	SW1-3
22	RED	3 1/4"	J13-S	SW1-1
22	BRN	3 1/4"	J13-R	SW1-2
22	BLU	3 1/4"	J13-L	SW1-4
22	BUSS	---	J13-B	J13-H
18	GRN/YEL	6 3/4"	J13-E	A3 E2
18	GRN/YEL	11 1/2"	A3 E1	A2 E1
18	GRN/YEL	3 1/2"	A3 E1	A4 E8

W1 } WIRE
W2 } MARKED (19)



1. THIS SHEET IS INTENDED TO SHOW WIRE HOOK UP ONLY - REFERENCE SHEET 1 OF 2 FOR MECHANICAL ASSEMBLY.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN: CHERYL ACK	DATE: 1/28/82	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PROJENGR	RELEASE APPROV	
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED X.XX ± .010 X.X ± .005		TITLE: ASSEMBLY, REAR PANEL (-3)
SCALE	DO NOT SCALE DWG	HOUSE NO: 19	DWG NO: 0102-00-0952
		CODE IDENT: 23338	REV: LJ

REV	ECN	BY	DATE	APP
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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGOR-PART-NO	MFOR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. REAR PANEL	0102-00-0952	WVTK	0102-00-0952	1
4	SPACER	0480	WVTK	1400-00-0653	2
7	END BELL	137-500-EB	WVTK	1400-00-3224	1
9	POST	180-302	WVTK	1400-00-5020	4
15	LABEL, WARNING	801-6940	WVTK	1400-00-6940	1
10	INSULATOR, PWR SWITCH REF: 1600-99-0001	801-8370	WVTK	1400-00-8370	1
14	I.D. LABEL	801-9090	WVTK	1400-00-9090	1
5	BRACKET, SWITCH MNTG	189-3263	WVTK	1400-01-3263	1
6	REAR PANEL	191-3782	WVTK	1400-01-3782	1
2	SHIELD, VOLTAGE	191-5190	WVTK	1400-01-5190	1
13	HOUSING	1-640433-0	AHP	2100-02-0080	1
6	RECEPTACLE	6UJ1	CORCH	2100-03-0026	1
11	SOLDER LUG	11A144	ZIER	2100-04-0025	3
12	FUSE, 3/4A, 250V, S-B	313-750	LITFU	2400-03-0011	1
3	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1
T1	TRANSFORMER	5600-00-0031	CGIL	5600-00-0031	1

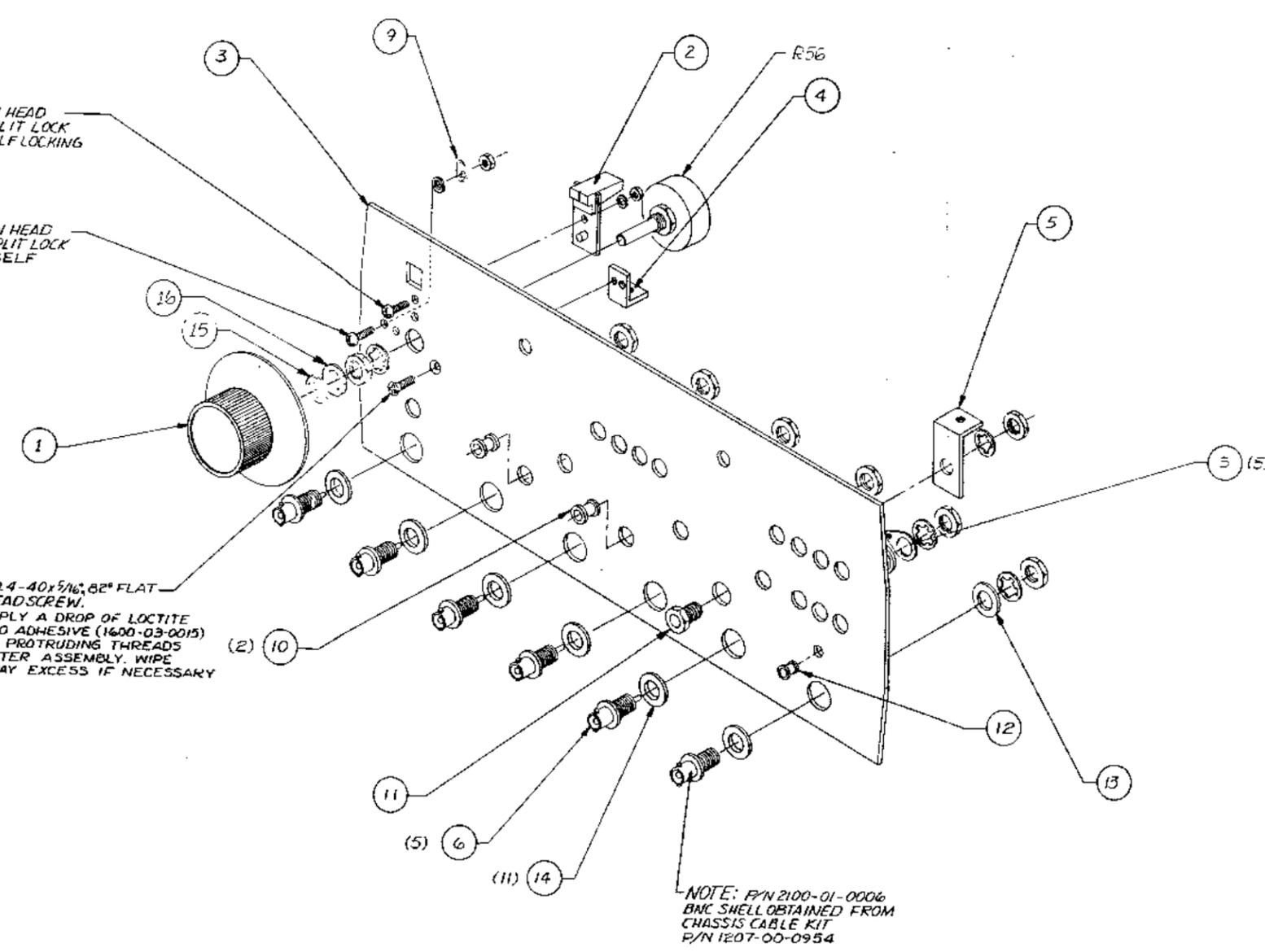
	TITLE ASSY. REAR PANEL	ASSEMBLY NO 1101-00-0952	REV B
	PAGE 1		

IMPROVE ALL BURNS AND BREAK SHARP EDGES MATERIAL FINISH WAVETEK PROCESS SCALE	DRAWN PROFENGR RELEASE APPROV TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.030 ANGLES .1 XX - .010 DO NOT SCALE DWG	DATE SAN DIEGO - CALIFORNIA TITLE PARTS LIST ASSY. REAR PANEL MODEL NO 191 DWG NO 1101-00-0952 CDOR 23338	SHEET 1 OF 1
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NOTE: UNLESS OTHERWISE SPECIFIED

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REV	EDN	BY	DATE	APP
B	4499			
C	4634	ACT	10/16/81	H.N.
D	8043			



NO. 4-40x3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND SELF LOCKING NUT

NO. 6-32x7/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND SELF LOCKING NUT

NO. 4-40x1/4" B2" FLAT HEAD SCREW. APPLY A DROP OF LOCTITE 290 ADHESIVE (1600-03-0015) TO PROTRUDING THREADS AFTER ASSEMBLY. WIPE AWAY EXCESS IF NECESSARY

NOTE: P/N 2100-01-0006 BNC SHELL OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-0954

NOTE BOTTOM EDGE OF FRONT PANEL

NOTE ORIENTATION OF GROUND LUGS, AS SHOWN

INSTALL #20 AWG BUSS WIRE BETWEEN THESE GND LUGS

BNC GROUND LUG ORIENTATION

1. FOR FRONT PANEL PARTS LIST SEE: 1101-00-0981

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRW: D.C.C. 10/16/81	CHK: 2881	WAVETEK SAN DIEGO - CALIFORNIA
MATERIAL	PRO/ENGR: [Signature]	DATE: 10/16/81	
FINISH: WAVETEK PROCESS	PLEASE APPROVE: [Signature]	TOLERANCE UNLESS OTHERWISE SPECIFIED: .010 ANGLES: 1:1 XX: .010	TITLE: ASSEMBLY FRONT PANEL (A2)
	DO NOT SCALE DWG	SCALE	MODEL NO: 191 DRWG NO: 1102-00-0981 CODE: 23338 SHEET / OF /

1102-00-0981

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REV ECN BY DATE APP

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D

D

REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-MFR-PART-NO	MFR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, FRONT PANEL	0102-00-0981	WVTK	0102-00-0981	1
NONE	DIAL ASSY	WVTK	190-187	1201-00-1873	1
2	INDICATOR, DIAL	180-303	WVTK	1400-00-4970	1
3	FRONT PANEL	190-3770	WVTK	1400-01-3770	1
4	ANGLE, PANEL MNTG	190-4523	WVTK	1400-01-4523	1
5	ANGLE, PANEL MNTG	190-4533	WVTK	1400-01-4533	1
6	CONN BNC	KC-7946	KING	2100-01-0002	5
8	SOLDER LUG	1497	SMITH	2100-04-0012	5
9	SOLDER LUG	11A144	ZIER	2100-04-0025	1
10	BUSHING NYLINER	4L2FF	THOMP	2800-01-0002	2
11	BEARING, PANEL	119	SMITH	2800-01-0004	1
12	BUSHING(NYLINER)11/B	2L2FF	THOMP	2800-01-0005	1
14	WASHER, SHOULDER	266B	SMITH	2800-27-0004	11
13	NYLON FLAT WASHER	2264-N-385	AMTOM	2800-28-0003	1
15	WASHER, WAVE SPRING	5804-133-1	SEA	2800-28-0021	1
16	WASHER, FLAT, BRASS, .025 ID, .400 OD	5714-62-32	SESTH	2800-28-0022	1

WAVETEK PARTS LIST	TITLE ASSY, FRONT PANEL	ASSEMBLY NO 1101-00-0981	REV A
	PAGE 1		

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REFERENCE DESIGNATORS	PART DESCRIPTION	DRG-MFR-PART-NO	MFR	WAVETEK NO	QTY/PT
R56	POT, DIAL, 5K +/- 5%, PRECISION, LINEAR	ECONDPT MKIII 78PF-14	NEI	4600-03-0212	1

WAVETEK PARTS LIST	TITLE ASSY, FRONT PANEL	ASSEMBLY NO 1101-00-0981	REV A
	PAGE 2		

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REMOVE ALL BURS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO - CALIFORNIA	
MATERIAL	PROTECTOR		FRONT PANEL PARTS LIST	
	RELEASE APPROV			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - DIM ANGLES - 1 XX - 030		MODEL NO 191	DWG NO 1101-00-0981
	DO NOT SCALE DWG	SCALE	REV 23338	SHEET 1 OF 1

NOTE: UNLESS OTHERWISE SPECIFIED

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