

OPERATOR'S & MAINTENANCE MANUAL

Model 190
20 MHz
Function Generator

WAVETEK®

OPERATOR'S & MAINTENANCE MANUAL

Model 190

20 MHz

Function Generator

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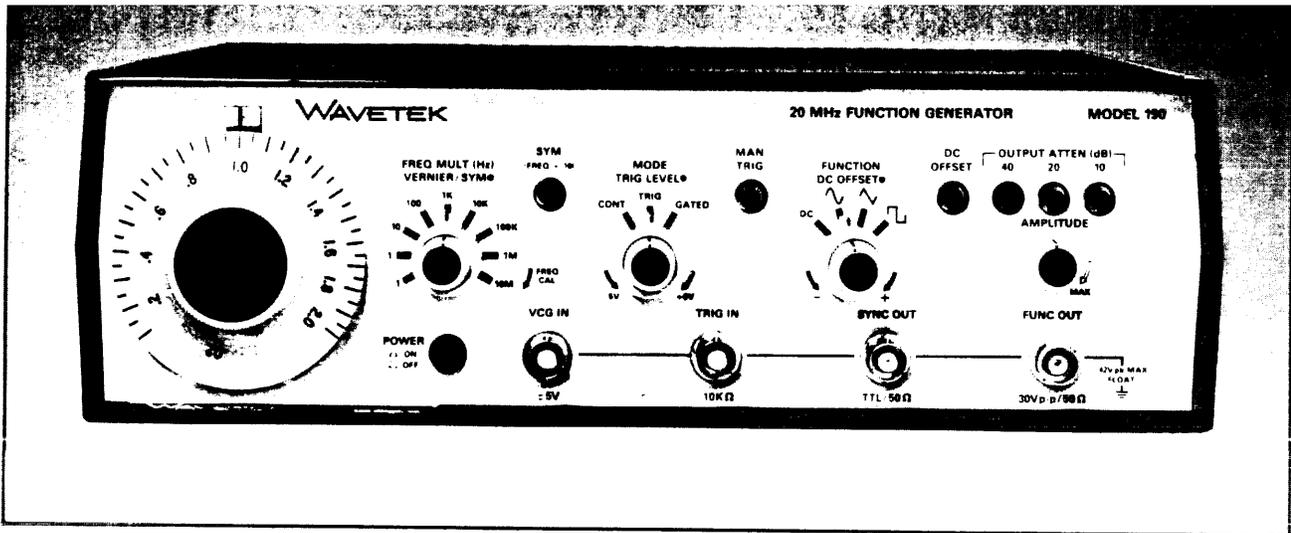
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SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with \oplus or \triangle).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.



1

SECTION

GENERAL DESCRIPTION

1.1 MODEL 190

The Wavetek Model 190, 20 MHz Function Generator, is a precision source of sine, triangle and square waveforms plus dc voltage. All waveforms are front panel variable from .002 Hz to 20 MHz and can be externally modulated. Outputs can be continuous or the generator can be triggered or gated by an external signal or a front panel switch. Amplitude of the waveforms is variable from 30V peak-to-peak (15V peak-to-peak into 50 Ω) down to 1.5mV peak-to-peak. DC reference of the waveform can be offset positively or negatively. Maximum 150mA peak current can be continuously varied over an 80 dB range. A sync output provides a TTL level into 50 Ω .

1.2 SPECIFICATIONS

1.2.1 Versatility

Waveforms

Selectable sine , triangle , square , and dc with TTL sync. Symmetry of waveforms may be varied for sawtooth and variable duty cycle pulses.

Operational Modes

Continuous: Generator oscillates continuously at selected frequency.

Triggered: Generator is quiescent until triggered by external signal or manual trigger, then generates one cycle at selected frequency.

Gated: As triggered mode, except generator oscillates for the duration of gate signal plus time to complete the last cycle.

Frequency Range

0.002 Hz to 20 MHz in 9 overlapping decade ranges with approximately 1% of full scale vernier control.

Function Output

, ,  selectable and variable to 30 Vp-p (15 Vp-p into 50 Ω). All waveforms and dc can supply 150 mA peak current and may be attenuated in 10 dB steps to 70 dB with 10 dB vernier for overall attenuation of 80 dB. 50 Ω source impedance.

DC Output and DC Offset

Selectable thru function output BNC. Controlled by front panel control with separate on-off switch. Adjustable

between ± 15 Vdc (± 7.5 Vdc into 50 Ω) with signal peak plus offset limited to ± 15 Vdc (± 7.5 Vdc into 50 Ω). DC offset and output waveform attenuated proportionately by the 0 to 70 dB output attenuator.

Sync Output

A TTL level pulse when terminated with 50 Ω . Duty cycle varies with symmetry when in square wave function. 50 Ω source impedance.

VCG—Voltage Controlled Generator

Up to 1000:1 frequency change with external 0 to ± 5 V signal. Upper frequency is limited to maximum of selected range.

Slew Rate: 2% of range per μ s.

Linearity: $\pm 0.5\%$ thru $\times 100$ K range.
 $\pm 5\%$ on $\times 1$ M and $\times 10$ M range.

Impedance: 10 k Ω .

Trigger (and Gate) Input

Input Range: 1 Vp-p to ± 10 V.

Trigger Level Adj: -5 V to $+5$ V.

Impedance: 1.5 k Ω shunted by 1.5 pF.

Pulse Width: 25 ns min.

Repetition Rate:

| Input | Max Rep Rate |
|-------------|--------------|
| ± 1 V | 1 MHz |
| ± 2.5 V | 10 MHz |

Symmetry

Symmetry of all waveform outputs is continuously adjustable from 1:19 to 19:1. Varying symmetry provides variable duty-cycle pulses, sawtooth ramps and distorted sine waves.

NOTE

When SYMMETRY control is used, indicated frequency is divided by approximately 10.

1.2.2 Frequency Precision

Dial Accuracy

$\pm 3\%$ of full scale from $\times .1$ Hz to $\times 1$ MHz ranges.
 $\pm 5\%$ of full scale on $\times 10$ M range.

Time Symmetry

Square wave variation from 0.1 to 2 on dial less than:

±1% to 200 kHz.
 ±10% to 20 MHz.

1.2.3 Amplitude Precision

Amplitude Change with Frequency

Sine variation with frequency less than:
 ±0.2 dB on all ranges thru ×100K.
 ±0.5 dB on ×1M range.
 ±1.5 dB on ×10M range.

Step Attenuator Accuracy

±0.3 dB with 10, 20 and 40 dB attenuator setting.
 ±0.6 dB with 30, 50 and 60 dB attenuator setting.
 ±0.9 dB with 70 dB attenuator setting.

1.2.4 Waveform Characteristics

Sine Distortion

<0.5% on X1K, and X10K ranges.
 <1.0% on X.1 to X100 and X100K ranges.

All harmonics 30 dB below fundamental on X1M range,
 and 25 dB below fundamental on X10M range.

Square Wave

Rise/Fall Time: <15 ns (10% to 90%).

Total Aberrations: 5% of full amplitude (each peak).

Triangle Linearity

>99% for 0.002 Hz to 200 kHz.

1.2.5 General

Stability

Amplitude, frequency and dc offset after two hour warm-up.

Short Term: ±0.05% for 10 minutes.

Long Term: ±0.25% for 24 hours.

Environmental

Specification apply at 25°C ±5°C.

Instrument operates from 0°C to +50°C.

Dimensions

28.6 cm (11 ¼ in.) wide; 8.9 cm (3½ in.) high; 28.6 cm (11 ¼ in.) deep.

Weight

4.7 kg (10.4 lb) net; 5.9 kg (13 lb) shipping.

Power

100/120/220/240V (+5%, -10%), 48 Hz to 66 Hz,
 70 VA.

NOTE

All specifications apply from 0.1 to 2.0 on frequency dial, when FUNC OUT is maximum and 50Ω terminated, and with SYM control OFF.

SYMMETRY and VERNIER controls affect frequency calibration. Maximum possible asymmetry is a function of frequency setting.

SECTION 2

INITIAL PREPARATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a 3/4 amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

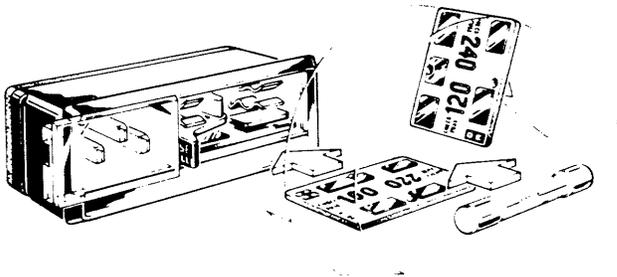


Figure 2-1. Voltage Selector and Fuse

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.

2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.
3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

| Card Position | Input Vac | Fuse |
|---------------|------------|---------|
| 100 | 90 to 105 | 3/4 amp |
| 120 | 108 to 126 | 3/4 amp |
| 220 | 198 to 231 | 3/8 amp |
| 240 | 216 to 252 | 3/8 amp |

2.2.2 Signal Connections

Use RG58U 50Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

2.3 ELECTRICAL ACCEPTANCE CHECKOUT

This checkout procedure verifies the generator operation. If a malfunction is found, refer to the Warranty in the front of this manual. A dual trace, 150 MHz bandwidth oscilloscope with X10 time base magnification, a 50Ω load, a coaxial tee and three 50Ω cables are required to perform this checkout.

Set up as in figure 2-2 and preset the generator front panel controls as follows.

| CONTROL | POSITION |
|------------------------------|-----------------|
| Dial | 1.0 |
| FREQ MULT | 1K |
| VERN/SYM | FREQ CAL (cw) |
| SYM | OFF (Extended) |
| MODE | CONT (FUNC) |
| TRIG LEVEL | 10 o'clock |
| FUNCTION | ~ |
| DC OFFSET (On/Off) | OFF (Extended) |
| DC OFFSET (Variable Control) | ccw |
| OUTPUT ATTEN 40, 20, 10 | All Extended |
| AMPLITUDE | MAX (cw) |
| POWER | ON |

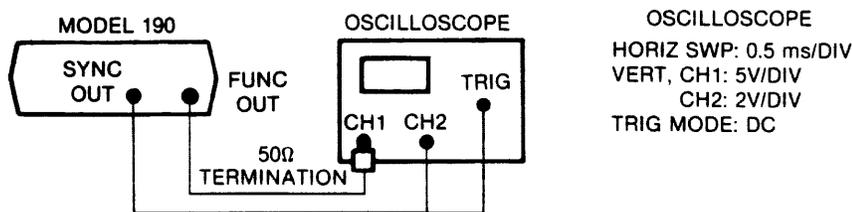


Figure 2-2. Checkout Setup

Table 2-1. Checkout Procedure

| Step | Control | Position/Operation | Observation |
|-------------|----------------------|---|---|
| 1 | Oscilloscope | Trig level and slope, both positive. | CH2: Square wave that begins on positive going edge. CH1: 15 Vp-p square wave. |
| 2 | Dial and VERNIER/SYM | Rotate dial full cw, vernier full ccw. Then the opposite. Return dial to 1.0, vernier to CAL. | CH2: Square wave remains in sync for all dial positions. Range is less than 2 Hz to 2000 Hz (1000:1). |
| 3 | FREQ MULT | Rotate to all positions. Return to 1K position. | Frequency is 1 x each range position. |
| 4 | AMPLITUDE | Set to 6 Vp-p on scope. | CH1: Amplitude decreases to approximately 6 Vp-p. |

Table 2-1. Checkout Procedure (Continued)

| Step | Control | Position/Operation | Observation |
|------|------------------------------|---|--|
| 5 | DC OFFSET | Depress DC OFFSET switch, then rotate DC OFFSET Control CW. (Extended DC OFFSET upon completion.) | Full CCW gives negative offset. Clipping occurs when the offset plus waveform peak amplitude exceeds approximately $\pm 7.5V$ into 50Ω . Initially the negative peak is clipped, but as the DC offset is rotated cw the clipping of the negative peak disappears and eventually the positive peak begins to clip. |
| 6 | AMPLITUDE | Rotate cw. | Waveform returns to 15 Vp-p. |
| 7 | OUTPUT ATTN 10, 20, 40 | Depress buttons in various combinations. Then release all buttons. | Output level varies from 15 Vp-p (0 dB) to 4.7 mV (70 dB). |
| 8 | FUNCTION | Rotate ccw. Select DC \sim , \sim , \square . Reset to \sim . | Observe 0 Vdc level; \sim , \sim and \square are 15 Vp-p. Note phase relationships; \square in phase with \sim and \sim . |
| 9 | SYM, VERNIER/SYM. | Depress SYM switch and rotate VERNIER/SYM control ccw. Extend SYM, return VERNIER/SYM to CAL. | Frequency decreases to approximately 1 kHz. CCW of the 12 o'clock position gives 1:19; CW gives 19:1 (a skewed sinewave and variable duty cycle pulses can be observed for \sim and \square .) |
| 10 | MODE and FUNCTION | Select GATE. Select \sim , \sim , \square . Return to \sim . | A dc level near zero volts (except \square function; quiescent level is at negative peak value). |
| 11 | MANUAL TRIGGER | Press, hold and release. | A burst of \sim for the period the MAN TRIG is depressed. |

SECTION 3

OPERATION

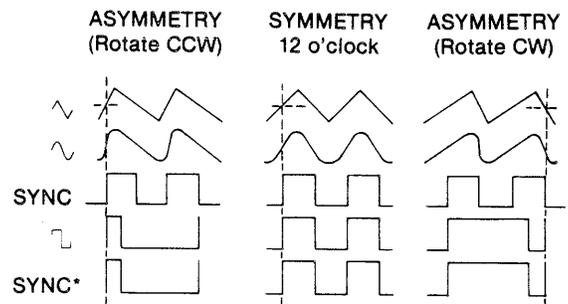
3.1 CONTROLS AND CONNECTORS

The generator front panel controls and connectors are shown in figure 3-1 and keyed to the following descriptions.

- 1 **Frequency Dial** — Settings under the dial index mark summed with **13** and multiplied by **2** determine the output signal frequency.
- 2 **FREQ MULT Control** — Selects one of nine frequency multipliers for dial **1** setting.

VERNIER/SYM Control — When the SYM switch **3** is off (extended) this inner control is a fine adjustment of the frequency dial **1** setting. When the SYM switch is on (depressed) this control varies the symmetry of the waveforms (normally 50% duty cycle). Symmetry range is 19:1 to 1:19 (half cycle to half cycle ratio). When SYM is used, the main generator frequency is divided

by 10. Extending SYM switch ensures 1:1 (50%) symmetry. See figure 3-2.



* SYNC DUTY CYCLE VARIES SAME AS FUNC OUT SIGNAL WHEN SQUARE FUNCTION () IS SELECTED.

Figure 3-2. Effect of Symmetry Control

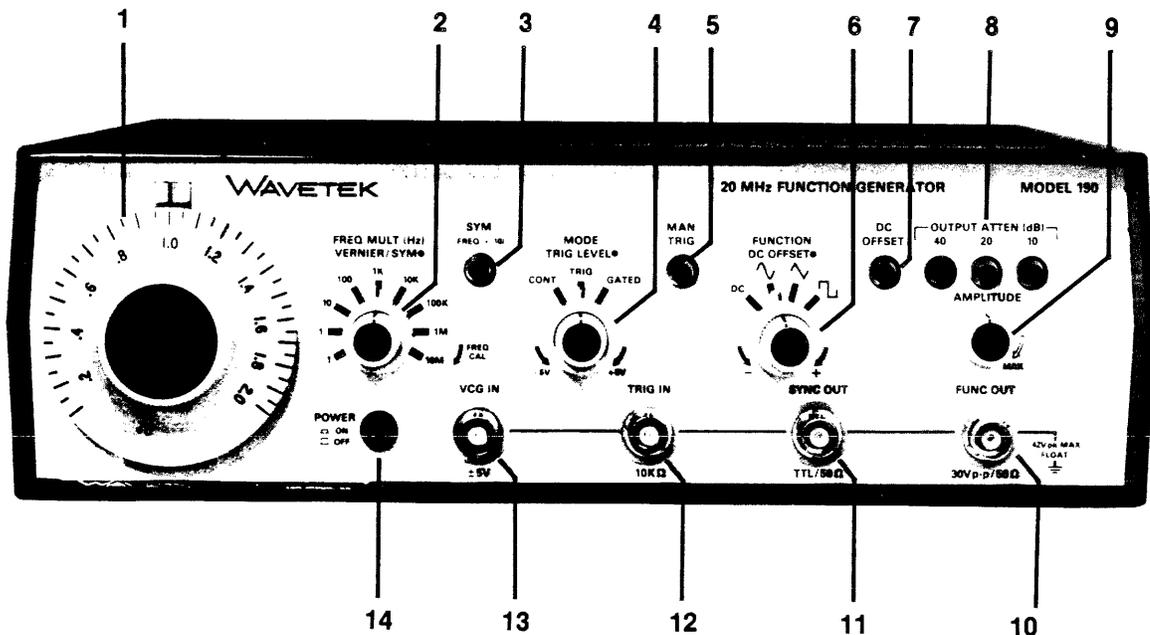


Figure 3-1. Controls and Connectors

3 **SYM Pushbutton** — This switch, when depressed, allows the waveform symmetry to be varied 19:1 to 1:19 range by the VERNIER/SYM control **2**; as a result the generator frequency is divided by 10. When extended, the switch allows the generator to produce normal (50% duty cycle) waveforms.

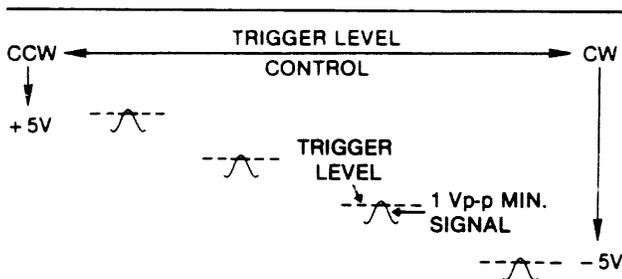
4 **MODE Control** — This switch selects one of the three operating modes:

CONT — Continuous output at FUNC OUT **10** and SYNC OUT **11** connectors.

TRIG — A dc level output until the generator is triggered by the MAN TRIG **5** or with a signal at the TRIG IN connector **12**. When triggered the generator output is one cycle of waveform followed by a dc level.

GATED — As for TRIG except the output is continuous for the duration of the manual or external trigger signal. The last waveform cycle started is always completed.

TRIG LEVEL Control — This inner control is a continuously variable adjustment of the trigger circuitry firing point. When full ccw, a positive going signal at approximately +5V is required for triggering (see figure 3-3). In the full cw position, a positive going signal at approximately -5V or more positive voltage is required for triggering. In the GATED modes, the generator will run continuously when the control is cw from 12 o'clock.



Trigger signal must be a positive going signal exceeding the TRIGGER LEVEL setting.

Figure 3-3. Minimum Trigger Signal

5 **MAN TRIG Pushbutton** — Triggers or gates the output signals when generator mode is TRIG or GATED **4**. In trigger mode, one waveform cycle is output when the button is pushed. In gated mode, waveform cycles are continuously output as long as the button is held in.

6 **FUNCTION Selector** — Outer coaxial knob selects one of three waveforms (sine, triangle, square) or dc.

DC OFFSET Control — Inner coaxial control offsets the main generator output waveform vertically from its normal position and when FUNCTION (outer coaxial switch **6**) is in the DC position, controls polarity and voltage of dc output. DC output range is 0 ± 15 Vdc (± 7.5 Vdc into 50Ω). DC OFFSET switch **7** must be depressed to enable this DC OFFSET Control. Extending the DC OFFSET switch ensures zero volt offset. DC offset and waveform are attenuated by the OUTPUT ATTEN control **8**, but dc offset is not attenuated by the AMPLITUDE control **9**. Waveform peak voltage plus dc offset is limited to ± 15 Vdc (± 7.5 Vdc into 50Ω). See figure 3-4.

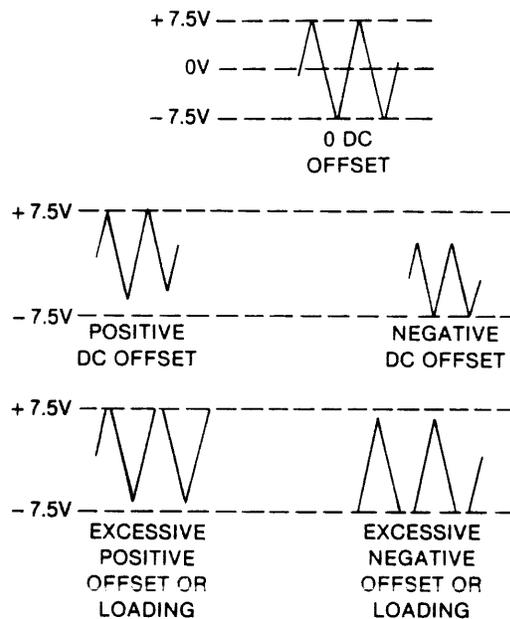


Figure 3-4. DC OFFSET Control

7 **DC OFFSET Pushbutton** — When depressed, the dc offset is switched on and controlled by the DC OFFSET control **6**. When extended, zero offset is assured.

8 **OUTPUT ATTEN Pushbuttons** — These buttons select the attenuation range of the FUNC OUT **10** signal. The AMPLITUDE control **9** allows continuous level variations within each attenuator range. Each of the three buttons may be used individually for 40, 20 or 10 dB steps of attenuation, or pressed in combinations for up to

70 dB of attenuation. The attenuator attenuates both the waveform and dc offset.

- 9 **AMPLITUDE** — This control continuously varies the waveform amplitude within each OUTPUT ATTEN **8** range. CCW rotation reduces waveform amplitudes at FUNC OUT **10** by approximately 10 dB. DC and dc offset voltages are not affected by this control.
- 10 **FUNC OUT Connector** — This BNC is the waveform (or dc) output of the generator. Maximum output is 30 Vp-p (15 Vp-p into 50Ω). Source impedance is 50Ω.
- 11 **SYNC OUT Connector** — The sync signal from this BNC is a TTL level into 50Ω. Duty cycle varies with waveform symmetry. Source impedance is 50Ω.
- 12 **TRIG IN Connector** — This BNC receives the external trigger and gate signals. These signals are applied to the trigger and gate circuit when the MODE switch **4** is in the TRIG or GATED positions. Refer to paragraph 1.2.1, Trigger (and Gate) Input, for trigger signal requirements. The TRIG LEVEL control **4** selectively accepts trigger and gate signals for the trigger and gate circuits.
- 13 **VCG IN Connector** — This BNC accepts ac or dc voltages to proportionately control frequency within the range determined by the FREQ MULT **2**. Positive voltages increase the frequency set by the dial **1**; negative voltages decrease the frequency. The VCG IN will not drive the generator frequency beyond the normal limits of a range. Input impedance is 5 kΩ.
- 14 **POWER Pushbutton** — Depressed is power on, extended is power off.

3.2 OPERATION

Perform the initial checkout in Section 2 for the feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.1.

3.2.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. For example, the proper termination of the 50Ω OUT connector is shown in figure 3-5. Placing the 50 ohm terminator, or 50 ohm resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

The input and output impedances of the generator connectors are listed below.

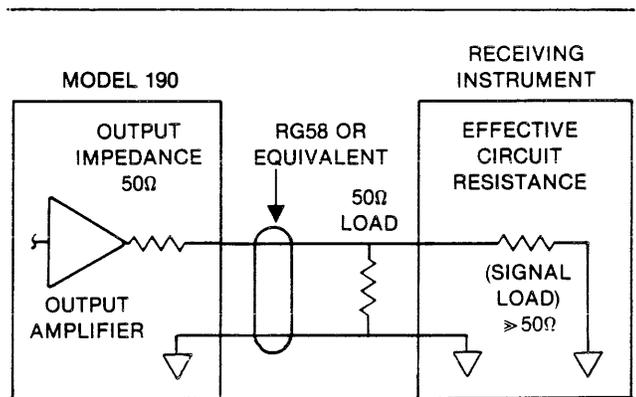


Figure 3-5. Signal Termination

| Connector | Impedance |
|----------------|-----------|
| FUNC OUT | 50Ω |
| SYNC OUT (TTL) | 50Ω |
| TRIG IN | 10k |
| VCG IN | 5kΩ |

3.2.2 Manual Function Generator Operation

The following steps demonstrate manual control of the function generator. (Bold numbers are keys to figure 3-1.)

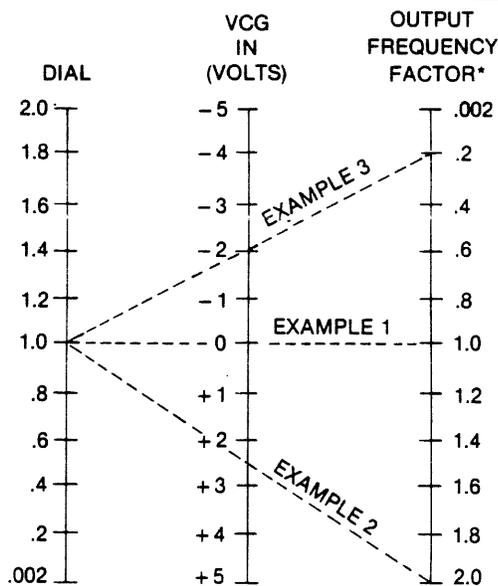
| Step | Control/Connector | Setting |
|------|-------------------|--|
| 1 | FUNC OUT | 10 Connect circuit to output (refer to paragraph 3.2.1). |
| 2 | MODE | 4 Select CONT. |
| 3 | SYM | 3 Extended. |
| 4 | FREQ MULT | 2 Set to desired range of frequency. |
| 5 | Frequency Dial | 1 Set to desired frequency within the range. |
| 6 | FUNCTION | 6 Set to desired waveform. |
| 7 | DC OFFSET | 7 Set as desired. Limit offset to prevent waveform clipping (see figure 3-4). |
| 8 | OUTPUT ATTEN | 8 Select for desired attenuator range. |
| 9 | AMPLITUDE | 9 Select for desired waveform amplitude. |

3.2.3 Voltage Controlled Function Generator Operation

Operation as a voltage controlled function generator (VCG) is as for a manually controlled function generator, only the frequency within particular ranges is additionally controlled by an external voltage ($\pm 5V$ excursions) injected at the VCG IN connector. Perform the steps given in paragraph 3.2.2, only set the frequency dial to determine a reference from which the frequency is to be voltage controlled.

1. For frequency control with positive dc inputs at VCG IN, set the dial for a lower frequency limit.
2. For frequency control with negative dc inputs at VCG IN, set the dial for an upper frequency limit.
3. For modulation with an ac input at VCG IN, set the dial at the desired center frequency. Do not exceed the maximum dial range of the selected frequency range.

Figure 3-6 is a nomograph with examples of dial and voltage effects. Example 1 shows that with 0V VCG input, frequency is determined by the main dial setting, 1.0 in this example. Example 2 shows that with a positive VCG input, output frequency is increased. Example 3 shows that with a negative VCG input, output frequency is decreased. (Note that the Output Frequency Factor column value must be multiplied by a frequency range multiplier to give the actual output frequency.)



*Must be multiplied by FREQ MULT switch setting

Figure 3-6. VCG Voltage-to-Frequency Nomograph

NOTE

Nonlinear operation may result when the VCG input voltage is excessive; that is, when the attempted generator frequency exceeds the range limits. The upper limit is 2 times the multiplier setting, and the lower limit is 1/1000th of the upper limit.

The up to 1000:1 VCG sweep of the generator frequencies available in each range results from a 5V excursion at the VCG IN connector. With the frequency dial set to 2.0, excursions between $-5V$ and $0V$ at VCG IN provide the up to 1000:1 sweep within the set frequency range.

3.2.4 Waveforms

See figure 3-7 for definition of controllable waveform characteristics.

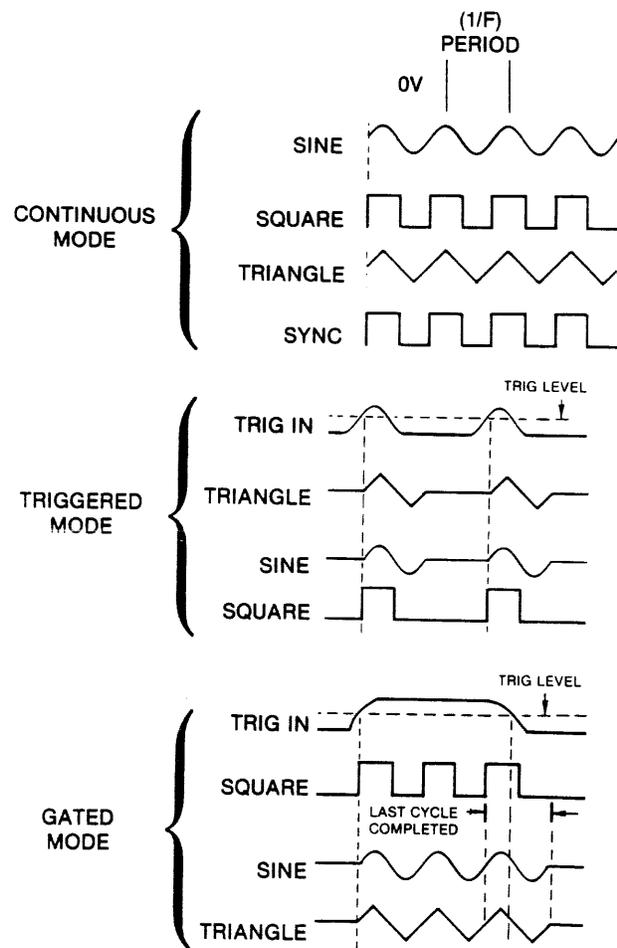


Figure 3-7. Waveform Characteristics

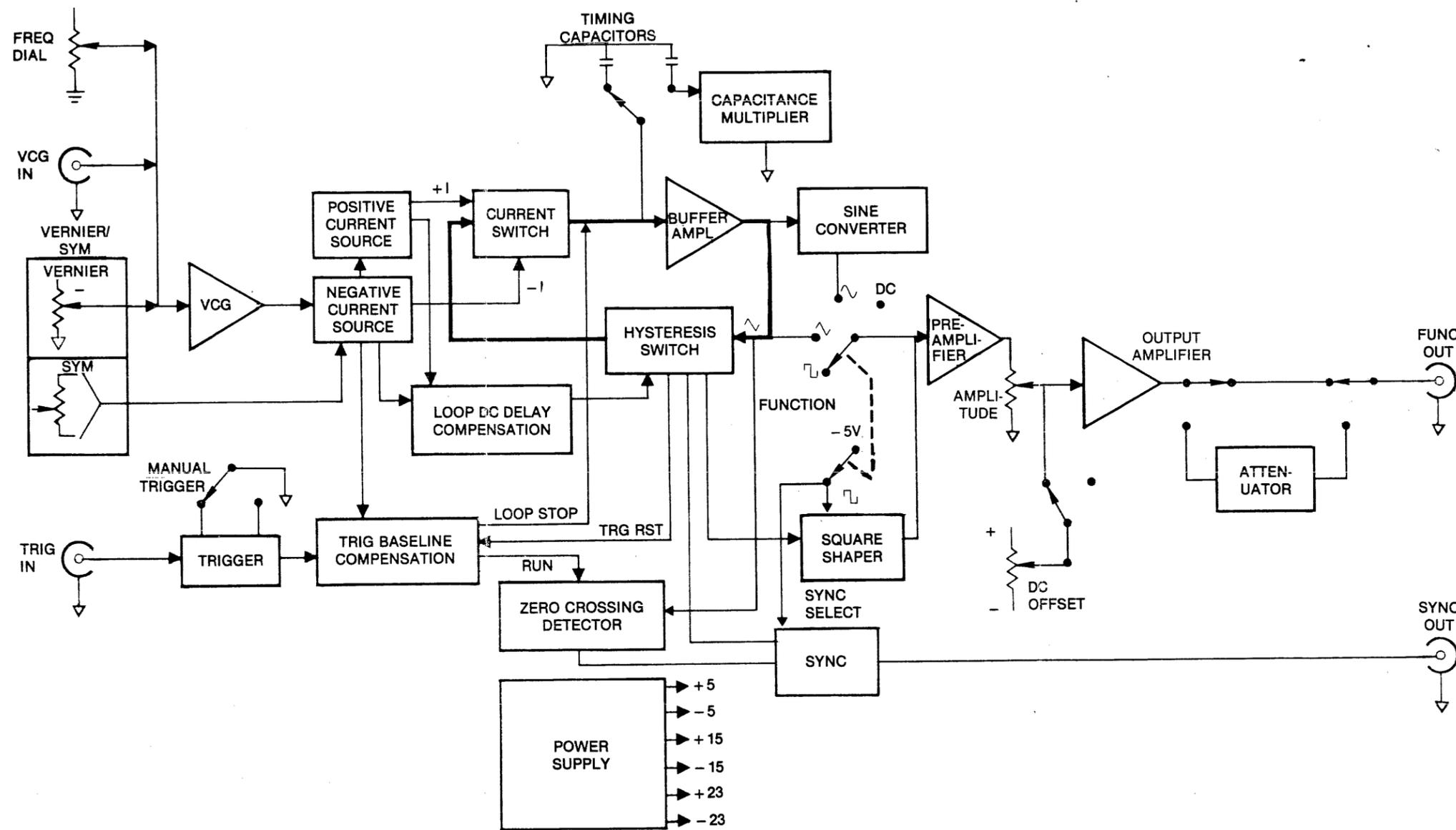


Figure 4-1. Function Block Diagram

4

SECTION

CIRCUIT DESCRIPTION

4.1 INTRODUCTION

This section describes the functions of the major circuits elements and their relationships to one another as shown in figure 4-1, functional block diagram.

4.2 FUNCTIONAL BLOCK DIAGRAM ANALYSIS

As shown in figure 4-1, the VCG (Voltage Controlled Generator) sums the voltage inputs from the frequency dial, VCG IN, and frequency vernier to provide a voltage control signal for the positive and negative current sources. The positive and negative current sources generate precision currents, linearly related to the output of the VCG summing amplifier, which pass through the current switch to the timing capacitors. Additional linear currents are generated for loop dc delay compensation and the trigger baseline compensation.

The current switch, controlled by the hysteresis output, causes either the positive current source or the negative current source to charge the timing capacitor selected by the frequency multiplier. When the positive current source is switched in, the charge on the timing capacitor will rise linearly producing the positive-going triangle slope. Likewise the negative current source produces the negative going triangle slope.

The triangle buffer amplifier is a unity gain amplifier whose output is fed to the hysteresis switch, sine converter and output circuits. The hysteresis switch operates as a "window" comparator with limit points set to the triangle peaks. When the positive going ramp reaches + 1.0V, the hysteresis switch toggles to a low state causing the current switch to connect the negative current source. This causes the timing capacitor voltage to linearly ramp to -1.0V as the timing capacitor voltage reaches -1.0V, the hysteresis switch toggles to a high state, switching in the positive current source. The generator loop continues to oscillate producing simultaneous triangle and square waves, at a frequency determined by the frequency multiplier and the magnitude of the timing current controlled by the sum of the dial setting, the VCG input, and the vernier.

Depressing the SYM button produces an unsymmetrical waveform and a division of the frequency by

a factor of 10. The VERNIER/SYM control creates an imbalance in the current sources and therefore an imbalance in the waveform symmetry up to a ratio of 19:1. The result is variable duty cycle pulse, variable askewed sine wave and variable "sawtooth" triangle waves.

The dc loop delay compensation circuit is used on the two highest frequency ranges to compensate for loop delay. This circuit causes the hysteresis switch trip points to switch earlier in the cycle, and prevents the timing capacitors from charging beyond $\pm 1.0V$. The switch points are adjusted in proportion to the charging current, thus ensuring a constant amplitude as frequency is varied.

The capacitance multiplier is an active circuit which simulates capacitors up to 10,000 times larger than the timing capacitor, thus allowing very long charging times using physically small capacitors. This circuit is used in the four lowest frequency ranges.

The sine converter accepts a ± 1.0 volt triangle signal from the triangle buffer and converts it to a sine wave current. The output is fed via the function switch to the preamplifier.

The trigger circuit allows precise single or multiple (gated) cycles at the output in response to external trigger signals or manual trigger operation. The trigger circuit operates by holding the timing capacitor at 0 volts, via the loop stop signal, on the positive going triangle ramp, until a trigger signal occurs. In the TRIG mode a single cycle is produced for each trigger signal above the variable trigger level threshold. In the GATED mode continuous cycles are generated for the time period at which the external signal is above the trigger level threshold plus the time for completion of the last partial cycle. The RUN signal causes the SYNC output to stay in the low state when the generator is quiescent. The TRGRST signal resets the trigger circuit and generator to the quiescent state on every generator cycle to arm it for the next trigger input. The trigger baseline compensation circuit holds the generator output at zero volts, LOOP STOP, (within specified limits) during the quiescent intervals at any position (value) of the frequency dial, FREQ MULT, VCG IN, or VERNIER.

The sync circuit accepts the square wave signal from the hysteresis or the zero crossing detector switch and converts it to a true 50Ω TTL level output. In square wave function (SYNC SELECT enabled) the sync is in phase with the output, but in triangle or sine functions (SYNC SELECT disabled), the zero crossing detector causes the sync output to be in phase with the zero crossing of the output waveform.

When square is selected by the function switch, the square shaper accepts the signal from the hysteresis switch and converts it to a clean, fast square wave current to drive the preamplifier. The function switch also enables the sync circuit, causing the sync output to be in phase with the positive going edge of the output square wave. In sine, triangle or DC functions, the square shaper input and output are disabled so as not to interfere with the selected waveform.

The preamplifier is fed from both the function switch and the square shaper. The voltage output drives the output amplifier via the amplitude control.

The output amplifier accepts signals from the preamplifier by way of the amplitude control and drives the output attenuator. DC offset is achieved by offsetting the output amplifier.

The output attenuator, fed directly from the output amplifier, provides up to 70 dB of attenuation to the selected waveform or DC offset. This signal is connected directly to the FUNC OUT BNC.

4.3 DETAILED CIRCUIT DESCRIPTION

4.3.1 Current Sources

Refer to the Generator Board Schematic sheet 4. The VCG IN (J7) and FREQ VERNIER (R88) are summed with the dial potentiometer (R56) at the summing node, U14 pin 6 of the VCG amplifier. Full scale on the dial causes a -5 volt control signal at the dial buffer output U14 pin 7. Rotating the dial to minimum, plus turning the FREQ VERNIER ccw produces -5 mV at U14 pin 7. The output of the buffer drives both the GCV buffer and current sources. The GCV output at U14 pin 1 is $+5.0$ volts at full scale.

The current source from U14 pin 7 is present at U13 pin 1. The output of U13 at pin 12 is fed through level shifting transistor Q14 to U8 pin 6. The collector current at pin 7 flows from ground through R81 and R80. As the voltage at U14 pin 7 varies, amplifier U13 and transistor Q14 adjust the base drive of U8 pin 6, and hence the collector current, until the voltage at U13 pin 2 equals the voltage at U13 pin 1. Because U8 is an array of matched transistors with the bases connected together, and all emitter resistors are equal

with VERNIER selected, all collector currents are also equal.

The positive current source is controlled by a current control signal at U8 pin 1, which is held at 0 volts by the servo action of U13 pins 6, 7 and 10, level shifting transistor Q15 and U7 pins 6 and 7. The current "I" in R84 must flow through R93, and because these resistors are both $1\text{k}\Omega$, an equal but opposite base control voltage is present on U7 pin 6 compared to U8 pin 6. Because the transistors in U7 are matched and their bases are at the same point, a positive current "I" flows in R97 and hence the positive current source. A small amount of adjustable balance is provided by R95 and R94 to enable the positive and negative currents to be set for correct symmetry.

On the 1M and 10M ranges, the timing current is increased by approximately 25%, allowing the use of larger timing capacitors and hence, minimizing the effect of any stray capacitance. On the higher ranges, the parallel resistance across R83 (at ISCAL) is greater than the resistance on the lower ranges. This would decrease the current through U8 pin 8 were it not for the servo loop action of U13 pin 12, Q14 and U8 pins 6, 7 and 8. For any VCG setting at U14 pin 7 and U13 pin 1, no matter which range is selected, this servo loop maintains the voltage at U13 pin 2 equal to pin 1. Because the voltage at U13 pin 2 remains constant from range to range, the voltage across, and therefore the current through R80 and R81 also remains constant. This current also flows through U8 pins 7 and 8. To enable this current to remain constant, the servo loop drives the base voltage at U8 pin 6 in a positive direction. Because all of the bases in U8 are at the same point, the current relative to the lower ranges increases in R84 through R87 and also in the collectors of U8 pins 1, 14, 2, and 9.

Variable symmetry is controlled by R88 which doubles as the frequency vernier. With VERNIER selected, R88 functions as a frequency vernier with one end of the control connected to ground and the other connected to the -15 volt supply. The wiper supplies current to the summing node U14 pin 6. Additionally, one end of $1\text{k}\Omega$ resistors R84 through R87 are all connected to the -15 volt supply. For any given dial setting, the current through each of the four resistors is "I". With SYM selected, R88 functions as a variable symmetry vernier with the wiper connected to the -15 volt supply. One end of this vernier supplies current to R84 and R85, while the other end supplies current to R86 and R87. With the vernier centered, each leg is approximately 5000Ω and reduces the current through each of these 4 resistors to $1/10$ I, dividing the generator frequency by 10. As the symmetry control

is varied, resistors for the positive and negative current sources are changed in ratio, hence the current sources are unbalanced and the timing for the positive waveform is varied in respect to the negative waveform, resulting in variable symmetry.

Loop delay dc compensation currents (+ICMP and -ICMP), are supplied by Q16 and U8 pin 9 and track the timing currents.

A current (ITRGL), is supplied by U8 pin 14 to the trig baseline circuit to compensate for variations in freq dial settings when the generator is in a quiescent trigger or gated mode.

4.3.2 Current Switch

Refer to sheet 3. The current switch is driven by the square wave signal (ISWCTRL) from the hysteresis switch. Level shifting transistor Q10 provides a control signal for the diode bridge CR8, CR9, CR30 and CR31. When the control signal is +1.8 volts, CR30 is reversed biased, allowing CR8 to conduct current from the positive current source to the timing capacitor selected by SW9-D. This produces a positive going ramp. CR31 is also turned on, which reverse biases CR9 and prevents current sinking from the timing capacitor to the negative current source. When the control signal is -1.8 volts, both CR30 and CR9 are forward biased, while CR31 and CR8 are reversed biased. At this time, current from the negative current source sinks from the timing capacitor, producing a negative going ramp.

4.3.3 Triangle Buffer Amplifier

Refer again to sheet 3 of the schematic. The signal on the selected timing capacitor is present at both the gate of Q11, and at U9 pin 2. These devices provide a very high input impedance for the signal to avoid leakage which would otherwise cause poor triangle linearity. The output current of Q11 controls the base drive to emitter follower Q13 and hence the output voltage on the emitter. This voltage is sensed at U9 pin 3, causing U9 to adjust the base voltage of Q12 until the differential input of U9 is zero. The low impedance source output voltage at the emitter follower Q13 now follows the high impedance input signal at the gate of Q11 with a circuit gain of 1.0 up to a bandwidth of approximately 1 MHz, above which the gain will drop down to approximately 0.95 typically.

4.3.4 Hysteresis Switch

Refer to sheet 2. U10 pin 5 is the input to the positive peak comparator, while pin 10 is the input to the negative peak comparator. A level shifted triangle signal of

-0.9 volts to -2.8 volts is present at pins 5 and 10 of U10. Assume a positive going ramp. R18 and R19 set the reference voltage on U10 pin 4 at -0.9 volts. When the voltage on pin 5 exceeds the reference voltage on pin 4, the positive comparator changes state and the voltage on pin 3 pulses from an ECL low (-1.8V) to an ECL high (-0.8V). This signal is connected to clear direct (pin 4) of D flip flop U5. The output of U5 pin 2 goes low, while U5 pin 3 goes high. These outputs toggle the differential pair Q7 and Q8 so that Q7 is on and Q8 is off. This causes the current switch control signal (ISWCTRL) to go low, which connects the negative current source to the timing capacitor, and causes the triangle to begin to ramp negative. The negative peak comparator functions in an identical manner to the positive comparator except that the reference voltage at U10 pin 9 is -2.8 volts. At the negative triangle peak, U10 pin 6 pulses high, causing a set direct at U5 pin 5, toggling the current switch signal (ISWCTRL) high and producing a positive going ramp. In addition to being used to store the first peak comparison pulse from U10 pins 3 and 6, U5 also ignores "chatter" from both positive and negative comparators.

4.3.5 Loop DC Delay Compensation

The circuit is also located on sheet 2 of the schematic diagram. The purpose of this circuit is to adjust the reference voltages on the comparators in the two highest frequency ranges so that the triangle peaks do not increase in amplitude due to loop delay. Q2 functions as a variable positive current source controlled by the range switch and the main current source. As the generator frequency is increased, the base voltage of Q2 progressively moves negative causing positive current through R15 and increasing the reference voltage on U5 pin 9 in a positive direction. This causes the negative peak to switch earlier in time, compensating for the loop delay and maintaining constant triangle amplitude and correct frequency tracking.

The positive peak comparator reference is changed in an identical way, except that the voltage on U10 pin 4 becomes more negative with increased frequency. Q4 is a variable negative current source. Q1 and Q3 function as temperature compensating diodes.

4.3.6 Capacitance Multiplier

Refer to schematic diagram sheet 5. The capacitance multiplier is a precision current splitter which shunts up to 99.990% of the VCG current away from the integrating capacitor (C57) to produce the 100 through 0.1 frequency ranges. Timing current is divided between

C57 and R114, then again between R113 and the selected timing resistor (R110 through R112 or R108).

The signal at U11 pins 2, 6, and 7 is a ± 1.0 volt triangle. U11 (pins 6, 7, and 10) is a non-inverting amplifier with a gain of 8. The waveform at U11 pin 1 is a ± 1.0 volt triangle with 0.5 volt spikes at each peak. At any given moment, the junction of R103 and C55 (differentiator circuit input) has 8 times the voltage as the junction of R104 and C55. This voltage difference causes a constant current to charge C55 through R104 and the selected timing resistor. Thus a frequency dependent charging current flows into the summing node of U11 pin 1, producing an inverted square wave component at the differentiator output U11 pin 12 sinking or sourcing current from the main current sources and limiting the amount of current available to charge C57. The ± 1.0 triangle at U11 pin 2 provides the triangle portion of the waveform at U11 pin 12. Since the triangle slopes on U11 pins 1 and 12 are identical, only the square wave component of the waveform at U11 pin 12 is across the timing resistor. The amount of current supplied to charge C55 is therefore this voltage divided by the range resistor value. As the range resistor is increased, the feedback for U11 between pins 1 and 12 is also increased, causing less current to charge C55 and increasing the amount of current being shunted to U11 pin 12 by a factor of 10 for each lower frequency range.

4.3.7 Sine Converter

Refer to sheet 6 of the circuit diagram. The sine converter converts the buffered ± 1.0 volt peak triangle to a sinusoidal current of 2mA peak. The input triangle voltage (TRIBUFC) passes through a voltage divider network to the input of the diode at pins 1, 4 and 6. As this signal progressively increases, the diode between pins 1 and 9 is progressively reversed biased, sinking less current and causing the diode between pins 2 and 5 to pass increasingly more current in a sinusoidal manner to IFUNC. This produces the positive half of the sine wave at the output of the preamplifier. At the same time, the diode between pins 2 and 8 is progressively reversed biased. This slows and eventually prevents current from flowing from the negative portion of the sine converter.

When the input waveform moves negatively, the diode between pins 2 and 5 is reversed biased and the diode between pins 2 and 8 progressively conducts, producing the negative half of the sine wave.

R159 sets the input amplitude for correct biasing of the sine conversion diodes, while R165 adjusts the input signal offset. Thermister R161 adjusts the input voltage to compensate for the diode voltage change

with temperature. The network consisting of R166, R167 and C102 provides a signal (SINCMP) to the non-inverting input of the preamplifier to compensate for the effects of diode capacitance which would otherwise distort the sinewave peaks at high frequencies.

4.3.8 Trigger Circuit

Refer to sheet 5. The trigger input at J8 is added to the voltage from the trigger level control R119 and compared at U12 pin 5 with a reference at U12 pin 4. When the signal at U12 pin 5 exceeds pin 4 by a few millivolts, U12 pin 3 goes high. R120 and C60 ensure a noise free pulse at U12 pin 3 which is one of two wire ORed inputs to U4 pin 7. The second input originates from the MAN TRIG switch circuit. When this switch is depressed, R115 pulls U12 pin 10 low. Pin 10 is compared to the Vbb reference voltage at pin 9, latching pin 6 high and preventing false triggering due to switch contact bounce. Pin 13 connected to pin 6, is referenced to pin 12, causing pin 15 to also go high. When either U12 pin 3 or pin 15 go high, U4 pin 3 goes low because these outputs are wire ORed to U4 pin 7. U4 pin 3 is connected to pins 4 and 10. Because pin 10 was previously high, U4 pin 14 was low causing a low at U4 pin 5. The trigger pulse low at U4 pin 4 causes a 10 ns ECL high pulse at U4 pin 2. At the same time, U4 pin 14 goes high and after the time delay set by R126 and C62, U4 pin 5 also goes high. This causes U4 pin 2 to return low.

In the gate mode CR14 holds U4 pin 11 high, forcing pin 14 low. The length of the control pulse at U4 pin 2 is now equal to the period during which U4 pin 7 is held high. In the continuous mode, U4 pin 2 is held high by CR16 regardless of any input trigger signals.

4.3.9 Trigger Baseline

Refer to sheet 5. In the trigger mode, with no trigger inputs, U5 pin 12 is held low. On the next positive going triangle, the trigger reset (TRIG RST) signal at U5 pin 11 causes U5 pin 14 to go high. This turns Q18 off and Q17 on, which turns off Q19. The Q19 emitter voltage is pulled down by the negative current sources Q20 and Q21, causing CR19 to conduct. Because the anode is at ground and CR18 is matched to CR19, the voltage at the anode of CR18 is also zero. This causes the triangle on the positive going ramp to stop at exactly zero volts. When a trigger signal occurs, U5 pin 12 goes high for about 10ns, causing pin 15 to also go high. This turns on Q18 and turns off Q17, which turns on Q19, causing the emitter to rise to about 1.7 volts. This reverse biases CR18 and CR19 causing the generator to run for exactly one cycle. In the gate mode, U5 pin 12 is held high for the duration of the in-

put signal causing the generator to run for this interval plus the time required to complete a partial cycle.

In the trigger or gated mode, quiescent state, positive charging current I flows in CR18. As the VCG current is varied, I also varies, causing the voltage across CR18 to vary. To prevent this from causing a baseline shift, current (I) must also flow in the reference diode CR19. A negative current source (ITRGL) is connected to the bases of Q20 and Q21. Negative current ($-I$) flows through the collector of Q20 and R133. Because of the configuration of Q20 and Q21, and because R133 and R134 are both $1k\Omega$, an equal amount of current $-2I$ also flows through the collector of Q21 and R134, causing $-2I$ to flow at the junction of R133 and R134. Half of this current ($-I$) flows through CR19, while the remaining current flows through CR18. Therefore, the anode of CR18 is held at zero volts regardless of the VCG summing node current.

The RUN signal is used to hold the sync output low during quiescent periods.

4.3.10 Sync

Refer to sheet 2. The SYNC OUT amplifier is driven from the signal at U6 pin 10 in the triangle and sine functions, and from U6 pin 7 when the function switch is in the square function. These two inputs are wire ORed at U6 pin 13.

In the triangle and sine functions, SYNC SEL allows R23 to pull CR4 high causing a low at U6 pin 2. This enables the signal from the zero crossing detector output (U10 pin 15), and disables the hysteresis switch input at U6 pin 7. When the positive going ramp crosses 0 volts at the zero crossing detector input U10 pin 13, U10 pin 15 and U6 pin 10 go high. This causes a low at U6 pins 14 and 13. U6 pin 9 goes low and pin 15 goes high turning on Q5 and turning off Q6. This results in a high at SYNC OUT. As the triangle at U10 pin 13 crosses 0 volts in a negative direction, pin 15 goes low, causing Q5 to be turned on, producing a low at SYNC OUT. Therefore the SYNC OUT always toggles when the triangle crosses 0 volts.

When the square wave function is selected, CR4 pulls U6 pins 4 and 6 low. U6 pins 2 and 11 now go high, disabling the zero crossing detector input from pin 10, and enabling the square wave input from U6 pin 7. U5 pin 3 now drives the SYNC OUT connector in a similar manner as U10 pin 15. The SYNC OUT is in phase with the square wave output.

R26, a 49.9Ω resistor sets the 50Ω output impedance.

4.3.11 Square Shaper

The square shaper schematic is located on sheet 6. In square function, CR20 pulls U4 pin 13 low, enabling the hysteresis switch input (HYS) at U4 pin 12. A low at U4 pin 12 causes a low at U4 pin 15 and a high at pin 9. Q22 turns on while Q23 is turned off, producing a $+1.2$ volt high at the bases of the current switch control transistors Q24 and Q25. Transistor Q25 is on, reverse biasing CR23. Transistor Q24 is off allowing positive current to flow through R147, CR22, R154 and into the preamplifier node via R152.

When HYS toggles high, Q23 turns on forcing the bases of Q24 and Q25 to -1.2 volts. Q24 turns on and Q25 turns off, allowing negative current to flow through R157, CR23, R154 and the the amplifier node via R152.

R152 and R154 form a current divider to obtain a 2mA full scale current into the preamplifier. Overshoot caused by diode capacitance is reduced by R153 and C73. The output of the square shaper is disabled in all other functions by turning on Q26 and CR24 which reverse bias CR22 and CR23 and prevents current from flowing through R152.

4.3.12 Preamplifier

Refer to sheet 7 of the schematic circuitry. For all functions, full scale output voltage is produced when 2mA is injected into the input summing node U1 pin 8. Transistor array U1 forms a cascaded differential stage. Transistor Q27 is a fixed current source. Q28 and Q29 form a high gain voltage follower. DC negative feedback is applied through R195 to U1 pin 8. The closed loop voltage gain of the amplifier is determined by the ratio of R195 to the input resistors, R152 for square wave and R176 for triangle. The sine converter output supplies the correct current directly from U3 pin 2 to U1 pin 8. The servo action of the preamplifier holds this point at 0 volts, therefore no voltage can be measured. U1 pin 4 is the non-inverting input and is used both to adjust the offset to 0 volts at TP2 using R185 and to inject the sine converter compensation signal (SINCMP) described under paragraph 4.3.7, Sine Converter. High frequency compensation is provided by R182, C81, C86 and C153. Zener diode CR29 provides increased collector voltages for U1 pins 11 and 12 and also allows these two points to be relatively close in voltage.

4.3.13 Output Amplifier

The output amplifier consists of an ac coupled amplifier for signals above about 16 kHz, and a dc coupled

amplifier for signals below about 16 kHz, and to maintain zero dc output offset within specified limits. Refer to the simplified output amplifier schematic, figure 4-2.

Assume zero input voltage at the junction of R203 and R218. The output at R222 and R224 is maintained at 0 volts by dc amplifier U2. U2 pin 3 is connected to a 0 volt reference. If the output drifts away from 0 volts, this will be sensed at U2 pin 2 through R256, R257 and R254. Amplifier U2 will sense a difference between its inputs and produce an output voltage which adjusts the bias in the ac coupled amplifier to return the output to 0 volts. Because R218 and R223 form half of a balanced bridge, and R253, R256 and R257 form the second half, the amplifier node at the junction of R218 and R223 will be held at 0 volts as U2 has returned the junction of R253 and R256 to 0 volts.

A dc input of +1 volt at R218 and R253 is sensed as a positive increase at U2 pin 2, causing U2 pin 6 to go negative. The ac amplifier output goes negative in response to the dc control input. This continues until the output becomes sufficiently negative to sink all the input current, and return U2 pin 2 to 0 volts. The bridge circuit causes the ac amplifier node to be 0 volts. If the input is +1 volt and the node at the junction of R218 and R223 is 0 volts then the input current is $1/12 I = 8.26 \text{ mA}$. All of this current must flow in R223. Because the node is at 0 volts, the output voltage must be $-8.26 \text{ mA} \times 2\text{k}\Omega = -16.52\text{V}$. Therefore the amplifier voltage gain = $R223/R218 = 16.52$.

Above about 16 kHz, the ac amplifier controls the summing node directly, sinking or sourcing current through R223 by adjusting the output voltage to hold the node at 0 volts. The ac amplifier gain is also $R223/R218 = 16.52$. This is divided by 2 at the output terminal, due to the 50Ω source impedance resistors R222 and R224, providing the output is also terminated into 50Ω .

Refer to sheet 7. The top half of the circuit amplifies the positive portion of the signal, and the bottom half amplifies the negative part. Q30 and Q31 form an ac gain stage. An emitter follower stage is formed by Q32 and Q33, to provide a low impedance drive to the second voltage gain stage Q36 and Q39. This stage drives the parallel output emitter followers Q37 and Q38 on the positive side, and Q40 and Q41 on the negative. Diodes CR23 and CR26 set thermally stable bias for the output transistors. Networks R211, R212, C94 and C93 bypass emitter resistor R208, while R245, R246, C107 and C106 bypass R244. As frequency is increased, these components decrease the local negative feedback in the driver stage, increasing the high frequency gain. Voltage regulators VR5 and VR6 have external current limiting circuitry set to limit at about 220 mA to prevent damage in the event of a shorted transistor. When the offset button is depressed, offset current is injected directly into both nodes in proportion to the feedback resistor values. The amplifier responds exactly as described above for a dc input.

4.3.14 Output Attenuator

Refer to sheet 7. Each attenuator button selects an independent voltage divider, which has 50Ω input and output impedances to correctly load the amplifier and to provide a constant 50Ω impedance at the FUNC OUT terminal.

The 10dB attenuator has a 3.16/1 voltage division ratio. The 20dB attenuator has a 10/1 voltage division ratio, and the 40dB stage has a 100/1 ratio. These ratios multiply in voltage. For example if the 20dB and 40dB buttons are depressed, the voltage division ratio is 1000/1. The attenuators add algebraically in dB, therefore any attenuation from 10 to 70dB may be selected in 10dB steps.

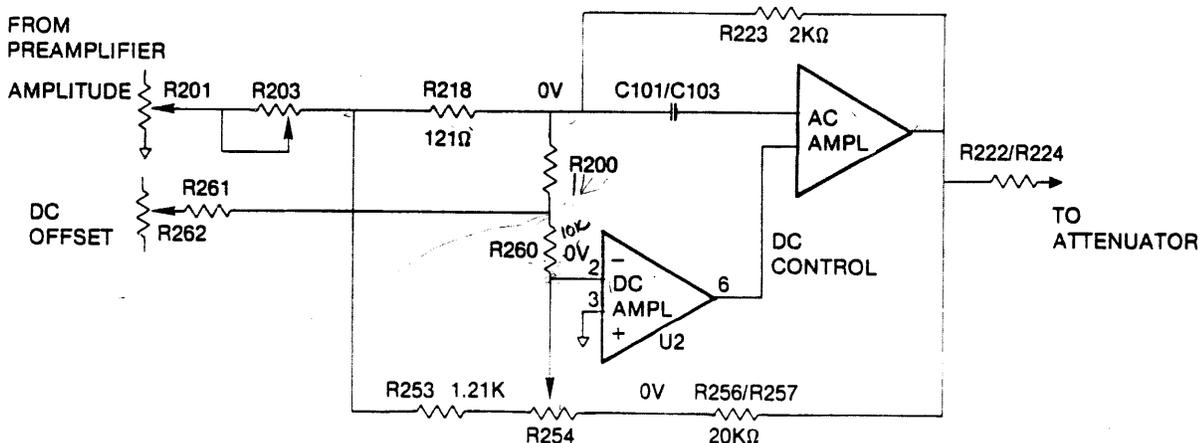


Figure 4-2. Simplified Output Amplifier

5.1 FACTORY REPAIR

Wavetek maintains a factory department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

| | |
|----------------------------|---|
| Voltmeter | Millivolt dc measurement (0.1% accuracy), true rms |
| Oscilloscope, Dual Channel | 100 MHz bandwidth |
| Counter | 20 MHz (0.01% accuracy) |
| 50 Ω | $\pm 0.1\%$ accuracy, 2W |
| Distortion Analyzer | To 200 kHz |
| RG58U Coax Cable | 3 ft length BNC male contacts |
| Spectrum Analyzer | To 20 MHz |

5.3 COVER REMOVAL

NOTE

Before removing the covers, disconnect the instrument from the ac power source.

Invert the instrument and remove the four screws in the bottom cover. Remove the bottom cover.

NOTE

Remove the cover only when it is necessary to make adjustments or measurements.

5.4 CALIBRATION

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1. If performing partial calibration, check previous settings and

adjustments for applicability. Calibration points are shown in figure 5-1.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

1. All measurements made at the FUNCTION OUT connector must be terminated into a 50 Ω ($\pm 0.1\%$) load.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

2. Start the calibration by removing covers as described in paragraph 5.3, connecting the unit to an ac source and setting these front panel switches as follows:

| | |
|--------------|---------------------|
| SYM | Off (extended) |
| TRIG LEVEL | 12 o'clock |
| DC OFFSET | Off (extended) |
| OUTPUT ATTEN | 0 dB (all extended) |

3. Allow the unit to warm up at least 30 minutes for final calibration. Keep the instrument covers on to maintain heat. Remove covers only to make adjustments or measurements.

Table 5-1. Generator Board Calibration Procedure

Note: Where there are no entries, open column indicates previous entry is applicable.

| Step | Test | Freq/Start Freq | Freq Mult | Vern/Sym | Mode | Func | Ampl | Test Point | Tester | Adjust | 50Ω Load | Result | Remarks |
|--------|---------------------------|-----------------|-----------|----------|------|------|------|-------------|---------------|-----------------|----------|-----------------------------|---|
| 1 (1) | ± 15V Balance | 2.0 | 1K | cw | CONT | Sqr | cw | Board + 15V | DVM | R3 | No | + 15 ± 75 Vdc | Ref gnd is TP7 |
| 1 (2) | — | — | — | — | — | — | — | Board - 15V | — | Verify | — | - 15 ± 75Vdc See remarks | - 15V = - + 15V (reading) ± 10 mV , if not retouch R3 |
| 2 | + 5V Supply | — | — | — | — | — | — | + 5V | — | — | — | + 5 ± 25 Vdc | |
| 3 | - 5V Supply | — | — | — | — | — | — | - 5V | — | — | — | + 5 ± 25 Vdc | |
| 4 | + 23V Supply | — | — | — | — | — | — | FB1 | — | — | — | + 21.9 ± 1.10 Vdc | |
| 5 | - 23V Supply | — | — | — | — | — | — | FB2 | — | — | — | - 21.9 ± 1.10 Vdc | |
| 6 | Power Ampl Zero | — | — | — | — | DC | ccw | FUNC OUT | — | R258 | Yes | 0 ± 20 mVdc | |
| 7 | Preamp Zero | — | — | — | — | — | cw | — | — | R185 | — | — | |
| 8 | Top of Dial Symmetry | — | — | — | — | Sqr | — | — | Scope | R96 | — | Asym < 1μs | Set for min asym (Set by alternate triggering of scope ± slope) |
| 9 | VCG Null | 02 | 100K | — | — | — | — | — | — | R6 ^F | — | See remarks | Set for min freq shift when VCG IN is grounded. Repeat steps 8 and 9 as necessary |
| 10 | 100 1 Symmetry | — | — | — | — | — | — | — | — | R94 | — | Asym < 1μs | Set for min asym |
| 11 | 1000 1 Frequency | — | — | ccw | — | — | — | — | Counter | R63 | — | 160 (+ 0. - 20) Hz | |
| 12 | Triangle Offset | 2.0 | 1K | cw | — | Tri | — | — | DVM | R17 | — | 0 ± 20 mVdc | |
| 13 | Sine Distortion | — | — | — | — | Sine | — | — | Dist Analyzer | R159 R165 | — | < 18% | |
| 14 | Triangle Trigger Baseline | — | — | — | TRIG | Tri | — | — | DVM | R51 | — | 0 ± 20 mV | |
| 15 (1) | Dial Alignment | — | — | — | CONT | Sqr | — | SYNC OUT | Counter | R81 | — | 2 kHz ± 10 Hz | |
| 15 (2) | — | 0.2 | — | — | — | — | — | — | — | Verify | — | 200 ± 10 Hz | If satisfactory skip to step 16 (1) |
| 15 (3) | — | See remarks | — | — | — | — | — | — | — | R81 | — | 2.088 kHz ± 10 Hz | Remove dial and set the shaft ccw |
| 15 (4) | — | — | — | — | — | — | — | — | — | See remarks | — | 200 ± 10 Hz | Replace dial, align to 0.2, tighten set screw and verify setting |
| 16 (1) | X10M Frequency | 2.0 | 10M | — | — | — | — | — | — | C37 | — | 20 MHz ± 600 kHz | Optimize C66 value if setting is out of range for C37 |
| 16 (2) | — | See remarks | — | — | — | — | — | — | — | Verify | — | Dial mark ± 600 kHz | Verify frequency at each major dial mark |
| 17 (1) | X1M Frequency | 2.0 | 1M | — | — | — | — | — | — | — | — | See remarks | Trim C33 to set 2 MHz freq at 2 MHz ± 40 kHz |
| 18 | X100K Frequency | — | 100K | — | — | — | — | — | — | — | — | 200 ± 4.0 kHz | Optimize R39 value if necessary |

Table 5-1. Generator Board Calibration Procedure (Continued)

Note: Where there are no entries, open column indicates previous entry is applicable.

| Step | Test | Freq/ Start Freq | Freq Mult | Vern/ Sym | Mode | Func | Ampl | Test Point | Tester | Adjust | 50Ω Load | Result | Remarks |
|--------|-------------------------------|------------------------|--------------|--------------|------|------|------|---------------|---------|--------------|-------------|------------------|---|
| 19 | Capacity Mult Symmetry | 0.1 | 100 | cw | CONT | Sqr | cw | FUNC OUT | Scope | R106 | -- | < 200µs | Set for min asym (Very important for low freq sine dist.) |
| 20 (1) | Capacity Mult Frequency | 2.0 | | -- | -- | -- | -- | SYNC OUT | Counter | R102 | -- | 199.5 ± 5 Hz | |
| 21 | Low Frequency Aberrations | | 1K | -- | -- | -- | -- | FUNC OUT | Scope | R254 | -- | See remarks | Adjust the "Corner Shape" for just noticeable peaking |
| 22 (1) | Function Output Amplitude | | | -- | -- | Sine | -- | -- | DVM | R203 | -- | 5.35 Vrms ± 0.1V | |
| 23 | High Frequency Aberrations | 5 | 10M | -- | -- | Sqr | -- | -- | Scope | R245 R211 | -- | < 0.6 Vp-p | Worst case aberrations not to exceed 4% of full ampli for each peak |

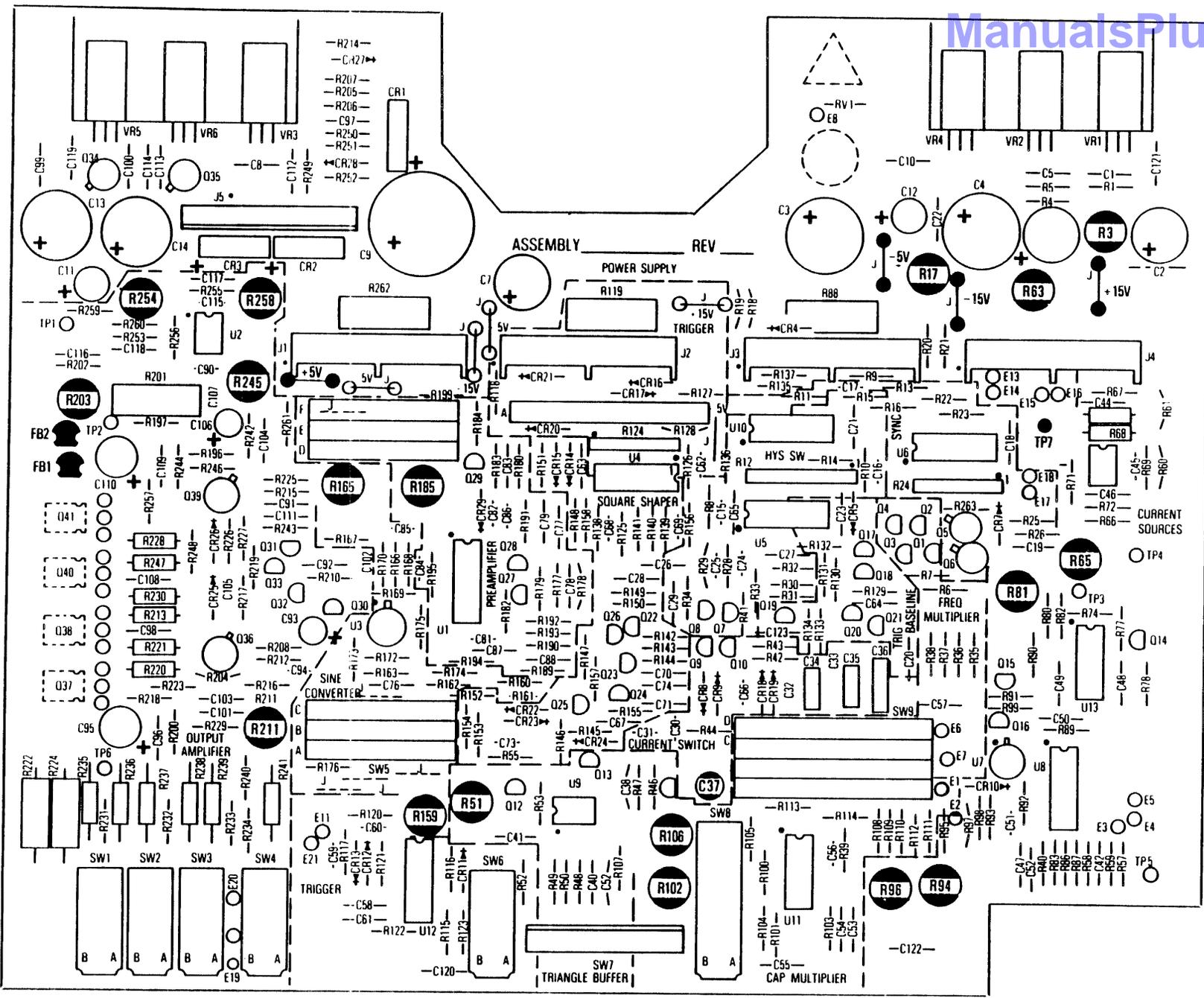


Figure 5-1. Calibration Points

6

SECTION 6

TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description in conjunction with the schematic. Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

6.3 TROUBLESHOOTING

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

Table 6-1 gives an index of common symptoms. For each symptom a troubleshooting guide is referenced (Paragraphs 6.3.1 through 6.3.15) that, when correctly followed, will lead to a solution to the problem.

The troubleshooting guide is arranged in three (3) levels:

1. Identify improperly set controls.
2. Isolate the faulty functional blocks.
3. Identify the faulty circuit or component.

Individual component troubleshooting is given in paragraph 6.5, recommended test equipment is given in paragraph 5.2 and circuit schematics are in the back of this manual.

In all problems:

1. Double check for proper control settings.
2. Calibrate or rule out calibration as a problem.
3. Inspect components, wiring and circuit boards for heat damage.
4. Recalibrate as necessary after circuit repair.

Find the instrument symptom in table 6-1 and proceed as directed to the proper troubleshooting paragraph.

Table 6-1. Symptoms

| Symptom | Paragraph |
|---|-----------|
| Fuse blows, no dial lamp. | 6.3.1 |
| Power supply > 100 mVp-p ripple or out of specification. | 6.3.2 |
| Function out (all functions) distorted or missing. | 6.3.3 |
| Square output distorted or missing. | 6.3.4 |
| Sine wave output distorted or missing. | 6.3.5 |
| Triangle output distorted or missing. | 6.3.6 |
| Sync output distorted or missing (FUNC OUT normal). | 6.3.7 |
| Excessive high frequency sine or triangle roll off, excessive square wave overshoot and rise/fall time. | 6.3.8 |
| Low frequency square wave tilt. | 6.3.9 |
| Time symmetry cannot be adjusted within specification. | 6.3.10 |
| Frequency accuracy and dial response problems. | 6.3.11 |
| Trigger, gate and trigger baseline problems. | 6.3.12 |
| Voltage at VCG IN connector not changing frequency properly. | 6.3.13 |
| DC offset not functioning correctly. | 6.3.14 |
| Variable symmetry problems | 6.3.15 |

6.3.1 Fuse Blows, No Dial Lamp

1. Fuse size incorrect for voltage setting.
2. Line voltage selector incorrectly positioned.
3. Disconnect P5. If ac voltages are now correct, refer to the power supply guide, paragraph 6.4.1. If not, inspect the transformer and power receptacle.

6.3.2 Power Supply > 100 mVp-p Ripple or Out of Specification

1. Check line voltage selector for correct position.
2. If the supply is 0V, check for a short between the faulty supply and ground by lifting the jumpers at rear of the board.
3. Lift P5 from the board. If the voltages at P5 are not close to the values shown on the schematic table, inspect the transformer and power receptacle. If the voltages are normal, connect P5, then lift the jumpers (rear of board) for faulty supply. If the supplies are still bad, refer to paragraph 6.4.1. If not, the problem is caused by an excessive current drain by the generator circuits.

6.3.3 All Waveforms at FUNC OUT Distorted or Missing

Improperly set controls:

1. OUTPUT ATTEN or AMPLITUDE controls incorrectly set too low for scope gain or voltmeter range.
2. FUNCTION switch incorrectly set to DC.
3. MODE switch incorrectly set to TRIG or GATE.
4. SYM or DC OFFSET buttons depressed.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Check for a nonlinear triangle. If the triangle is nonlinear on only one range, check for a leaky capacitor on that range. If the triangle is nonlinear in more than one range, check for leaky capacitors or faulty active components in the frequency multiplier and triangle buffer circuits.
3. If the waveform is bad in one of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to the capacitance multiplier guide 6.4.9.
4. If the waveform is bad only in 1M or 10M FREQ MULT positions, refer to paragraph 6.4.3. If the delay compensation circuit appears normal, refer to figure 6-1.
5. If square wave symmetry, measured at FUNC OUT, is out of specification and cannot be calibrated, refer to paragraph 6.3.10.
6. If none of the above conditions apply, refer to figure 6-1.

6.3.4 Square Wave Distorted or Missing

Improperly set controls:

1. SYM button depressed.
2. Excessive dc offset overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If symmetry is not in specification and cannot be calibrated refer to paragraph 6.3.10.
4. If none of the above conditions apply, refer to figure 6-2.

6.3.5 Sine Wave Distorted or Missing

Improperly set controls:

1. SYM button depressed
2. Excessive dc offset overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. Check the triangle for nonlinearity at FUNC OUT. If it is nonlinear, but only on one range, check for a leaky capacitor on that range. If the triangle is nonlinear on more than one range, check for a leaky capacitor or faulty active component in the frequency multiplier and triangle buffer circuits. (NOTE: Some nonlinearity above 200 kHz is normal and not specified.)
3. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
4. Verify that square wave symmetry, at FUNC OUT, is in specification. If not and cannot be calibrated, refer to paragraph 6.3.10.
5. If none of the above conditions apply, refer to figure 6-3.

6.3.6 Triangle Distorted or Missing

Improperly set controls:

1. SYM button depressed.
2. Excessive dc offset overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.

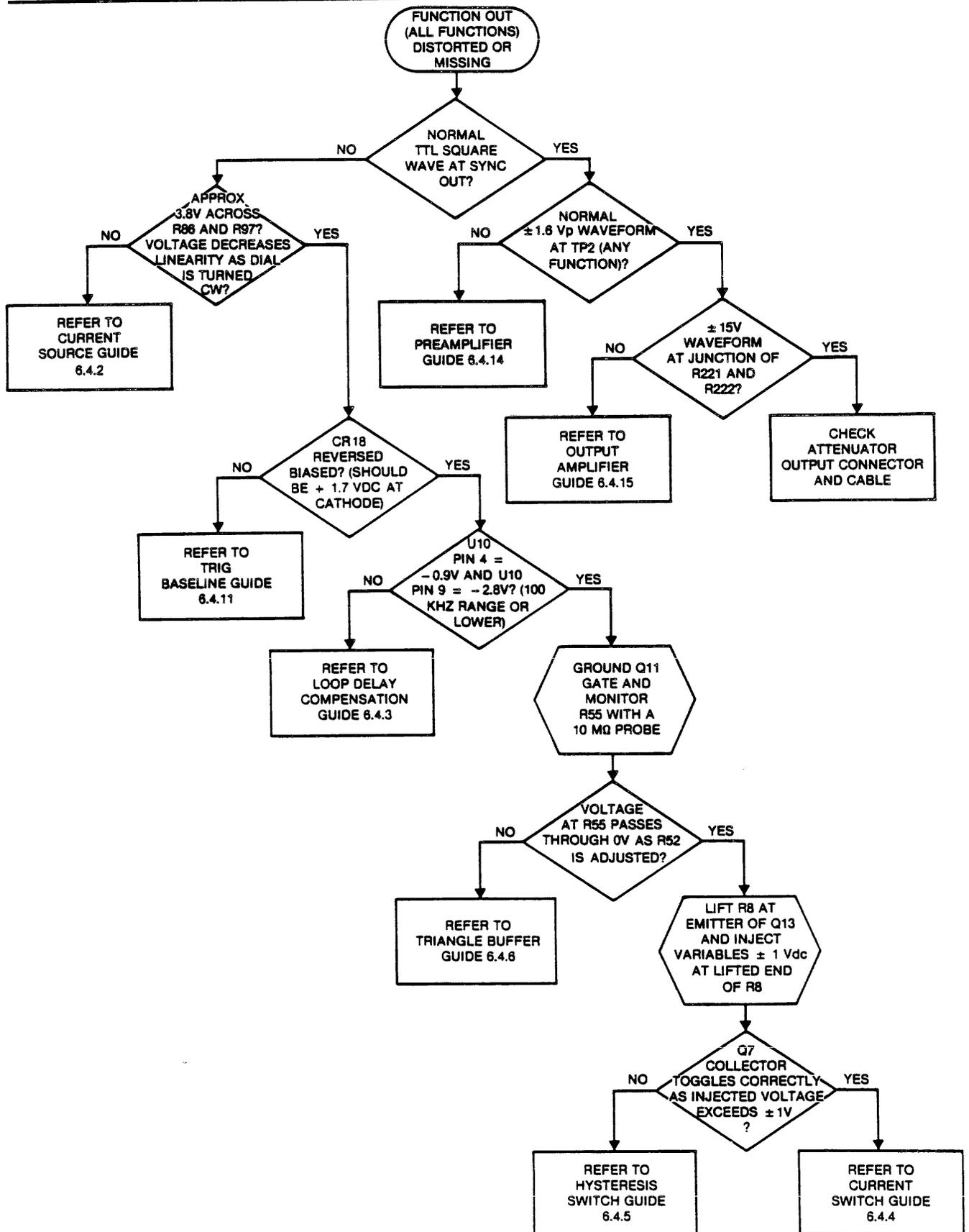


Figure 6-1. Function Output Troubleshooting

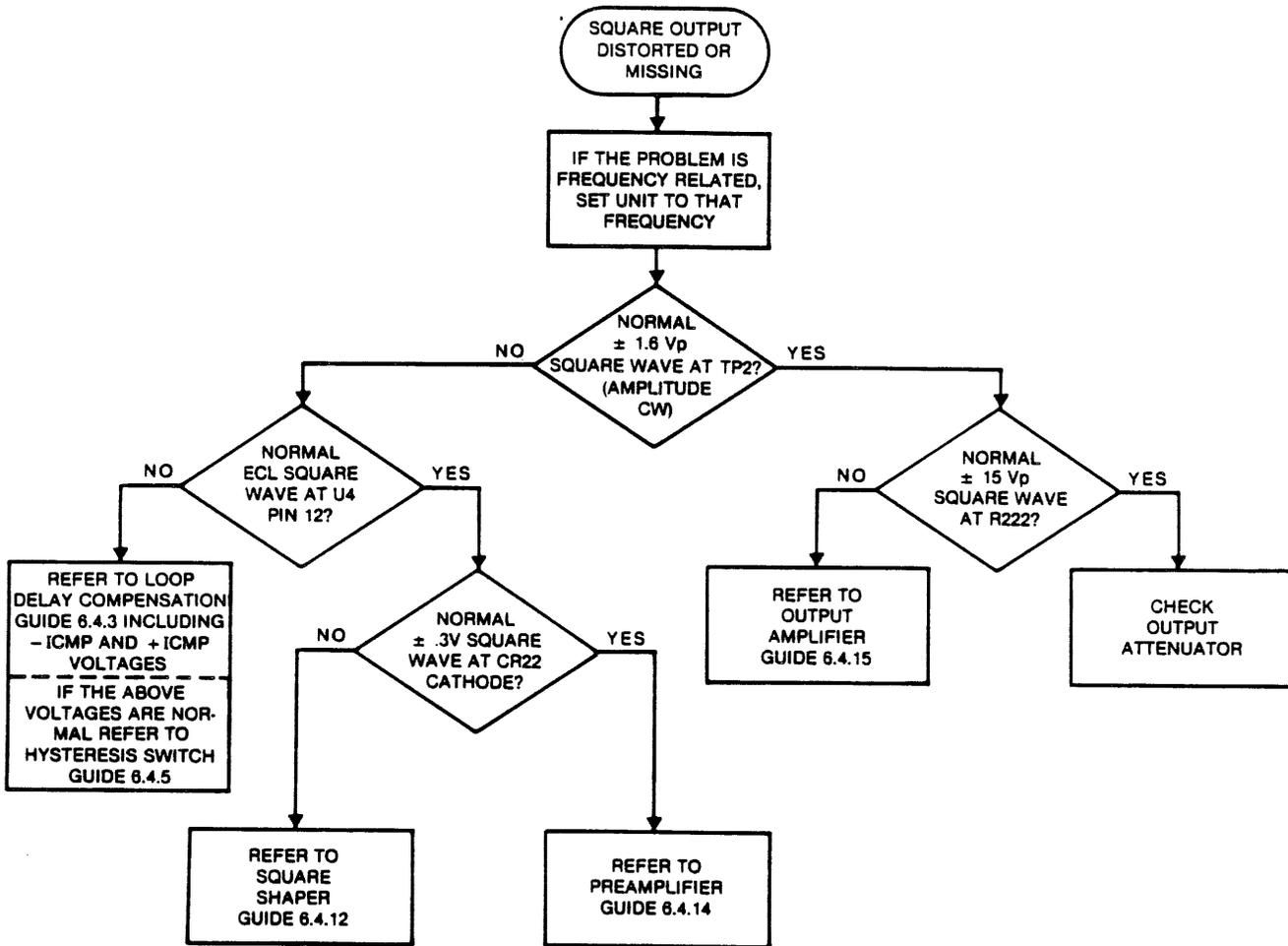


Figure 6-2. Square Output Troubleshooting

2. Check the triangle for nonlinearity at FUNC OUT. If it is nonlinear, but only on one range, check for a leaky capacitor on that range. If the triangle is nonlinear on more than one range, check for a leaky capacitor or faulty active component in the frequency multiplier and triangle buffer circuits. (NOTE: Some nonlinearity above 200 kHz is normal and not specified.)
3. If the waveform is bad in one or more of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
4. Verify square wave symmetry at FUNC OUT is in specification. If not and cannot be calibrated, refer to paragraph 6.3.10.
5. If none of the above conditions apply, refer to figure 6-4.

6.3.7 Sync Output Distorted or missing (FUNC OUT Normal)

Improperly set controls:

1. Because the FUNC OUT is normal, this cannot be caused by improperly set controls.

Functional block isolation:

1. If there is no ECL square wave at U6 pin 10, refer to paragraph 6.4.7. If there is an ECL square wave, refer to paragraph 6.4.8.

6.3.8 Excessive High Frequency Sine or Triangle Roll Off

Improperly set controls:

1. Excessive dc offset overdriving output amplifier.

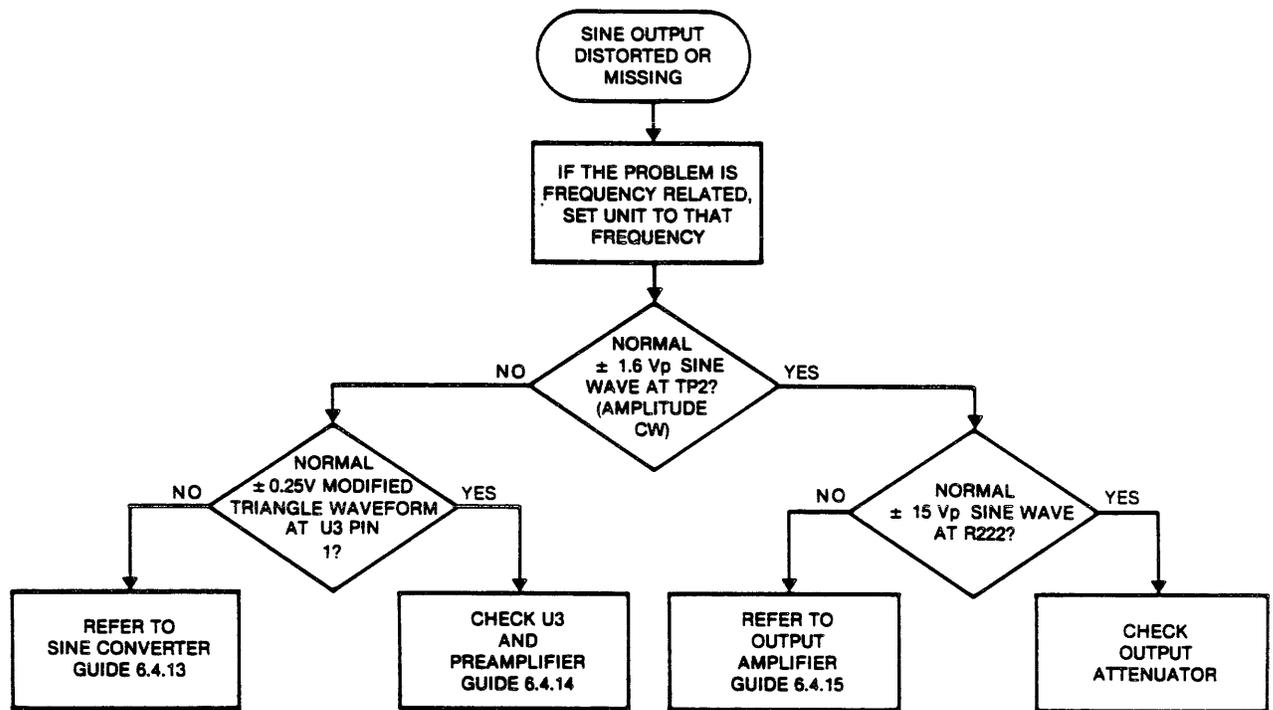


Figure 6-3. Sine Output Troubleshooting

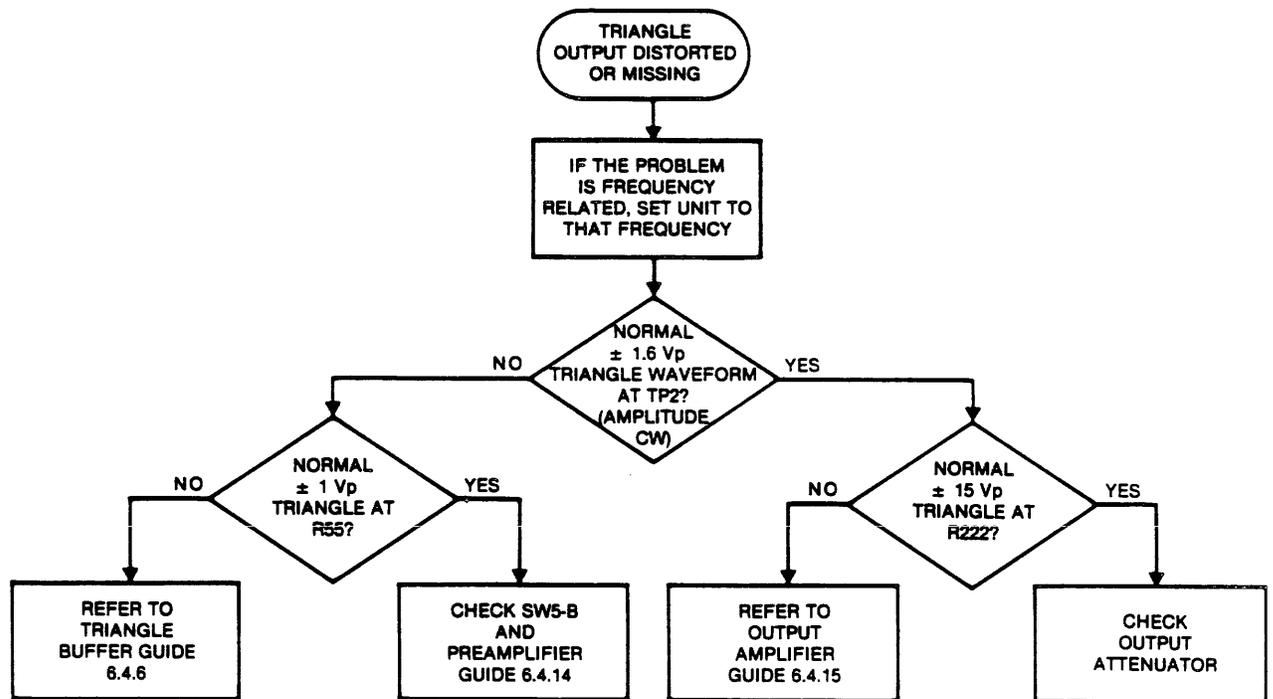


Figure 6-4. Triangle Output Troubleshooting

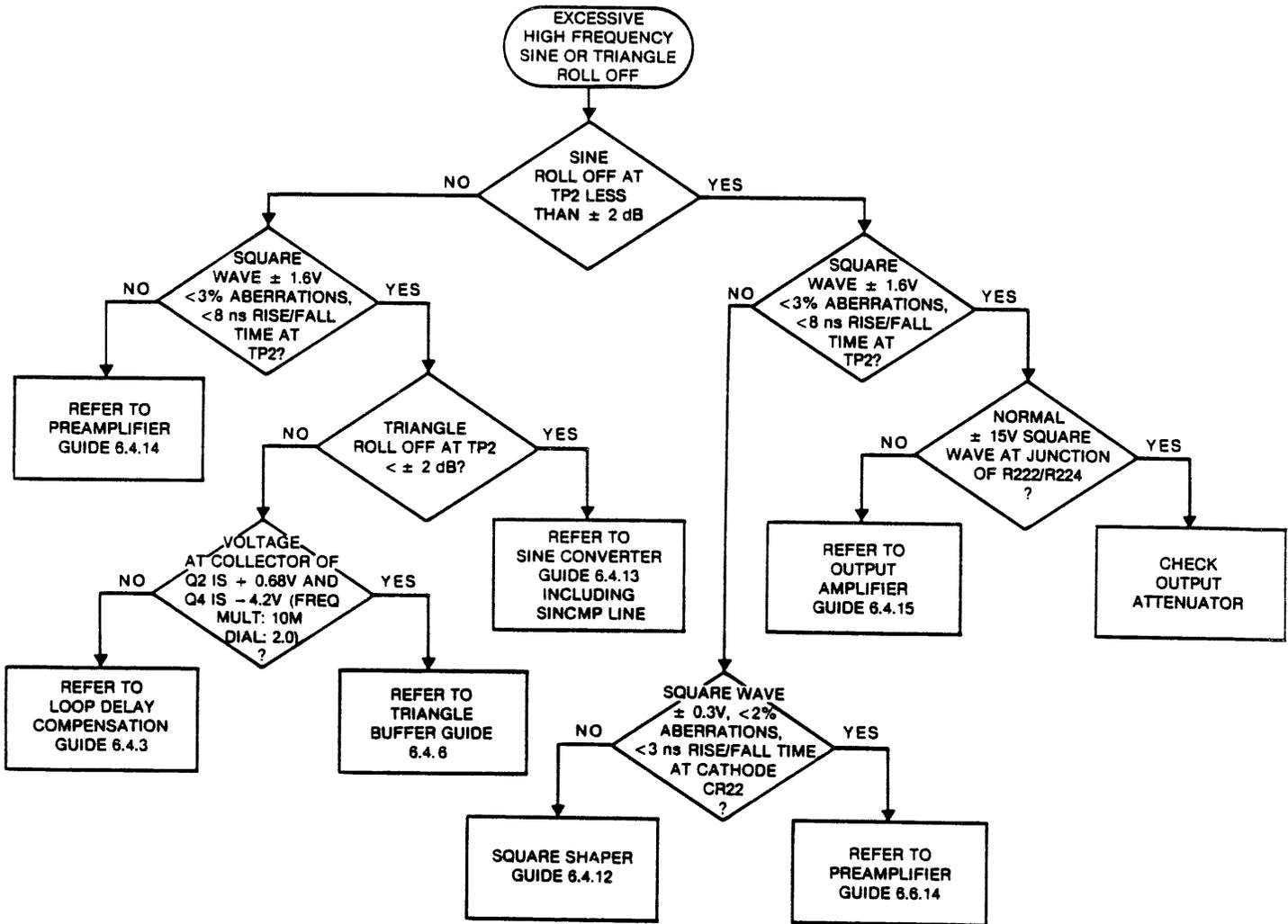


Figure 6-5. High Frequency Waveform Troubleshooting

2. Verify 50Ω load on the cable at oscilloscope end.

Functional block isolation:

1. Verify power supply voltages are within ±5% of nominal with less than 100 mVp-p of ac ripple. If not refer to paragraph 6.4.1. Use a X10 probe with a very short ground lead and a spectrum analyzer, RF voltmeter or a 200 MHz bandwidth scope when performing sine or triangle roll-off tests.
2. If none of the above conditions apply, refer to figure 6-5.

6.3.9 Low Frequency Square Wave Tilt

Improperly set controls:

1. Scope improperly set to ac.

Functional block isolation:

1. Verify power supply voltages are within ±5% of nominal, and less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1
2. If none of the above conditions apply, refer to figure 6-6.

6.3.10 Time Symmetry Cannot Be Adjusted To Within Specifications

Improperly set controls:

1. SYM button depressed.

Functional block isolation:

1. Verify power supply voltages are within ±5% of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.

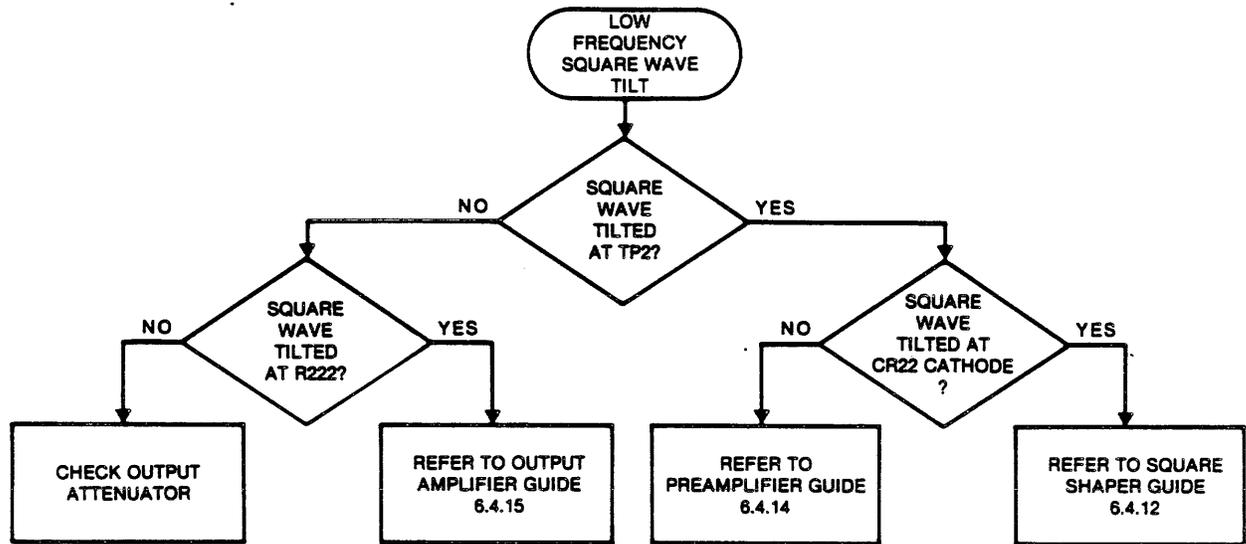


Figure 6-6. Low Frequency Square Wave Troubleshooting

2. If symmetry is out of specification in one of the four lowest ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If symmetry is out of specification on FREQ MULT settings 1M or 10M only, refer to paragraph 6.4.3.
4. If the voltages across R86 and R97 are not equal (typically 3.8V, Freq Dial: 2.0 Freq Mult: 100K or less), refer to paragraph 6.4.2.

6.3.11 Frequency Accuracy and Dial Response Problems

Improperly set controls:

1. SYM button depressed.
2. External signal connected to VCG in BNC.
3. VERNIER not in FREQ CAL position.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal with less than 100 mVp-p ac ripple. If not, refer to paragraph 6.4.1.
2. If the problem occurs in one of the four lowest frequency ranges (.1, 1, 10, 100), but the remaining ranges are normal, refer to paragraph 6.4.9.
3. If the frequency accuracy is out of specification on FREQ MULT settings 1M and 10M, refer to paragraph 6.4.3.
4. If the frequency is out of specification, but only on one range, check the range capacitor for that range.

5. If the problem occurs on the 1K, 10K, or 100K range, check the range capacitor.
6. On the 1K range and frequency dial set at 2.0, check for 3.8V across R86 and R97. As the dial is rotated, this voltage should linearly track the dial settings within $\pm 3\%$ of full scale. If not, refer to paragraph 6.4.2.
7. If none of the above conditions apply, refer to figure 6-7.

6.3.12 Trigger, Gating and Trigger Baseline Problems.

Improperly set controls:

1. MODE incorrectly set to CONT.
2. FUNCTION incorrectly set to DC.
3. DC OFFSET overdriving output amplifier.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of nominal, with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. If the trigger baseline cannot be calibrated within specification, set MODE to GATE and monitor the emitter of Q19. With TRIG IN disconnected, rotate the TRIG LEVEL ccw. The voltage should go about -0.7 Vdc. Rotating the TRIG LEVEL cw should change this voltage to about $+1.8$ Vdc. If these voltage readings are normal, check CR18 and CR19.

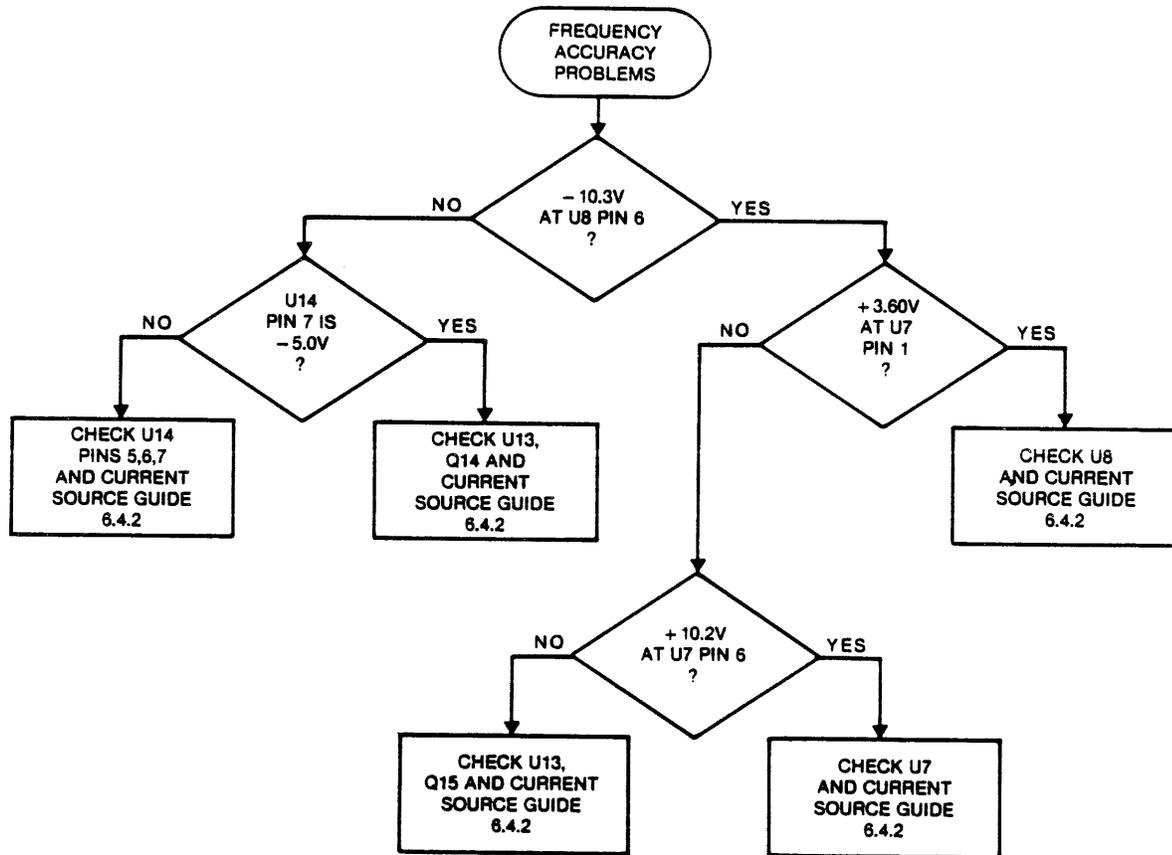


Figure 6-7. Frequency Accuracy Troubleshooting

3. If none of the above conditions apply, refer to figure 6-8.

4. For high frequency (1M and 10M ranges) trigger or gate problems, set the controls as follows:

| | |
|----------------|---|
| Frequency Dial | 2.0 |
| FREQ MULT: | 10M |
| SYM: | OFF |
| MODE: | TRIG or GATE (Depends on symptom- GATE preferred) |
| TRIG LEVEL: | 12 o'clock |

Set the scope as follows:

| | |
|-------------|-----------|
| Horizontal: | 20 ns/div |
| Vertical: | 1 V/div |

Inject a 15 MHz 1 Vp-p trigger signal and refer to figure 6-9.

6.3.13 Voltage At VCG IN Connector Not Changing Frequency Properly

Improperly set controls:

1. Excessive VCG IN voltage for dial setting (maxi-

mum input voltage is + 5.0 Vdc with the dial set at .02 and the Freq VERNIER turned ccw).

Functional block isolation:

1. Set the frequency dial to 2.0, FREQ MULT to 1K, and VCG IN with no input. Measure voltage across R86 and R97 (+ 3.8 Vdc). In addition, as the frequency dial is rotated, the voltage linearly tracks the dial settings within $\pm 3\%$ full scale. If it functions properly, check R67, R68, R69 and associated circuitry, but if not, refer to paragraph 6.3.11.

6.3.14 DC Offset Not Functioning Correctly

Improperly set controls:

1. Signal peak plus offset exceeding + or - 7.5V (with a 50Ω load), or $\pm 15V$ open circuit.
2. Check OUTPUT ATTEN since this also attenuates output offset.

Functional block isolation:

1. Verify power supply voltages are within $\pm 5\%$ of

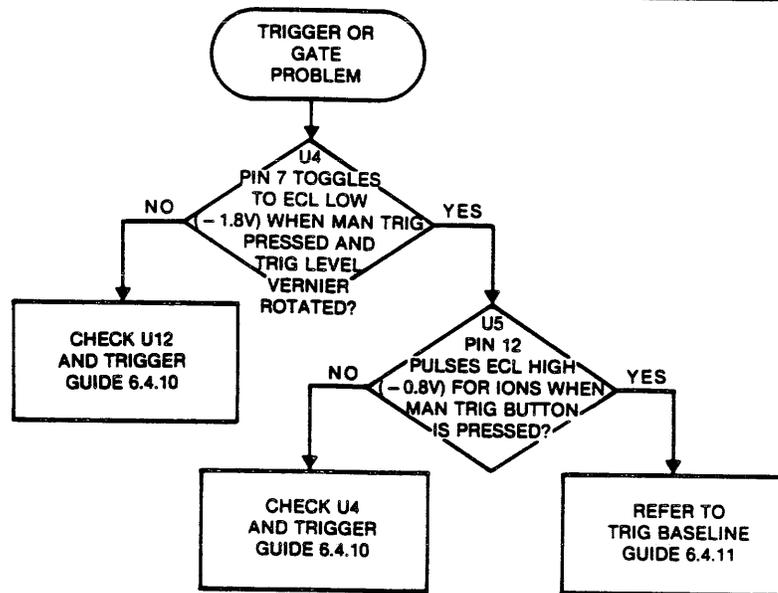


Figure 6-8. Trigger Gate Troubleshooting

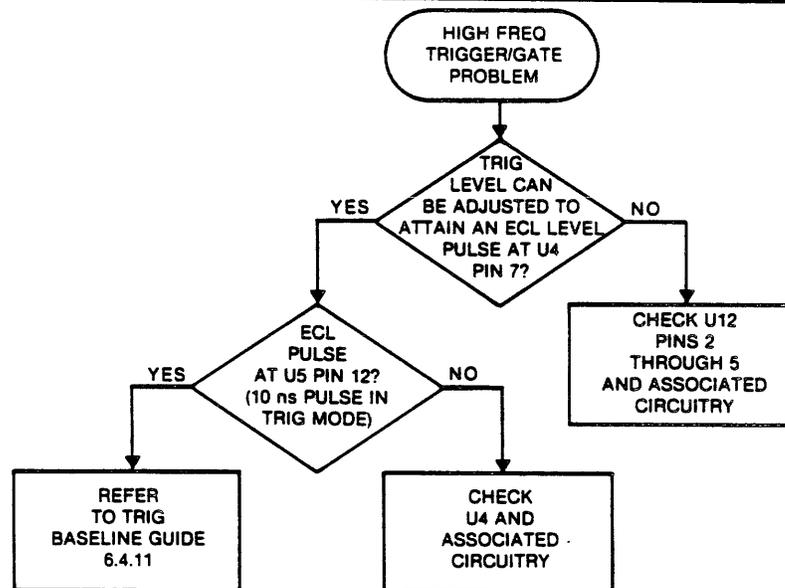


Figure 6-9. High Frequency Trigger/Gate Troubleshooting

nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.

2. Take the following voltage measurements with the DC OFFSET button depressed and the DC OFFSET control rotated cw:
 - a) The junction of R260 and C116 should vary from +8.0V to -8.0V as control is rotated.
 - b) U2 pin 2 should hold at 0.0V.
 - c) U2 pin 6 should vary from -1.0V to +1.0V. (Drifting of this voltage is typical because of

constant compensation by U2 of variations in output transistor currents.)

3. If none of the above conditions apply, refer to paragraph 6.4.15.

6.3.15 Variable Symmetry Problems

Improperly set controls:

1. SYM button is incorrectly extended.
2. Note: When SYM is depressed the output frequency should be one-tenth the selected frequency.
3. DC offset is overdriving the output amplifier.

Functional block isolation:

1. Verify power supply voltages within $\pm 5\%$ of nominal with less than 100 mVp-p of ac ripple. If not, refer to paragraph 6.4.1.
2. When the voltage at the right leg of R88 (VERNIER/SYM CW) is $-15V$ and when the voltage at the left leg of R88 (VERNIER/SYM) is $-15V$, refer to paragraph 6.4.2. If not, check R88 and SW8.

6.4 CIRCUIT GUIDES

Circuit guides provide listings of voltage levels, waveforms, and hints that, when used with the schematics, are helpful in isolating faulty circuits. Table 6-2 is an index of circuit guides.

Table 6-2. Circuit Guide Index

| Circuit Guide | Paragraph |
|-------------------------|-----------|
| Power Supply | 6.4.1 |
| Current Source | 6.4.2 |
| Loop Delay Compensation | 6.4.3 |
| Current Switch | 6.4.4 |
| Hysteresis Switch | 6.4.5 |
| Triangle Buffer | 6.4.6 |
| Zero Crossing Detector | 6.4.7 |
| Sync | 6.4.8 |
| Capacitance Multiplier | 6.4.9 |
| Trigger | 6.4.10 |
| Trig Baseline | 6.4.11 |
| Square Shaper | 6.4.12 |
| Sine Converter | 6.4.13 |
| Preamplifier | 6.4.14 |
| Output Amplifier | 6.4.15 |

6.4.1 Power Supply Guide

1. To determine a faulty power supply, check for the voltages given in table 6-3.
2. If the regulator input is bad, remove P5 and check for:
 - a. Shorted or open diodes (CR1, CR2, or CR3).
 - b. Shorted or open capacitors at the input of the regulator.
 - c. Short between the regulator metal mounting tab and chassis ground.

3. If the regulator input is good, check for:
 - a. Shorted or open capacitors at the output of the regulator.
 - b. Short between regulator metal mounting tab and chassis ground.
 - c. Excessive loading by main board circuits; to verify, lift jumper of the appropriate supply.
 - d. If all of the above conditions appear normal, replace the voltage regulator.

Table 6-3. Power Supply Checks

| Supply | Voltage Tolerance | Maximum Regulator Input Ripple (p-p) | Maximum Regulator Output Ripple (p-p) |
|-------------------|-------------------------|--------------------------------------|---------------------------------------|
| $\pm 15V$ Balance | $30 \pm 1.5 Vdc$ (a) | — | — |
| +15V | (b) | 1.5 Vac | 10 mV |
| -15V | (c) | 1.5 Vac | 10 mV |
| +5V | $\pm 750 mV$ | 1.5 Vac | 10 mV |
| -5V | $\pm 750 mV$ | 1.5 Vac | 10 mV |
| +23V | $\pm 1.15 Vdc$ | 1.5 Vac | 10 mV |
| -23V | $\pm 1.15 Vdc$ | 1.5 Vac | 10 mV |

(a) Measured between +15V and -15V supplies.
 (b) Measure and note +15V supply (V_{+15}).
 (c) $-15V$ supply = $-|V_{+15} \pm .01V|$.

6.4.2 Current Source Guide

Top of Dial Check: Set the controls as follows; then perform the checks in table 6-4.

| Control | Setting |
|----------------|----------------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| VERNIER | FREQ CAL |
| SYM | Off (extended) |
| VCG IN | Disconnected |

VCG Check: Set the controls as follows; then perform the checks in table 6-5.

| Control | Setting |
|----------------|----------------|
| Frequency Dial | .02 |
| FREQ MULT | 1K |
| VERNIER | Full ccw |
| SYM | Off (extended) |
| VCG IN | +5.0 Vdc input |

Table 6-4. Current Source Check (Top of Dial)

| Test Point | Desired Results |
|----------------------------|------------------|
| U14 pin 7 | -5 ± .5 Vdc |
| U13 pins 1, 2 | -5 ± .5 Vdc |
| Measure across R83 | +3.8 ± .38 Vdc |
| U8 pin 6 | -10.3 ± 1.03 Vdc |
| Measure across R84 and R93 | +3.8 ± .38 Vdc |
| U13 pin 6 | 0 ± .01 Vdc |
| U7 pin 6 | +10.2 ± 1.02 Vdc |
| Measure across R86 and R97 | +3.8 ± .38 Vdc |

Table 6-5. Current Source (VCG IN)

| Test Point | Desired Results |
|------------------------------|-------------------|
| U7 pin 6 | +14.38 ± 1.44 Vdc |
| U8 pin 6 (disconnect VCG IN) | -14.3 ± 1.43 Vdc |

10 MHz Range Check: Set the controls as shown below, then perform the checks in table 6-6.

| Control | Setting |
|----------------|----------------|
| Frequency Dial | 2.0 |
| FREQ MULT | 10M |
| VERNIER | FREQ CAL |
| SYM | Off (extended) |
| VCG IN | Disconnected |

Table 6-6. Current Source Check (10 MHz Range)

| Test Point | Desired Results |
|--------------------|-----------------|
| Measure across R99 | +5.9 ± .59 Vdc |
| Measure across R83 | +6.05 ± .61 Vdc |
| U8 pin 6 | -8.2 ± .82 Vdc |

Variable Symmetry Check: Set the controls as shown then measure the voltage across resistors R84, R85, R86, R87, R93, and R97. The measured voltages should read +0.38 ± .04V.

| Control | Setting |
|----------------|---------------------|
| Frequency Dial | 2.0 |
| VERNIER | 12 c'clock position |
| VCG IN | Disconnected |
| FREQ MULT | 1K |
| SYM | On (depressed) |

6.4.3 Loop Delay Compensation Guide

Set the controls as shown; then perform the checks in table 6-7.

| Control | Setting |
|----------------|----------------|
| Frequency Dial | 2.0 |
| VERNIER | FREQ CAL |
| VCG IN | Disconnected |
| FREQ MULT | 10M |
| SYM | Off (extended) |

Table 6-7. Loop Delay Compensation Checks

| Test Point | Desired Results |
|--------------------------------|---------------------------------------|
| Q1 and Q2 emitters | + 9.2 ± .92 Vdc |
| Q1 base and collector, Q2 base | +8.5 ± .9 Vdc |
| Q2 collector | +0.68 ± .07 Vdc |
| Q3 and Q4 emitter | -9.05 ± .91 Vdc |
| Q3 and Q4 base | -8.32 ± .83 Vdc |
| Q3 collector | |
| Q4 collector | -4.2 ± .42 Vdc |
| U10 pin 4 | -1.6 ± .16 Vdc (+ Peak reference) |
| U10 pin 9 | -2.17 ± .22 Vdc (- Peak reference) |

6.4.4 Current Switch Guide

Set the controls as shown; then take waveform measurements. Refer to figure 6-10.

| Control | Setting |
|----------------|----------------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off (extended) |
| MODE | CONT |

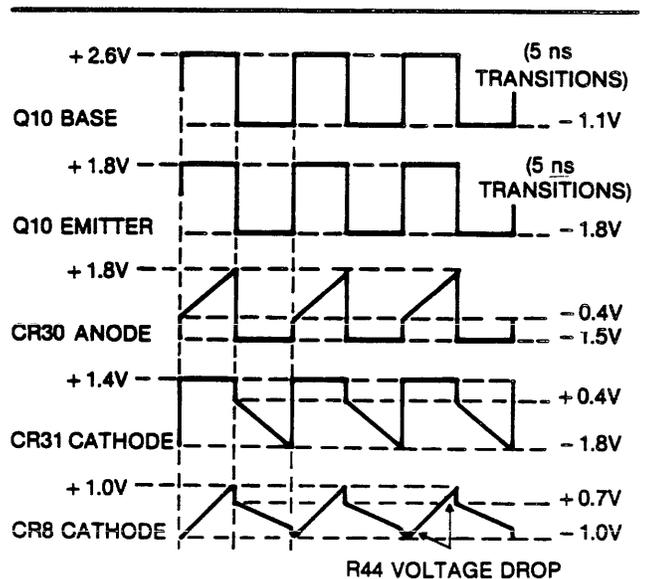


Figure 6-10. Current Switch Waveforms

6.4.5 Hysteresis Switch Guide

Set the controls as shown; then perform the checks in table 6-8 and take waveform measurements. Refer to figure 6-11.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off |
| MODE | CONT |

Table 6-8. Hysteresis Switch Guide

| Test Point | Desired Results |
|--------------------|--|
| U10 pin 4 | $-0.9 \pm .09$ Vdc (+ Peak reference) |
| U10 pin 9 | $-2.8 \pm .28$ Vdc (- Peak reference) |
| Q7 and Q8 emitters | $-3.0 \pm .3$ Vdc |

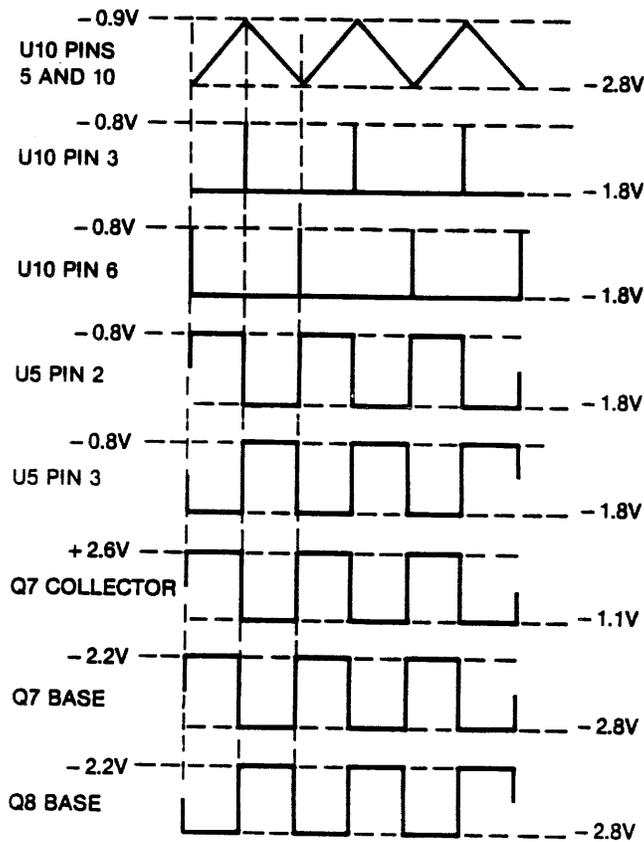


Figure 6-11. Hysteresis Switch Waveforms

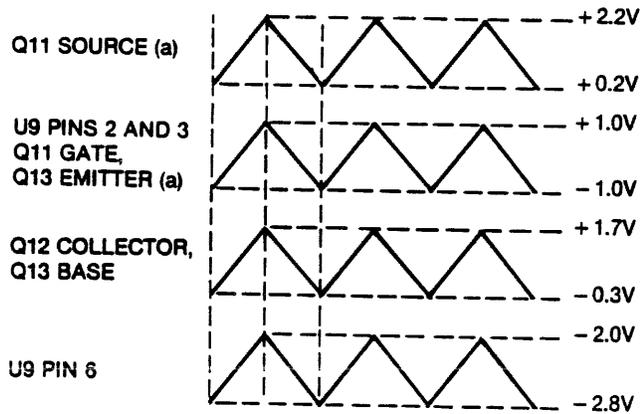
6.4.6 Triangle Buffer Guide

Set the controls as shown; then perform the checks in table 6-9 and take waveform measurements. Refer to figure 6-12. If, after setting the controls, the generator loop does not run, lift R45 at E23 and inject a $\pm 1.0V$ triangle into R45.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off |
| MODE | CONT |

Table 6-9. Triangle Buffer Checks

| Test Point | Desired Results |
|---------------|--|
| Q11 drain | $+6.5 \pm .65$ Vdc |
| Q12 emitter | $0.3 \pm .03$ Vp-p triangle, offset -10 ± 1 Vdc |
| Q12 base | $0.3 \pm .03$ Vp-p triangle, offset $-9.3 \pm .9$ Vdc |
| Q13 collector | $+5.0 \pm .5$ Vdc |



(a) Requires a X10 Probe (high impedance)

Figure 6-12. Triangle Buffer Waveforms

6.4.7 Zero Crossing Detector Guide

Set the controls as shown; then take waveform measurements. Refer to figure 6-13.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off |
| MODE | CONT |

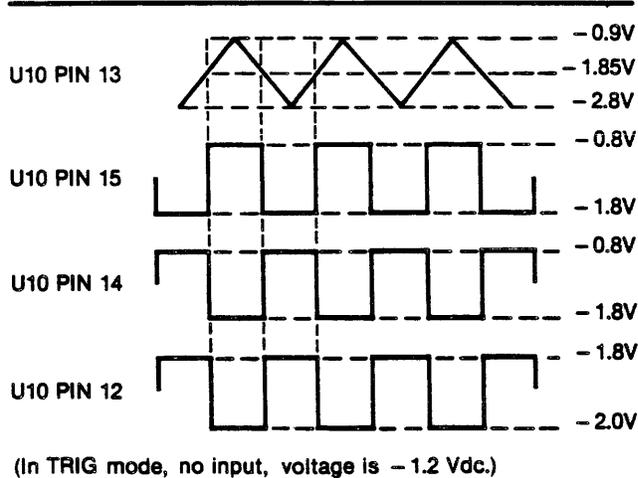


Figure 6-13. Zero Crossing Detector Waveforms

6.4.8 Sync Guide

Set the controls as shown then perform the checks in table 6-10 and take waveform measurements. See figure 6-14.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off |
| MODE | CONT |

Table 6-10. Sync Check

| Test Point | Desired Results | |
|------------------|---------------------------------|-----------------------|
| | Function: Sine or Triangle Wave | Function: Square Wave |
| CR4 cathode | +1.2 ± .12 Vdc | -5 ± .5 Vdc |
| U6 pins 4 and 6 | -1 ± .1 Vdc | -4.3 ± .43 Vdc |
| U6 pins 2 and 11 | -1.8 ± .18 Vdc | -0.8 ± .08 Vdc |
| Q5/Q6 emitters | -1.6 ± .16 Vdc | -1.6 ± .16 Vdc |

6.4.9 Capacitance Multiplier Guide

Set the controls as shown; then take the waveform measurements. Refer to figure 6-15.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 100 |
| SYM | Off |
| MODE | CONT |

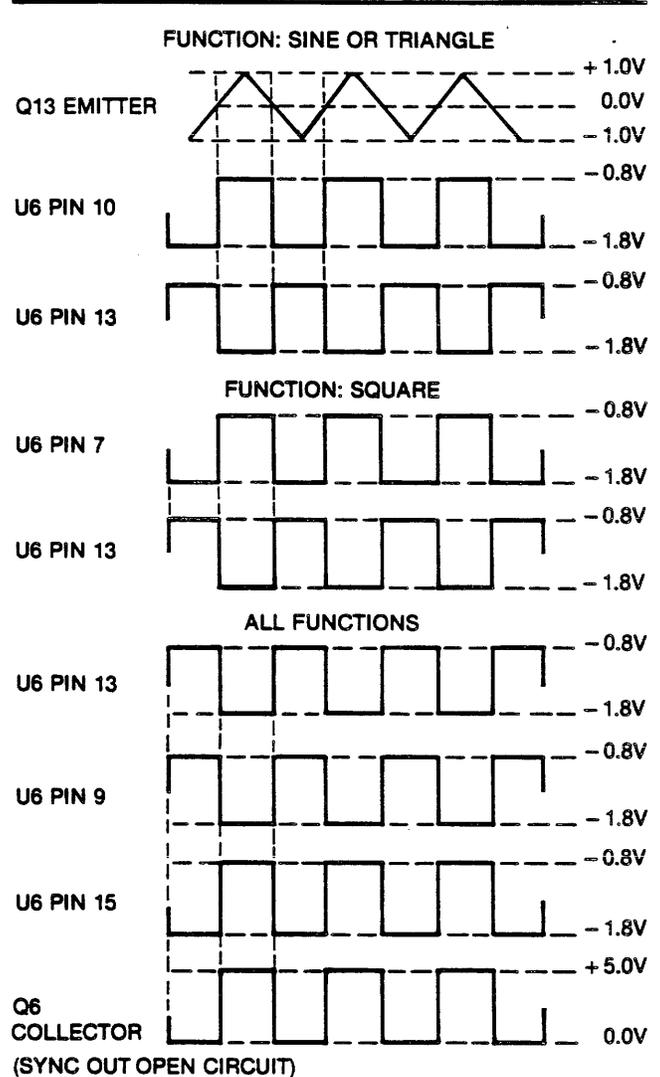


Figure 6-14. Sync Waveforms

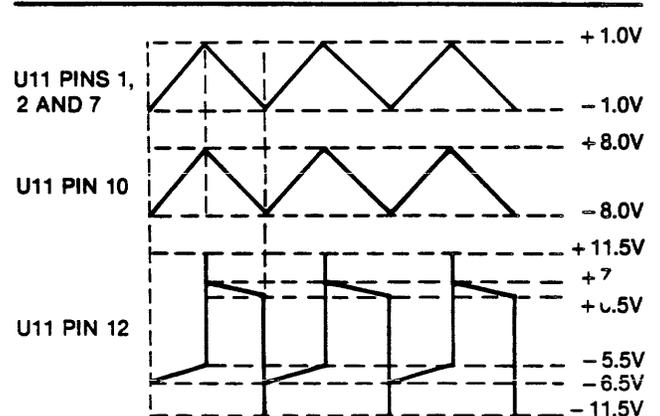


Figure 6-15. Capacitance Multiplier Waveforms

6.4.10 Trigger Guide

TRIG or CONT Check: Set the controls as shown; then take the waveform measurements. Refer to figure 6-16.

| Control | Setting |
|----------------|----------------------------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| MODE | TRIG or CONT |
| TRIG IN | $\pm 1V$ 1 kHz Square wave |

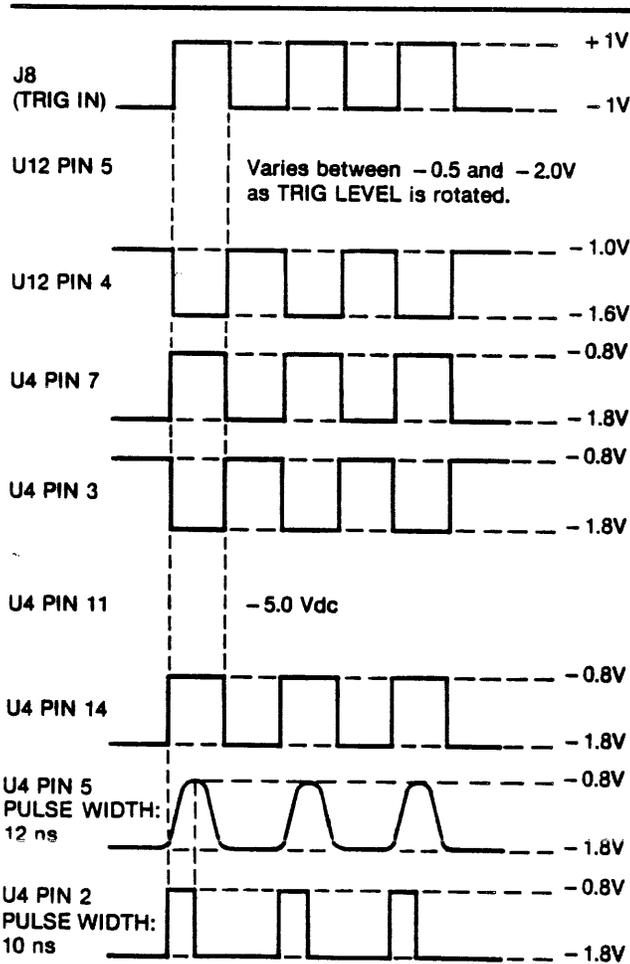


Figure 6-16. Trigger Waveforms (TRIG or CONT)

GATE Checks: Set the controls as shown; then take the waveform measurements. Refer to figure 6-17.

| Control | Setting |
|----------------|----------------------------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| MODE | GATE |
| TRIG IN | $\pm 1V$ 1 kHz Square wave |

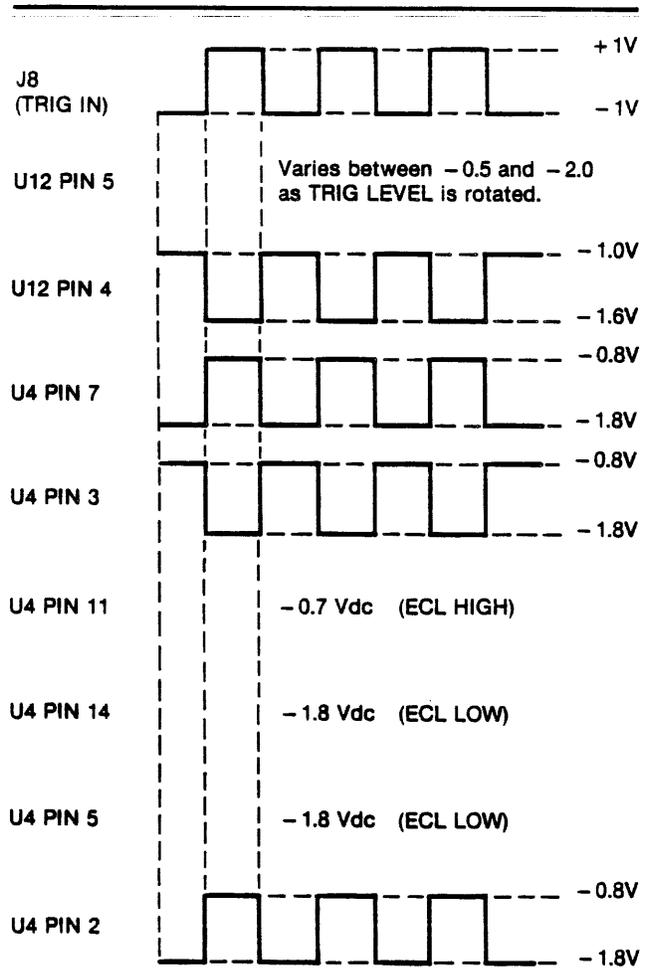


Figure 6-17. Trigger Waveforms (Gate)

6.4.11 Trigger Baseline Guide

Trigger or Gate Mode Problems: Set the controls as shown; then take the waveform measurements. Refer to figure 6-18.

| Control | Setting |
|----------------|---|
| Frequency Dial | 2.0 |
| FREQ MULT | 10K |
| SYM | Off |
| MODE | TRIG or GATE (Depends on symptom—GATE preferred) |
| TRIG LEVEL | Approximately centered |
| TRIG IN | $\pm 1V$ 10 kHz Square wave |

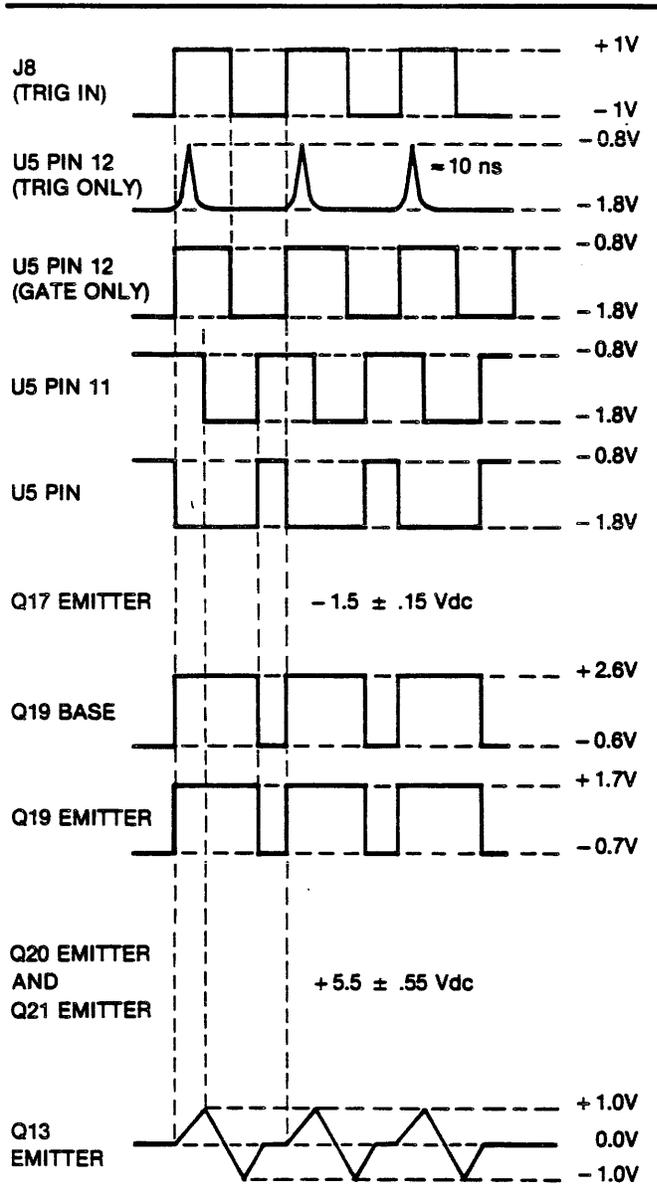


Figure 6-18. Trigger Baseline Waveforms

Continuous Mode Problems: Set the controls as shown; then take the waveform measurements. Refer to table 6-11.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 10K |
| SYM | Off |
| MODE | CONT |

Table 6-11. Trigger Baseline Check (Continuous)

| Test Point | Desired Results |
|-------------|-----------------|
| U5 pin 12 | -0.8 ± .08 Vdc |
| U5 pin 14 | -1.8 ± .18 Vdc |
| Q17 emitter | -1.5 ± .15 Vdc |
| Q19 base | +2.6 ± .26 Vdc |
| Q19 emitter | +1.7 ± .17 Vdc |
| Q20 emitter | +5.5 ± .55 Vdc |
| Q21 emitter | +5.5 ± .55 Vdc |
| Q13 emitter | ± 1.0V triangle |

6.4.12 Square Shaper Guide

Set the controls as shown; then perform the checks in table 6-12, and take waveform measurements. Refer to figure 6-19.

| Control | Setting |
|----------------|--------------------------------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off |
| MODE | CONT |
| FUNCTION | See Table 6-12 and Figure 6-19 |

Table 6-12. Square Shaper Checks

| Test Point | Desired Results | |
|-------------|------------------|----------------|
| | Sine or Triangle | Square |
| Q22 emitter | -3.0 ± .3 Vdc | -3.0 ± .3 Vdc |
| U4 pin 13 | -0.8 ± .08 Vdc | -4.3 ± .43 Vdc |
| Q26 base | -0.8 ± .08 Vdc | -4.2 ± .42 Vdc |
| Q26 emitter | -1.6 ± .16 Vdc | -4.0 ± .4 Vdc |
| CR24 anode | +1.6 ± .16 Vdc | -1.5 ± .15 Vdc |

6.4.13 Sine Converter Guide

Set the controls as shown; then perform the checks in table 6-13 and take waveform measurements. Refer to figure 6-20.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off |
| MODE | CONT |
| FUNCTION | Sine |

Table 6-13. Sine Converter Checks

| Test Point | Desired Results |
|------------------------|----------------------------------|
| Junction R170 and R171 | +14.8 ± 1.5 Vdc |
| Junction R173 and R174 | -14.8 ± 1.5 Vdc |
| U3 pin 2 | 0.0V (Full scale current = 2 mA) |

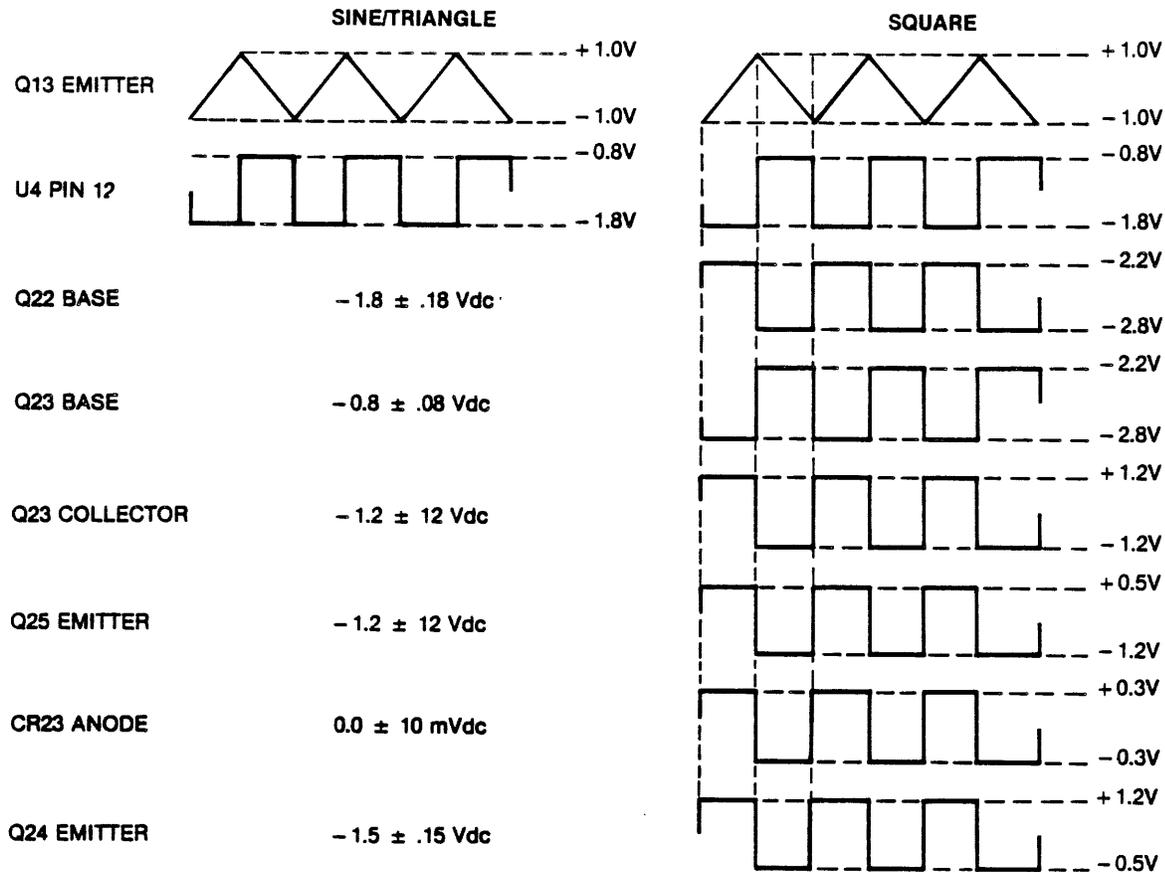


Figure 6-19. Square Shaper Waveforms

6.4.14 Preampifier Guide

DC Problems: Set the FUNCTION control to DC; then perform the checks in table 6-14.

Table 6-14. Preampifier Checks (DC)

| Test Point | Desired Results |
|---------------|------------------|
| U1 pin 2 | +14.86 ± 1.5 Vdc |
| U1 pin 3 | -0.7 ± .07 Vdc |
| U1 pin 13 | -1.4 ± .14 Vdc |
| U1 pin 9 | -0.7 ± .07 Vdc |
| U1 pin 4 | 0.0 ± 10 mV |
| U1 pin 8 | 0.0 ± 10 mV |
| U1 pin 12 | +5.8 ± .58 Vdc |
| U1 pin 11 | +6.6 ± .66 Vdc |
| Q27 base | +9.6 ± .96 Vdc |
| Q27 emitter | +10.3 ± 1 Vdc |
| Q28 collector | +11.3 ± 1.1 Vdc |

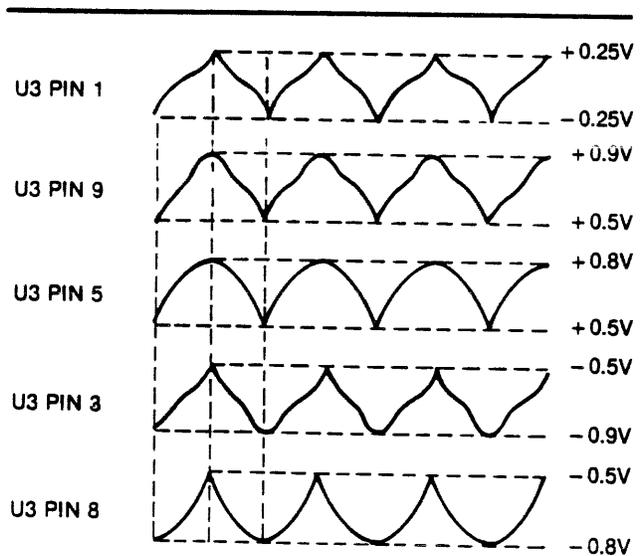


Figure 6-20. Sine Converter Waveforms

Function Problems: Set the controls as shown; then take the waveform measurements. Refer to figure 6-21.

| Control | Setting |
|----------------|---------|
| Frequency Dial | 2.0 |
| FREQ MULT | 1K |
| SYM | Off |
| MODE | CONT |
| FUNCTION | Square |

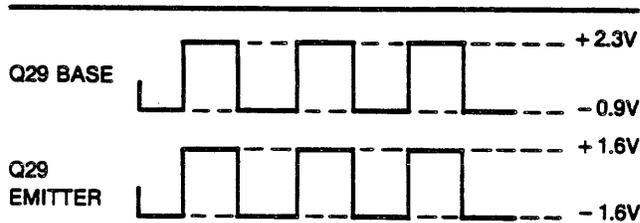


Figure 6-21. Preampifier Waveforms

6.4.15 Output Amplifier Guide

Set the controls as shown; then take the waveform measurements. Refer to table 6-15.

| Control | Setting |
|-----------|---------|
| FUNCTION | DC |
| DC OFFSET | Off |

6.5 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.5.1 Transistor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.
2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.
3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage (or reversed bias), the transistor is defective.
4. A transistor is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).

Table 6-15. Output Amplifier Checks

| Test Point | Desired Results | |
|------------|-----------------|-------------------|
| Q30 | Base | + 11.7 ± 1.2 Vdc |
| | Emitter | + 11 ± 1.1 Vdc |
| | Collector | + 19 ± 1.9 Vdc |
| Q32 | Collector | + 22.8 ± 2.3 Vdc |
| Q31 | Base | - 12 ± 1.2 Vdc |
| | Emitter | - 11.3 ± 1.1 Vdc |
| | Collector | - 19 ± 1.9 Vdc |
| Q33 | Collector | - 22.7 ± 2.3 Vdc |
| Q36 | Base | + 18.3 ± 1.8 Vdc |
| | Emitter | + 19 ± 1.9 Vdc |
| | Collector | + 0.7 ± .07 Vdc |
| Q37 | Emitter | + 0.05 ± .003 Vdc |
| | Collector | + 22.5 ± 2.3 Vdc |
| Q38 | Emitter | + 0.05 ± .005 Vdc |
| CR27 | Cathode | + 23 ± 2.3 Vdc |
| | Anode | + 0.6 ± .06 Vdc |
| VR5 | Input | + 31 ± 3.1 Vdc |
| | Output | + 24 ± 2.4 Vdc |
| Q34 | Collector | + 22.8 ± 2.3 Vdc |
| Q39 | Base | - 18.3 ± 1.8 Vdc |
| | Emitter | - 19 ± 1.9 Vdc |
| | Collector | - 0.05 ± .005 Vdc |
| Q40 | Emitter | - 0.05 ± .005 Vdc |
| | Collector | - 21 ± 2.1 Vdc |
| Q41 | Emitter | - 0.05 ± .005 Vdc |
| CR28 | Anode | - 23 ± 2.3 Vdc |
| Q35 | Base | - 0.6 ± .06 Vdc |
| VR6 | IN | - 31 ± 3.1 Vdc |
| | ADJ | - 21.3 ± 2.1 Vdc |
| | OUT | - 23.6 ± 2.4 Vdc |
| U2 | Pin 2 | 0.0 ± 10 mVdc |
| | Pin 6 | - 0.05 ± .005 Vdc |

5. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise, one of the transistors is defective.

6.5.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.5.3 Operational Amplifier

1. The "+" and "-" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.
2. When the output of the amplifier is connected to the "-" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "-" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.5.4 FET Transistor

1. No gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective.
2. The gate-to-source voltage is always reverse biased under a normal operating condition; e.g.,

the source voltage is more positive than the gate voltage for 2N5485, and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

3. If the device supplying gate voltage to an FET saturates, the FET has too large a V_{gs} (pinch off) for the circuit and should be replaced.

6.5.5 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.
3. Leaky capacitors will often have a decreased voltage across their terminals.

6.5.6 Digital ECL ICs

1. The device is operating correctly if the output high state is -0.81 to -0.96 V and low state is -1.65 to -1.85 V.
2. The input must show the same two levels as in step 1.

7

SECTION PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Whenever this occurs, errata pages are prepared and placed in the shipping container along with the instrument and current manual. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

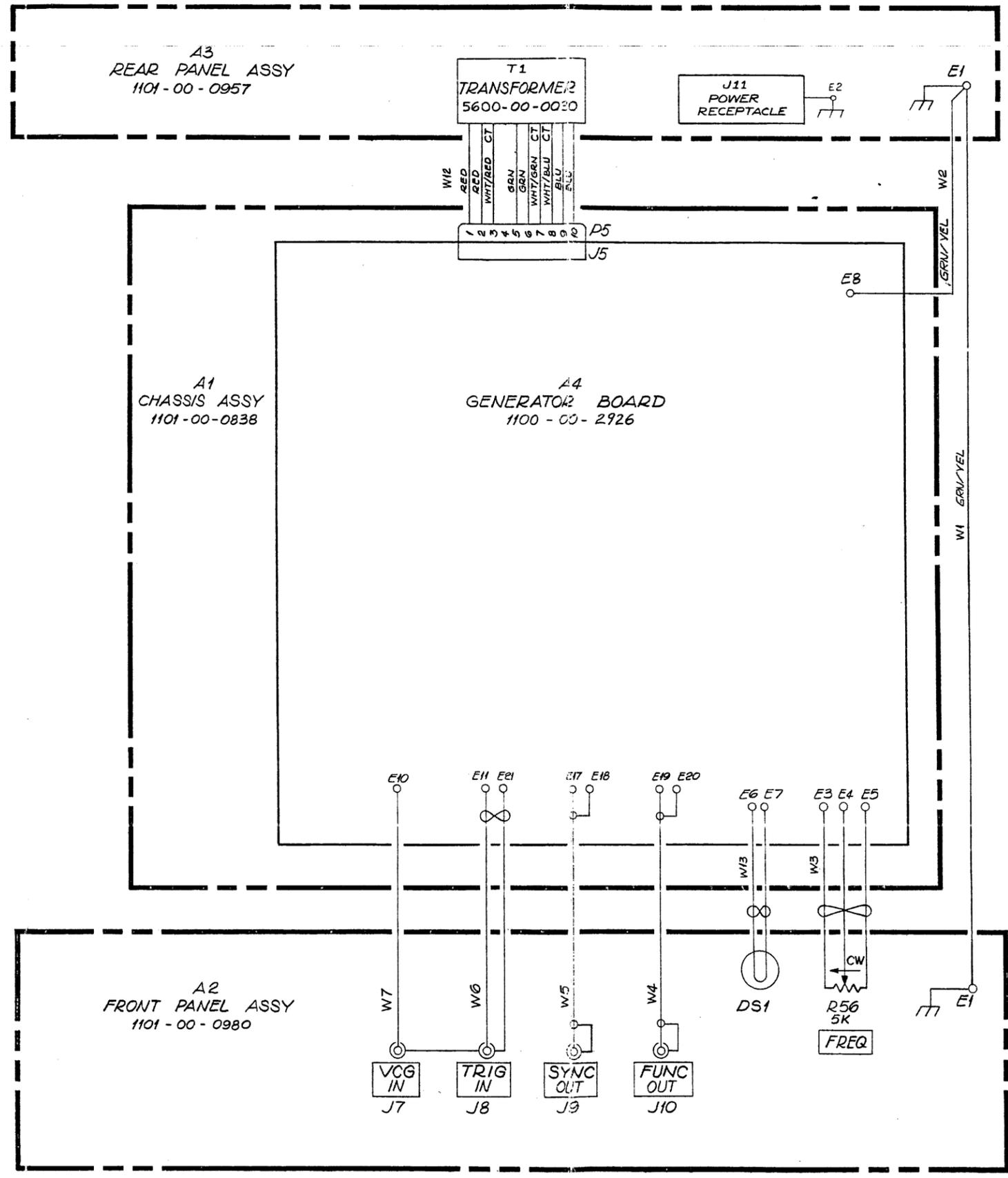
NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

| DRAWING | DRAWING NUMBER |
|-----------------------------------|----------------|
| Instrument Schematic | 0004-00-0167 |
| Chassis Assembly | 0102-00-0838 |
| Chassis Parts List | 1101-00-0838 |
| Generator Board Schematic | 0103-00-2926 |
| Generator Board Assembly | 1100-00-2926 |
| Generator Board Assembly | 0101-00-2926 |
| Generator Board Parts List | 1100-00-2926 |
| Generator Board Switch Detent | 0102-00-0958 |
| Generator Board Switch Parts List | 1202-00-0958 |
| Subassembly Mounting Angle | 0102-00-1024 |
| Subassembly Parts List | 1206-00-1024 |
| Rear Panel Assembly | 0102-00-0957 |
| Rear Panel Parts List | 1101-00-0957 |
| Front Panel Assembly | 0102-00-0980 |
| Front Panel Parts List | 1101-00-0980 |

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|-----|------|----|----------|--------|
| A | 4392 | | 10/21/82 | A.R.T. |



NOTE: UNLESS OTHERWISE SPECIFIED

| | | | |
|--|------------------|---|---------------------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: FN AQUINO | DATE: 11/3/81 | WAVETEK SAN DIEGO • CALIFORNIA |
| MATERIAL | PROJ ENGR: Ruck | DATE: 9/21/82 | |
| FINISH WAVETEK PROCESS | RELEASE APPROV: | TOLERANCE UNLESS OTHERWISE SPECIFIED: .XXX ± 0.10 ANGLES: 1° .XX ± 0.20 | TITLE: SCHEMATIC INSTRUMENT |
| | DO NOT SCALE DWG | SCALE | MODEL NO: 190 |
| | | | DWG NO: 0004-00-0167 |
| | | | REV: 1A |
| | | | CODE IDENT: 23338 |
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|-----|------------|-------------|---------|--------|
| A | 4633 | J. Cooper | 1/2/82 | Q.E.T. |
| B | 8043 | J.C. Cooper | 3/2/82 | H.N. |
| C | ECO # 9223 | J.C. Cooper | 10/2/82 | A.R.T. |

INSTALL TOP AND BOTTOM COVERS USING NO. 8-32x 2" PAN HEAD SCREW (4 PLCS.)

REAR PANEL (A3)
(REF. P/N: 1101-00-0957)

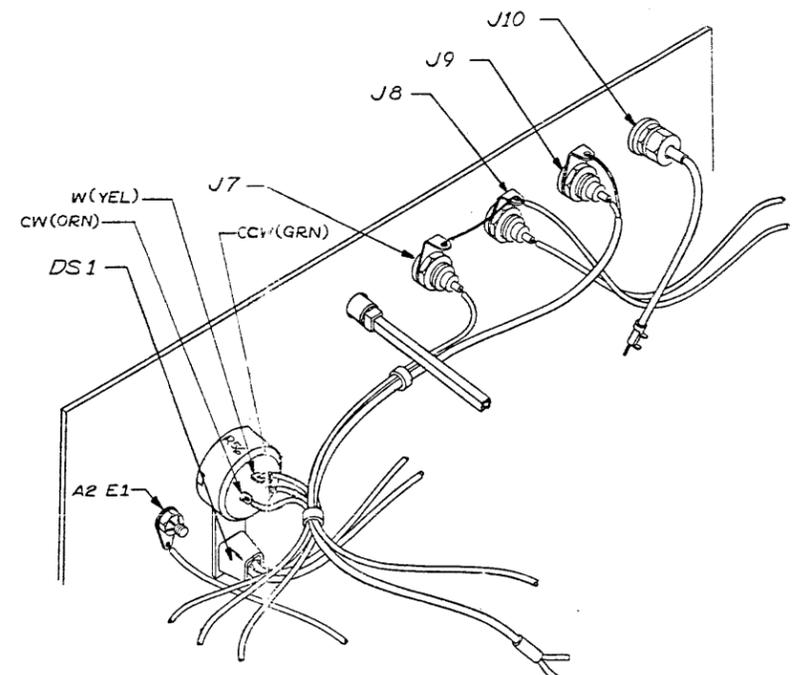
APPLY THERMAL COMPOUND (TYP 2 PLCS)

| CHASSIS ASSEMBLY WIRE & CABLE HOOK-UP | | | |
|---------------------------------------|--------------------|-----------------------|---------|
| REF DES | FROM | TO | COLOR |
| W1 | REAR PANEL - A3 E1 | FRONT PANEL - A2 E1 | GRN/YEL |
| W2 | REAR PANEL - A3 E1 | FRONT PANEL - A4 E8 | GRN/YEL |
| W3 | GEN BD - E3 | FRONT PANEL - R56-CW | ORN |
| | GEN BD - E4 | FRONT PANEL - R56-W | YEL |
| | GEN BD - E5 | FRONT PANEL - R56-CCW | GRN |
| W4 | GEN BD - E19 | FRONT PANEL - J10 | BLK |
| | GEN BD - E20 | FRONT PANEL - J10 | BLK |
| W5 | GEN BD - E17 | FRONT PANEL - J9 | BLK |
| | GEN BD - E18 | FRONT PANEL - J9 | BLK |
| W6 | GEN BD - E11 | FRONT PANEL - J8 | WHT/BRN |
| | GEN BD - E21 | FRONT PANEL - J8 | BLK |
| W7 | GEN BD - E10 | FRONT PANEL - J7 | WHT/BLK |
| W12 | REAR PANEL - A3 | GEN BD - J5 | N/A |
| W13 | GEN BD - A4 E6 | FRONT PANEL - DS1 | N/A |
| | GEN BD - A4 E7 | FRONT PANEL - DS1 | N/A |

NO. 4-40x 3/8" PAN HEAD SELF LOCKING SCREW WITH FLAT WASHER (4 PLCS.)

GENERATOR BD (A4)
(REF. P/N 1100-00-0834)
ATTACH TO SHIELD PLATE AND FRONT PANEL ASSY USING #4-40x1/4" SELF LOCKING SCREWS (10 REQ'D)

FRONT PANEL WIRING AND ROUTING



FRONT PANEL (A2)
(REF. P/N 1101-00-0980)

AFTER INSTALLATION OF FRONT AND REAR FEET, APPLY (1) DROP OF LOCTITE #14 (OR EQUIV.) TO SCREW THREADS (6). ALLOW 1 HR. MIN. TO DRY WITH FEET UP.

1. SEE PARTS LIST NO: 1101-00-0838.

NOTE: UNLESS OTHERWISE SPECIFIED

| | | | | |
|--|--|----------------|--------------------------------|----------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN D. COOPER | DATE 1/5/82 | WAVETEK SAN DIEGO • CALIFORNIA | |
| MATERIAL | PROJ ENGR <i>Kevin To</i> | RELEASE APPROV | TITLE ASSEMBLY CHASSIS (A1) | |
| FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED .XX ± .010 ANGLES 1:1 XX ± .030 | | MODEL NO 190 | DWG NO. 0102-00-0838 |
| SCALE | DO NOT SCALE DWG | SCALE | REV C | REV C |
| CODE IDENT 23338 | SHEET 1 OF 1 | | | |

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|-----|-----|----|------|-----|
|-----|-----|----|------|-----|

D

C

B

A

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|-----------------------|-----------------------|-------------------|-------|--------------|--------|
| NONE | ASSY DRWG. CHASSIS | 0102-00-0838 | WVTK | 0102-00-0838 | 1 |
| 1 | SPK ASSY. POWER ROD | 190-0956 | WVTK | 1206-00-0956 | 1 |
| NONE | CHASSIS CABLE KIT | 190-0959 | WVTK | 1207-00-0959 | 1 |
| NONE | PLATE, NAME | 139-305 | WVTK | 1400-00-2180 | 1 |
| NONE | COVER, TOP | 180-300-1 | WVTK | 1400-00-5000 | 1 |
| NONE | COVER, BOTTOM | 180-300-2 | WVTK | 1400-00-5030 | 1 |
| 2 | SHIELD PLATE | 170-3843 | WVTK | 14J0-01-3843 | 1 |
| 6 | COAX KNOB SET | RB-67-1-SB+0-H-9 | ROGAN | 2400-01-0009 | 3 |
| 7 | KNOB, SMALL | O-K-O | ROGAN | 2170-01-0010 | 1 |
| NONE | BAIL ASSY W/PT | 180-500 | WVTK | 2800-08-0010 | 1 |
| NONE | SPEEDNUT, SELF RETAIN | C7494-632-4 | TINN | 2800-09-0003 | 6 |

| | | | |
|------------------------------|------------------------|------------------------------|----------|
| WAVETEK PARTS LIST | TITLE ASSY, CHASSIS | ASSEMBLY NO. 1101-00-0938 | REV A |
| | PAGE 1 | | |

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| | | | | |
|--|--|------|---------------------------------------|-------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO • CALIFORNIA | |
| MATERIAL | PROJ ENGR | | TITLE | |
| | RELEASE APPROV | | PARTS LIST ASSY, CHASSIS | |
| FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 0.10 ANGLES ± 1 XX ± 0.30 | | MODEL NO | REV |
| SCALE | DO NOT SCALE DWG | | 190 | 1101-00-0838 A |
| | | | CORP DIN: 23338 | SHEET 1 OF 1 |

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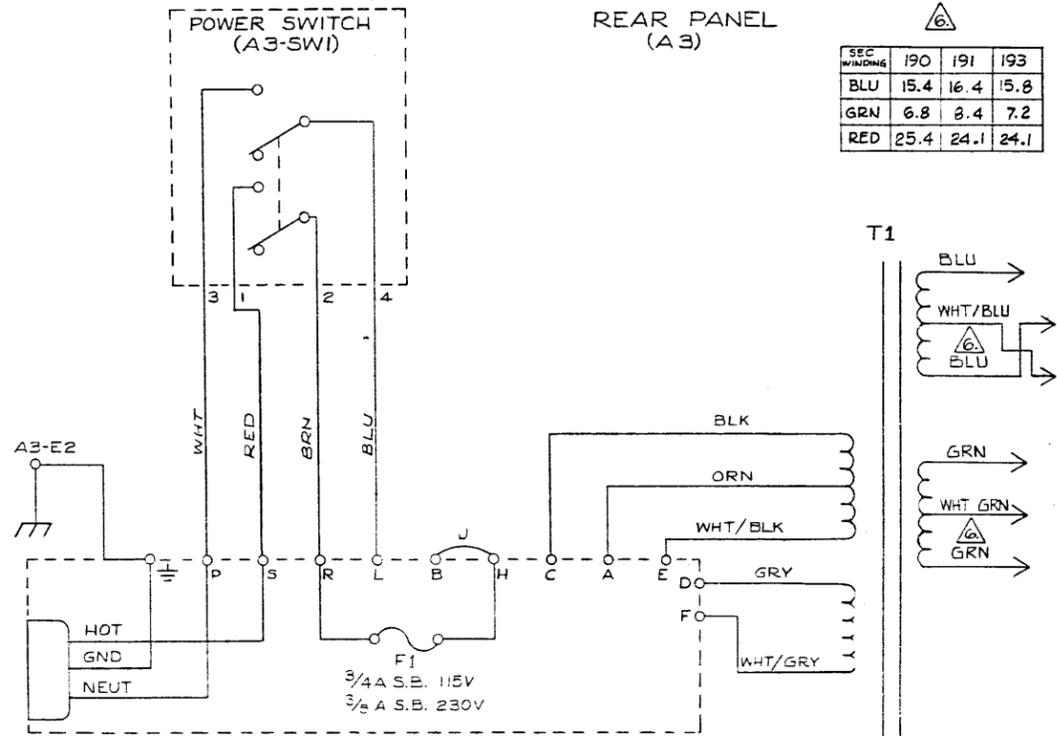
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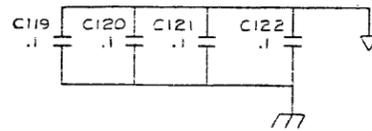
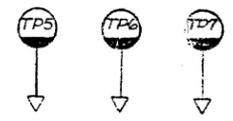
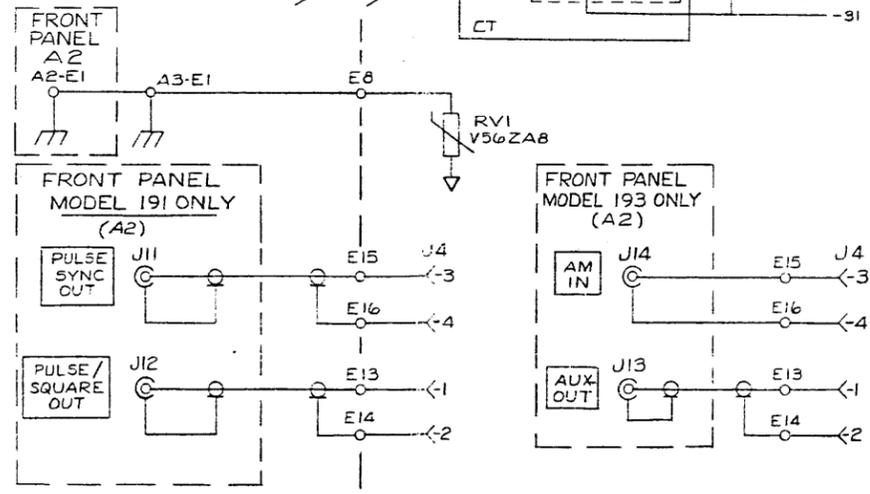
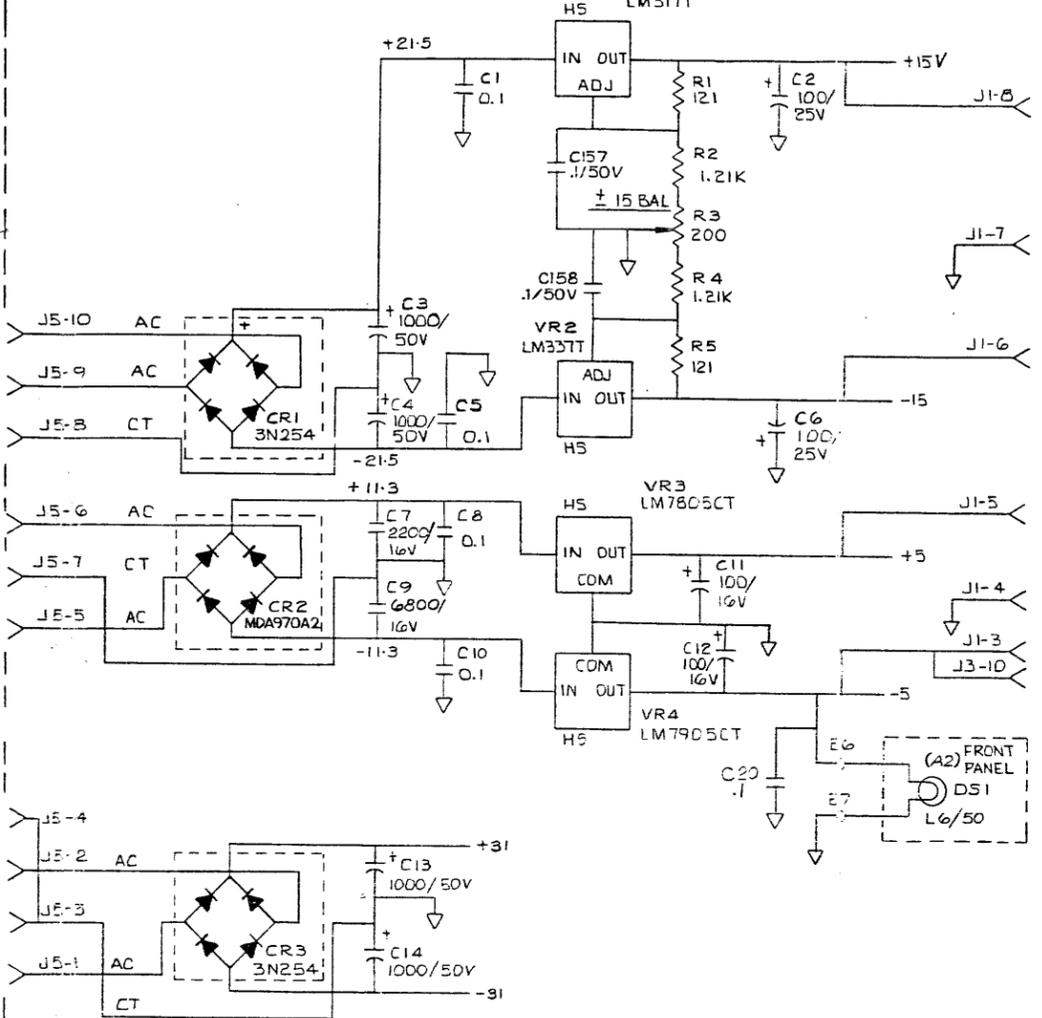
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|-----|-----------|----|----------|-------|
| A | ECN #4633 | JT | 8/26/81 | ALF T |
| B | #8A-474 | BG | 12/29/81 | RA |

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| SEC WINDING | 190 | 191 | 193 |
|-------------|------|------|------|
| BLU | 15.4 | 16.4 | 15.8 |
| GRN | 6.8 | 8.4 | 7.2 |
| RED | 25.4 | 24.1 | 24.1 |

POWER SUPPLY

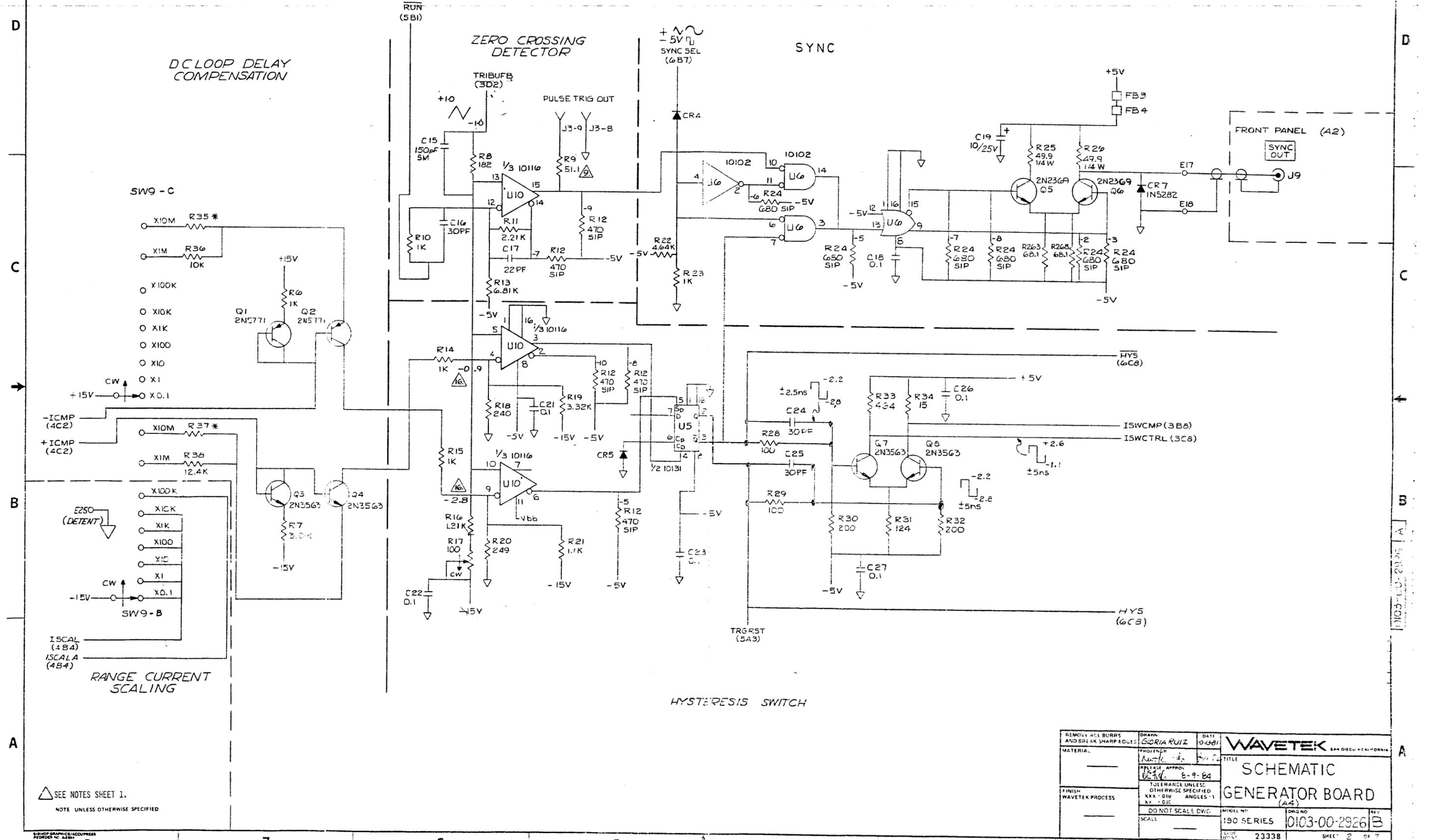


- 17. *NOMINAL VALUE-CALLED OUT ON PARTS LIST.
- 16. VOLTAGES VALID THRU X 100K ONLY (2 PLCS).
- 14. USED ON 192 ONLY.
- 13. NOT USED ON 193
- 12. NOT USED ON 191
- 11. NOT USED ON MODEL 192 (3 PLCS).
- 10. MODEL 193 ONLY (5 PLCS)
- 9. MODEL 191 ONLY (10 PLCS)
- 8. SELECTED 2N3866 FOR V_{CEO} .40V (3 PLCS)
- 7. P/N 4807-02-0777 (MATCHED PAIR FD777)
- 6. VOLTS AC WITH: V_{LINE} RMS = 115, CORCOM TAB = 120
- 5. SIP'S ARE: R12 = 470, R24 = 680, R124 = 680.
- 4. ALL DIODES ARE FD6666
- 3. ALL CAPACITORS ARE IN MICROFARADS.
- 2. ALL RESISTORS ARE 1/8W AND ARE IN OHMS.
- 1. PARTIAL REFERENCE DESIGNATORS SHOWN, USE ASSEMBLY REF. DES. PREFIX A4 (EXAMPLE A4R1)

NOTE UNLESS OTHERWISE SPECIFIED

| | | | | |
|--|--|--|--|---------------------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | | DRAWN: GIORIA KLIZ | DATE: 8/13/81 | |
| MATERIAL | | PROJENGR: [Signature] | DATE: [Signature] | |
| FINISH: WAVETEK PROCESS | | RELEASE APPROV: [Signature] | DATE: 3-4-84 | SCHEMATIC GENERATOR BOARD (A4) |
| | | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 010 ANGLES - 1 XX - 030 | DO NOT SCALE DWG | |
| | | SCALE | MODEL NO: 190 SERIES DWG NO: 0103-00-2926 | |
| | | EGG: 23338 | SHEET: 1 | PL: B |

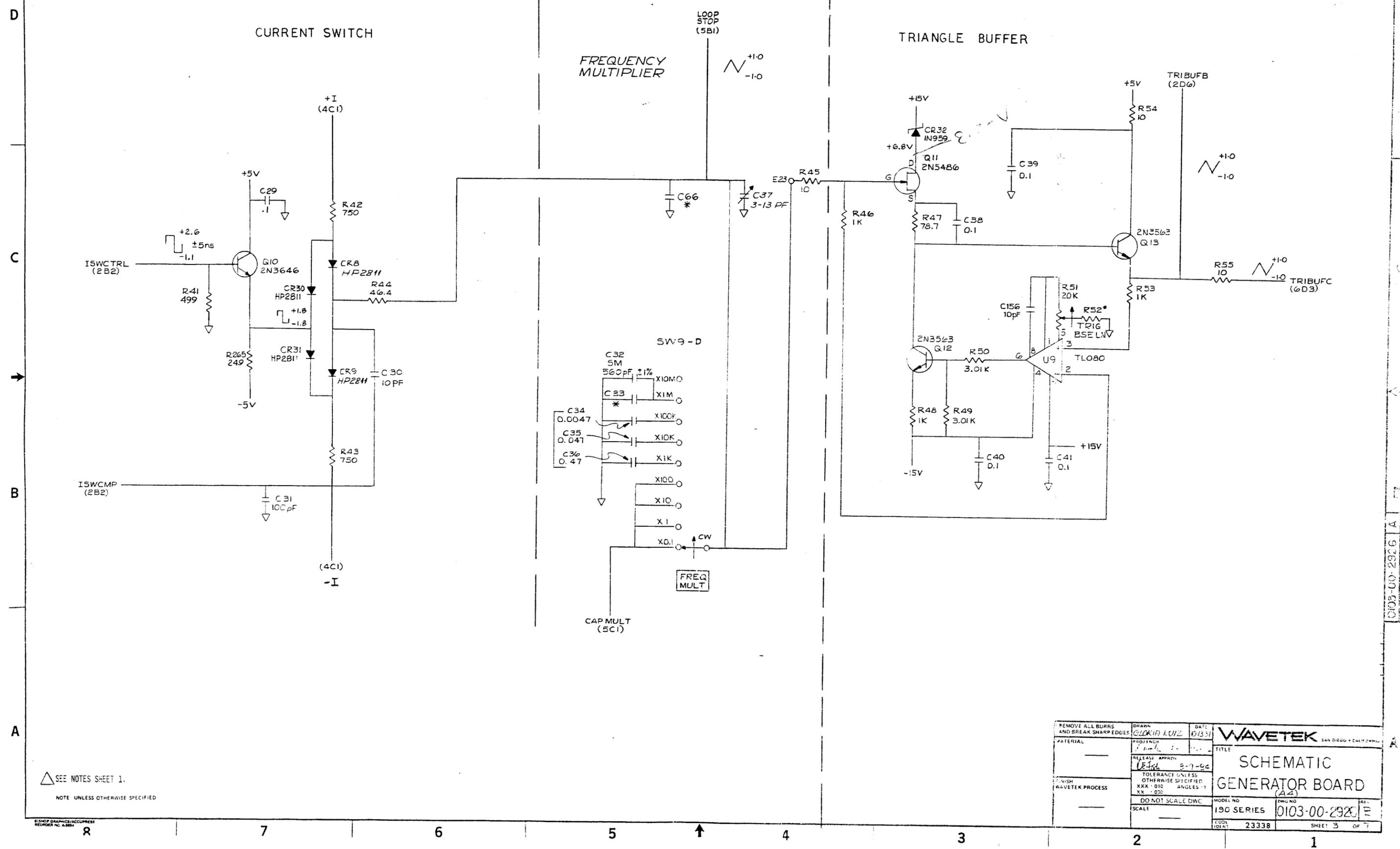
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SEE NOTES SHEET 1.
NOTE UNLESS OTHERWISE SPECIFIED

| | | | |
|--|--|-------------------|----------------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: GORJA RUIZ | DATE: 10-1981 | WAVETEK SAN DIEGO, CALIFORNIA |
| MATERIAL: | PROLENGTH: | REV: 1 | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV: [Signature] | DATE: 8-9-84 | TITLE: SCHEMATIC GENERATOR BOARD |
| | TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX: 010 ANGLES: 1 X: 0.01 | DO NOT SCALE DRG. | MODEL NO: 190 SERIES |
| | SCALE: | | DWG NO: 0103-00-2926 |
| | | | REV: 1 |
| | | | 23338 SHEET 2 OF 7 |

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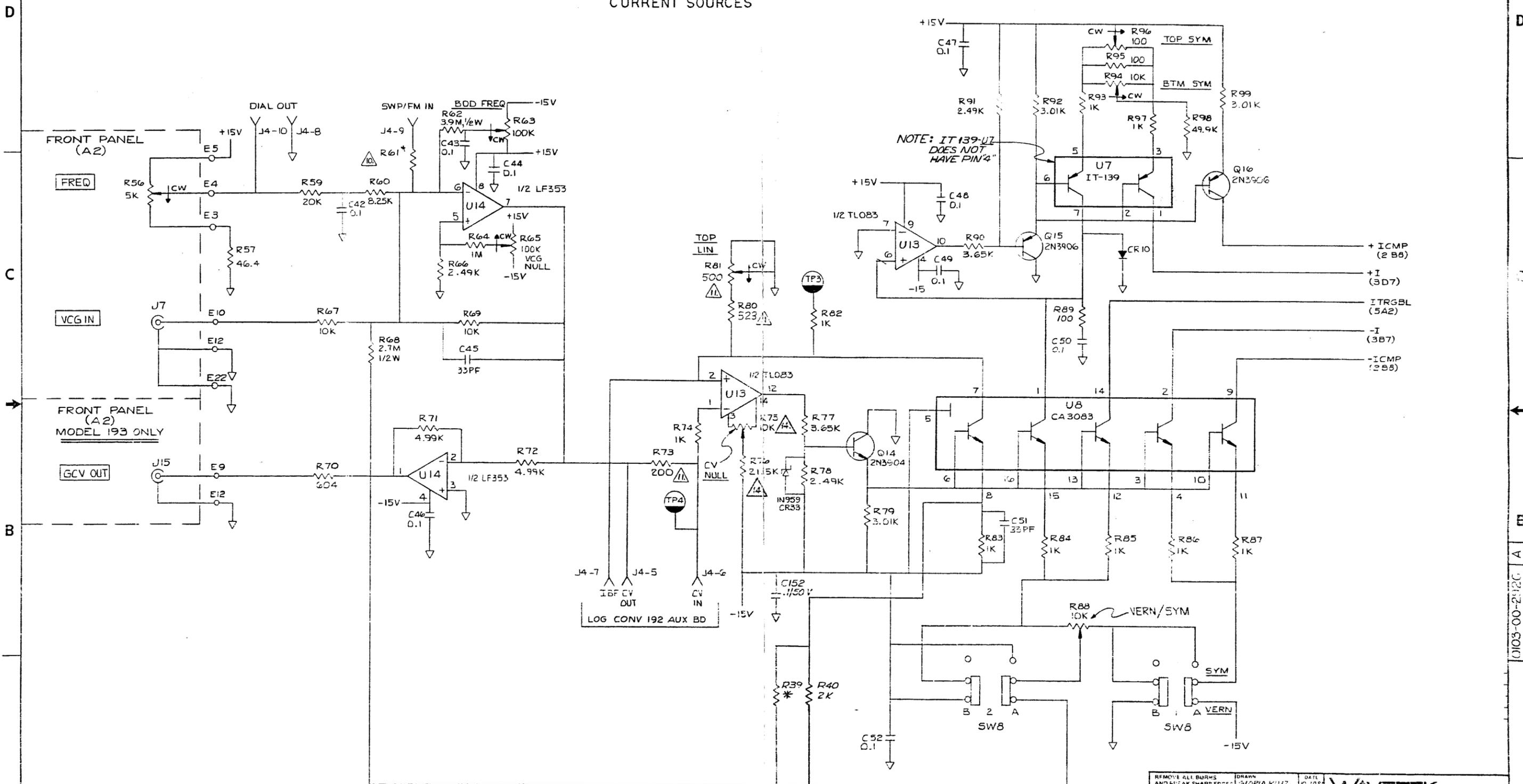


SEE NOTES SHEET 1.
NOTE: UNLESS OTHERWISE SPECIFIED

| | | | |
|--|---|------------------|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: G. L. LUIZ | DATE: 10/13/81 | WAVETEK SAN DIEGO, CALIF. 92161 |
| MATERIAL: | PROFILING: | TITLE: | |
| | RELEASE APPROV: [Signature] | DATE: 9-7-84 | SCHEMATIC GENERATOR BOARD |
| | TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX - 010 ANGLES - 1 XX - 030 | DO NOT SCALE DWG | |
| SCALE: | MODEL NO: | FIG NO: | REV: |
| | 19G SERIES | 0103-00-2926 | A |
| | CODE (LOCAL): 23338 | SHEET 3 OF 7 | |

0103-00-2926 A

CURRENT SOURCES



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SEE NOTES SHEET 1.
NOTE: UNLESS OTHERWISE SPECIFIED

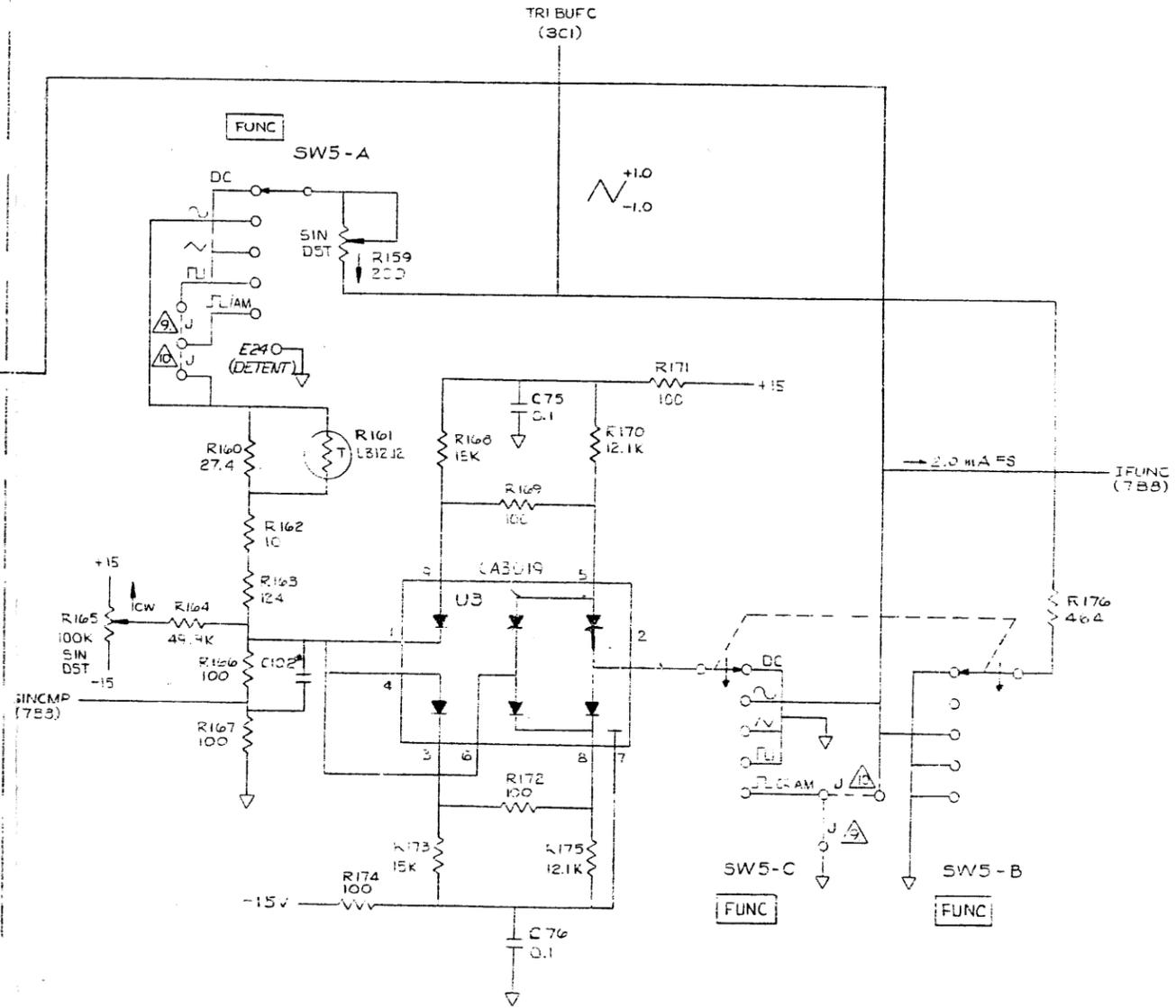
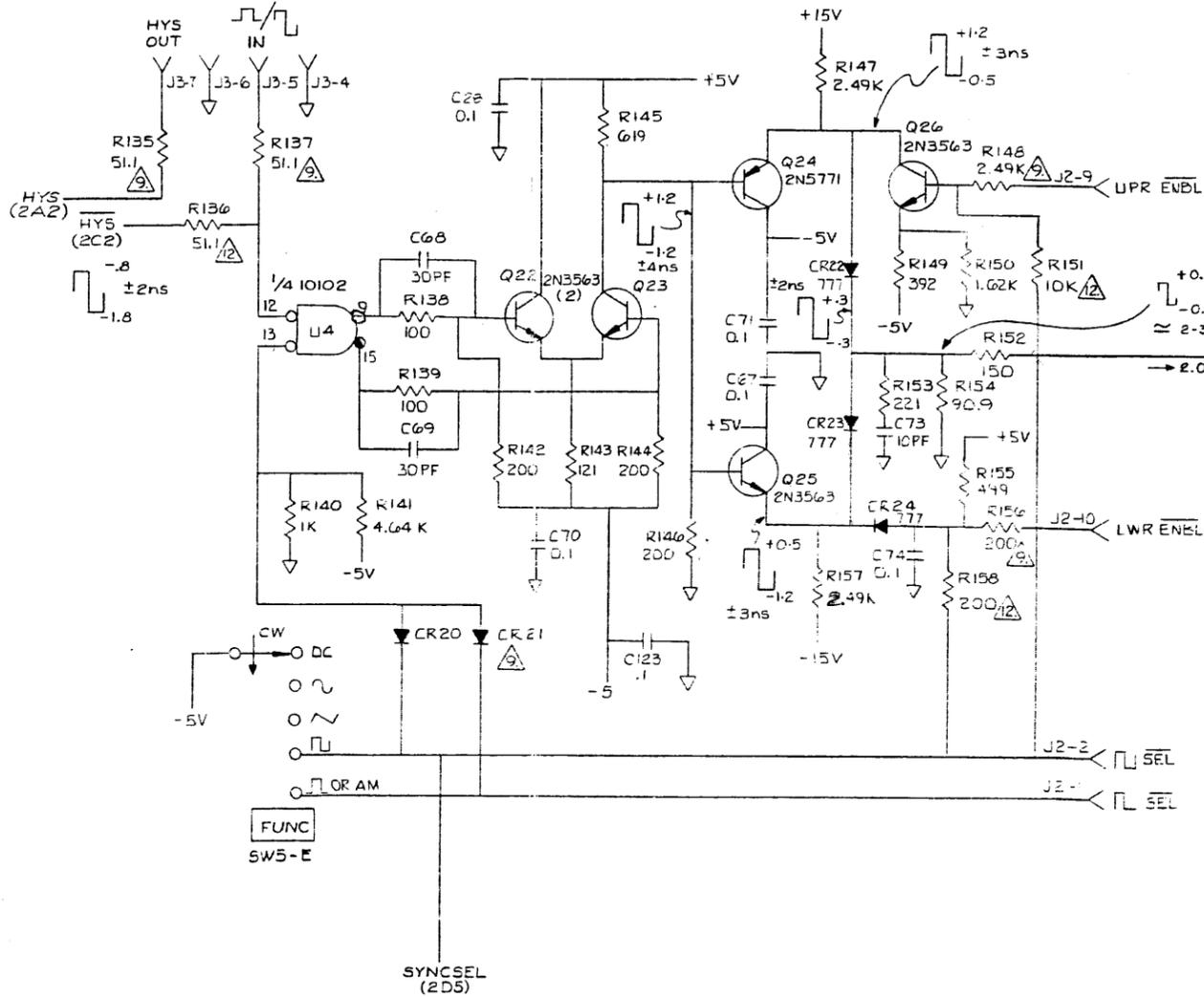
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|--|--|--|----------------------|---------------------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | | DRAWN: GLORIA KUIZ | DATE: 10-1988 | WAVETEK SAN DIEGO • CALIFORNIA |
| MATERIAL | | PROJECT: KUIZ | DATE: 8-4-84 | |
| FINISH: WAVETEK PROCESS | | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 010 ANGLES - 1 XX - 030 | | SCHEMATIC GENERATOR BOARD (A4) |
| SCALE | | DO NOT SCALE DWG | MODEL NO: 190 SERIES | |
| | | 23338 | 0103-00-2925 | REV: B |

0103-00-2925 A

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SQUARE SHAPER

SINE CONVERTER



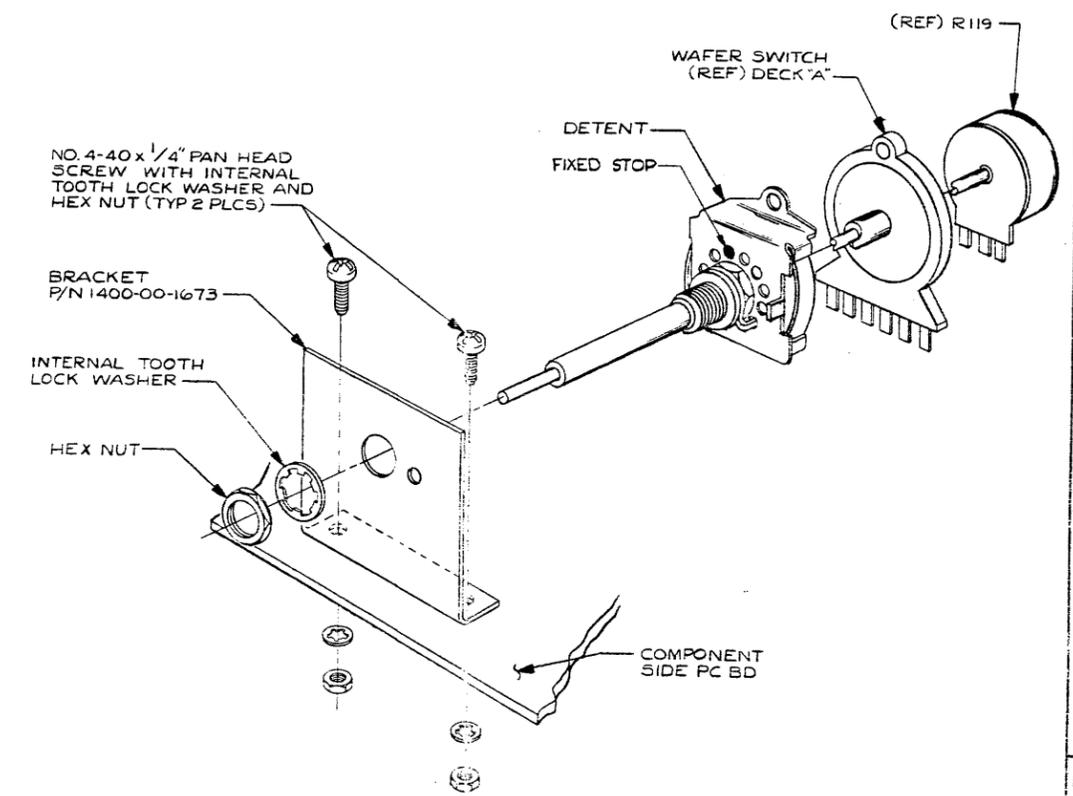
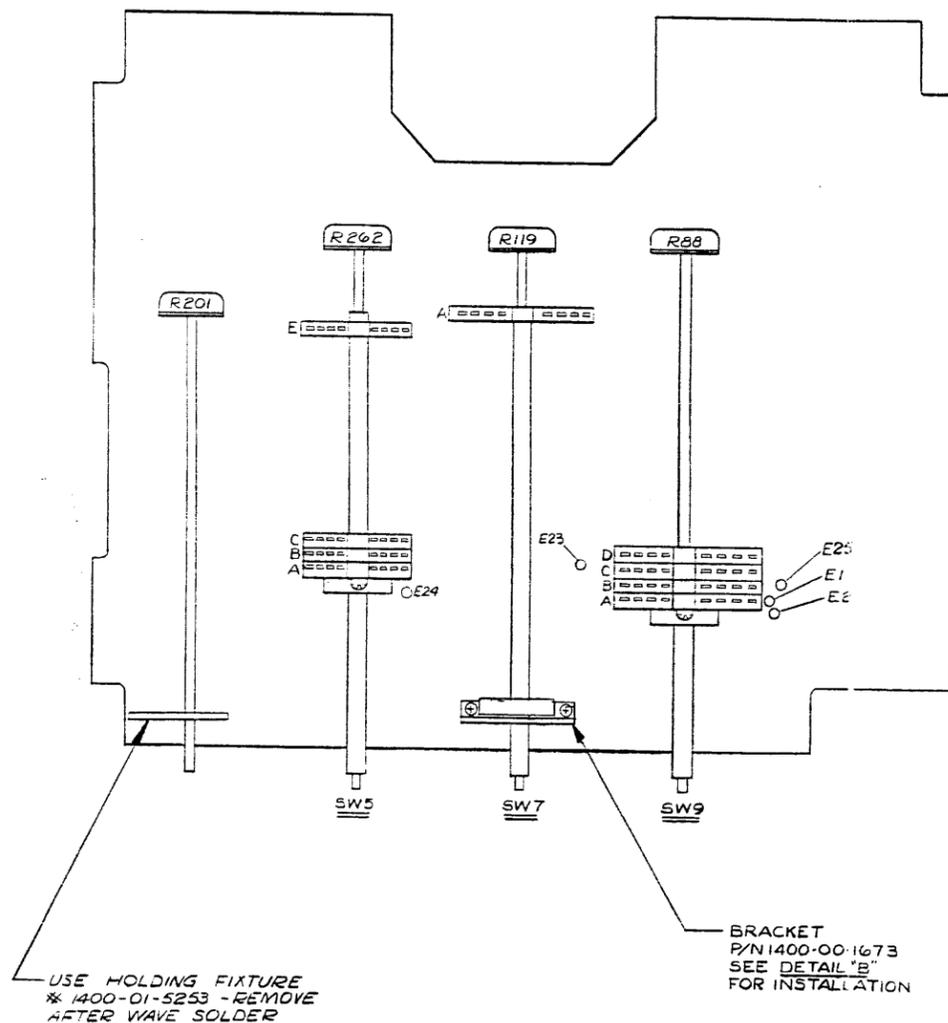
SEE NOTES SHEET 1.
NOTE: UNLESS OTHERWISE SPECIFIED

| | | | |
|--|----------------------|----------------------|---------------------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: GORAKUJ | DATE: 10-23-81 | WAVETEK SAN DIEGO • CALIFORNIA |
| MATERIAL | PROJECT: 1154 | REV: 1 | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV: 1154 | DATE: 8-9-84 | TITLE: SCHEMATIC GENERATOR BOARD |
| | DO NOT SCALE DWG | MODEL NO: 190 SERIES | REV: (24) |
| | SCALE | DWG NO: 0103-00-2926 | REV: B |
| | | ISSUE NO: 23338 | SHEET 6 OF 7 |

0103-00-2926 A

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| REV | ECN | BY | DATE | APP |
|-----|-----|----|------|-----|
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NOTE UNLESS OTHERWISE SPECIFIED

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|--|------------------------------------|---|---------------------------------------|--------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: CHERMACK | DATE: 11/7/61 | WAVETEK SAN DIEGO • CALIFORNIA | |
| MATERIAL: --- | PROJENGR: <i>Chermack</i> | DATE: <i>8-9-64</i> | TITLE: ASSEMBLY GENERATOR BOARD (A4) | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV: <i>[Signature]</i> | TOLERANCE UNLESS OTHERWISE SPECIFIED: .XXX ± .010 ANGLES: 1:1 | SCALE: NONE | REV: B |
| | | DO NOT SCALE DWG | DWG NO: 0101-00-2926 | |
| | | | SCALE: 190 | |
| | | | REV: 23338 | |

0101-00-2926

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Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DRG-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Includes parts like ASSY DRAWING, SCHEMATIC, SPK ASSY, BOARD MNTG BRACKET, etc.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DRG-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Includes parts like ASSY DRAWING, ASSY, PC BD PREPPED, CAP, CER DISK, 5PF, 1KV, 10%, etc.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DRG-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Includes parts like CAP, MYLAR, 0047MF, 50V, CAP, MYLAR, 047MF, 50V, etc.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DRG-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Includes parts like STANDOFF, SMAGE, 187L, 250DIA, 4-40, KNURL, HEATSINK, etc.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DRG-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Includes parts like CAP, CER, 22PF, 1KV, CAP, CER, 220PF, 1KV, etc.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DRG-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Includes parts like RES, C, 1/2W, 5%, 2.7M, RES, C, 1/2W, 5%, 3.9M, etc.

WAVETEK SAN DIEGO - CALIFORNIA. PARTS LIST PCA, GENERATOR. Includes fields for DRAWN, DATE, PROJ/ENGR, RELEASE APPROV, TOLERANCE UNLESS OTHERWISE SPECIFIED, DO NOT SCALE DWG, SCALE, DWG NO, and SHEET 1 OF 5.

NOTE UNLESS OTHERWISE SPECIFIED

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REV ECN BY DATE APP

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Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DR10-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Rows include R38, R231 R262, R152, R114 R117, R168 R173, R202 R34, R150, R267, RB, R142 R144 R146 R158 R210 R214 R243 R249 R30 R32 R73, R223 R35T R40, R257 R59, R188, R191 R193, R126 R153, R11 R37T R39T.

Summary table for page 5: WAVETEK PARTS LIST, TITLE: ASSY. KIT PREWAVE LOAD 190-0834, ASSEMBLY NO. 1208-00-2927, REV A, PAGE 5.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DR10-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Rows include R131 R141 R22, R44 R57, R120 R129 R155 R181 R207 R250 R41, R100 R105 R178 R189 R71 R72, R164 R98, R128 R136 R197, RB0, R208 R244, R70, R145 R209 R242, R240 R266, R115 R116 R122 R123, R13, R263 R268, R179 R195 R261 R42 R43, R246 R47.

Summary table for page 7: WAVETEK PARTS LIST, TITLE: ASSY. KIT PREWAVE LOAD 190-0834, ASSEMBLY NO. 1208-00-2927, REV A, PAGE 7.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DR10-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Rows include CR32 CR33, CR7, CR1 CR3, CR22 CR23 CR24, CR10 CR11 CR12 CR13 CR14 CR16 CR20 CR25 CR26 CR4 CR5, CR30 CR31 CR8 CR9, CR18 19, CR2, RV1, Q34, Q5 Q6.

Summary table for page 9: WAVETEK PARTS LIST, TITLE: ASSY. KIT PREWAVE LOAD 190-0834, ASSEMBLY NO. 1208-00-2927, REV A, PAGE 9.

C

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DR10-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Rows include R18, R20 R232 R233 R234 R265, R147 R157 R215 R225 R66 R78 R91, R107, R177, R160, R194, R118 R183 R49 R50 R7 R79 R92 R99, R186, R212, R259, R19, R77 R90, R132 R149, R176 R33.

Summary table for page 6: WAVETEK PARTS LIST, TITLE: ASSY. KIT PREWAVE LOAD 190-0834, ASSEMBLY NO. 1208-00-2927, REV A, PAGE 6.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DR10-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Rows include R60, R101, R108, R154, R217 R219 R227, R25 R26, R184, R235 R236, R224, R237 R238 R239 R241, R12, R124 R24, R112, CR29, CR27 CR28.

Summary table for page 8: WAVETEK PARTS LIST, TITLE: ASSY. KIT PREWAVE LOAD 190-0834, ASSEMBLY NO. 1208-00-2927, REV A, PAGE 8.

Table with 6 columns: REFERENCE DESIGNATORS, PART DESCRIPTION, DR10-MFGR-PART-NO, MFGR, WAVETEK NO., QTY/PT. Rows include Q35, Q12 Q13 Q17 Q18 Q19 Q22 Q23 Q25 Q26 Q28 Q3 Q30 Q32 Q4 Q7 Q8, Q10, Q29, Q14, Q15 Q16 Q20 Q21, Q36, Q11, Q1 Q2 Q24 Q27 Q31 Q33, U7, Q39, U9, U11 U13.

Summary table for page 10: WAVETEK PARTS LIST, TITLE: ASSY. KIT PREWAVE LOAD 190-0834, ASSEMBLY NO. 1208-00-2927, REV A, PAGE 10.

A

NOTE: UNLESS OTHERWISE SPECIFIED

WAVETEK SAN DIEGO CALIFORNIA PARTS LIST PCA, GENERATOR. Includes fields for DRAWN, DATE, TOLERANCE, FINISH, SCALE, MODEL NO. 190, DWG NO. 1100-00-2926, REV B, CODE 23338, SHEET 2 OF 3.

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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|-----------------------|--|-------------------|------|--------------|--------|
| U14 | OP AMP. WIDE BANDWIDTH DUAL JFET INPUT | LF353N | NSC | 7000-03-3300 | 1 |
| U2 | OP-AMP | LF356N | NSC | 7000-03-3600 | 1 |
| U3 | DIODE, ULTRA FAST, LOW CAPACITANCE | CA-3019 | RCA | 7000-30-1900 | 1 |
| U8 | TRANS ARRAY, GENERAL PURPOSE, NPN | CA3083 | FAIR | 7000-30-8300 | 1 |
| U1 | TRANS ARRAY, HIGH FREQ. NPN | CA3127E | RCA | 7000-31-2700 | 1 |
| U4 U6 | GATE, NDR, QUAD 2 INP, ECL | MC10102 | MOT | 8001-01-0200 | 2 |
| U10 U12 | RCVR, TR: LINE, ECL | MC10116P | MOT | 8001-01-1600 | 2 |
| U5 | FLIP-FLOP DUAL, ECL | MC10131 | MOT | 8001-01-3100 | 1 |

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|---------------------------|---|------------------------------|----------|
| WAVETEK PARTS LIST | TITLE ASSY, KIT PREWAVE LOAD 190-0834 | ASSEMBLY NO. 1208-00-2927 | REV A |
| PAGE 11 | | | |

NOTE: UNLESS OTHERWISE SPECIFIED

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|--|----------------|------|---|--------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO • CALIFORNIA | |
| MATERIAL | CHECKED | | | |
| FINISH WAVETEK PROCESS | PROJ ENGR | | TITLE PARTS LIST PCA, GENERATOR | |
| | RELEASE APPROV | | | |
| UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES | | | SIZE D | FSCW NO. 23338 |
| DO NOT SCALE DRAWING | | | DWG. NO. 1100-00-2926 | REV B |
| | | | SCALE MODEL 190 | SHEET 3 OF 3 |

| REV | ECN | BY | DATE | APP |
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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO | QTY/PT |
|-----------------------|-------------------------------------|-------------------|------|--------------|--------|
| NONE | ASSY DRWG. GENERATOR SWITCHES | 0102-00-0958 | WVTK | 0102-00-0958 | 1 |
| NONE | BRKT | 133-305 | WVTK | 1400-00-1673 | 1 |
| 1 | PLATE, SW | 008-004 | WVTK | 1400-00-2130 | 2 |
| R119 R262 R88 | POT. CONT. 10K FROM 4600-01-0312 | 4609-71-0319 | WVTK | 4609-71-0319 | 3 |
| 2 | WAFER | 133-SW1-1 | WVTK | 5104-02-0008 | 4 |
| 7 | WAFER | 147-400 | WVTK | 5104-02-0015 | 5 |
| 3 | SWITCH STOP | 211-33-001 | CTS | 5104-07-0001 | 3 |
| 4 | SWITCH STOP | 212-33-006 | CTS | 5104-07-0002 | 3 |
| 5 | DETENT, MOD FROM: 5104-01-0010 | 5104-99-0062 | WVTK | 5104-99-0062 | 1 |
| 6 | DETENT, MOD FROM: 5104-01-0010 | 5104-99-0063 | WVTK | 5104-99-0063 | 1 |
| 8 | DETENT, MOD FROM: 5104-01-0010 | 5104-99-0064 | WVTK | 5104-99-0064 | 1 |

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|------------------------------|-----------------------------------|-----------------------------|-----|
| WAVETEK PARTS LIST | TITLE ASSY. SWTCH SWS 190-0958 | ASSEMBLY NO 1202-00-0958 | REV |
| | PAGE 1 | | |

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|--|--|--|---------------------------------------|--|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO • CALIFORNIA | |
| MATERIAL | PROJ/ENGR | | | |
| FINISH WAVETEK PROCESS | RELEASE APPROV | TITLE PARTS LIST ASSY. GENERATOR SWITCHES | | |
| | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1 XX : 030 | MODEL NO | REV | |
| | DO NOT SCALE DWG | 190 | 1202-00-0958 | |
| SCALE | | 23338 | SHEET 1 OF 1 | |

NOTE UNLESS OTHERWISE SPECIFIED

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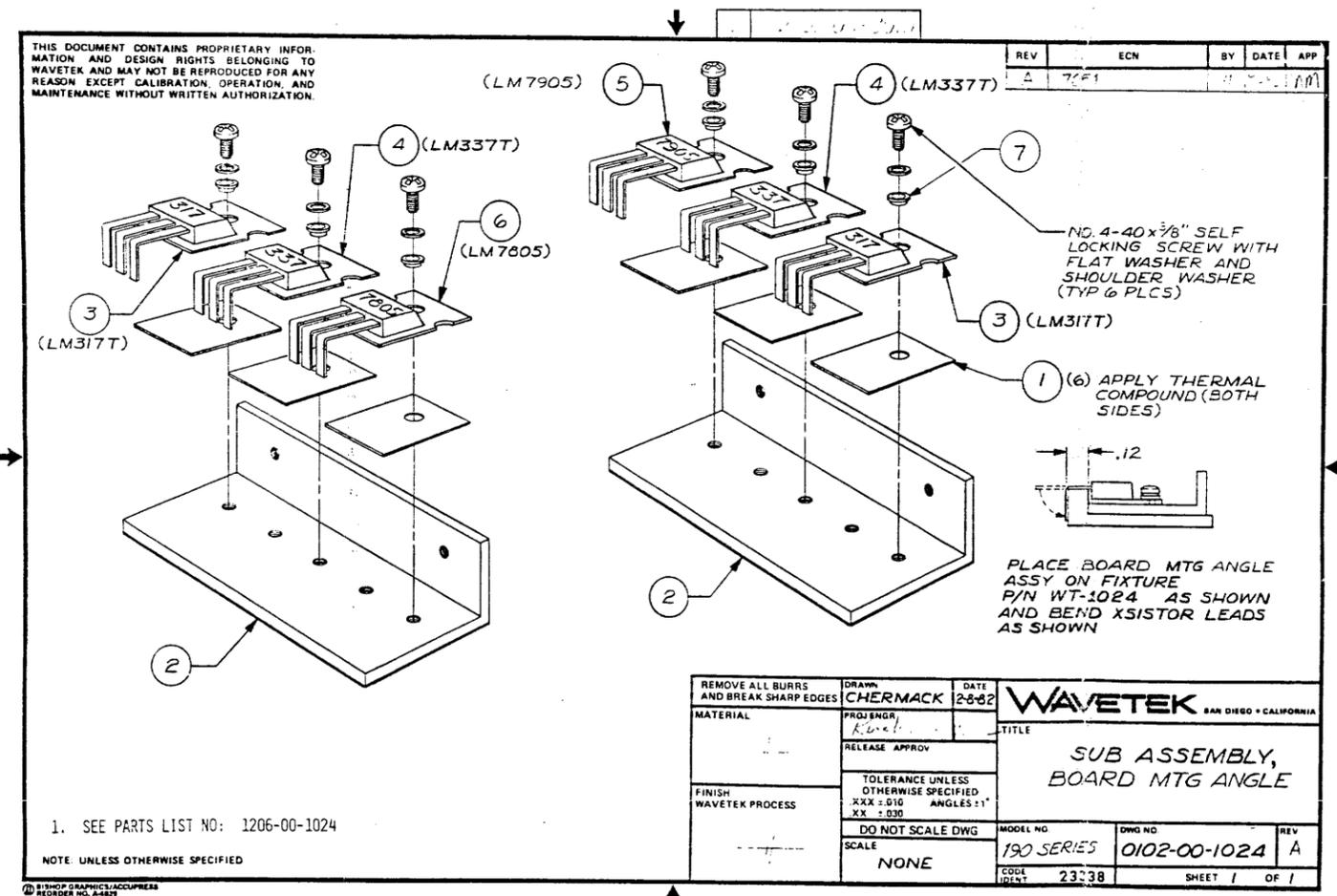
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| REV | ECN | BY | DATE | APP |
|-----|-----|----|------|-----|
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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|-----------------------|----------------------------------|-------------------|-------|--------------|--------|
| NONE | ASSY DRWG, BOARD MNTG ANGLE | 0102-00-1024 | WVTK | 0102-00-1024 | 1 |
| 2 | ANGLE, BOARD MOUNTING | 190-3863 | WVTK | 1400-01-3863 | 2 |
| 7 | WASHER | B51547F015 | HOT | 2800-11-0015 | 6 |
| | SCREW, SELF-LOCK, PH. 4-40 X 3/8 | 4-40 X 3/8 PH. SL | CHRCL | 2800-56-9106 | 6 |
| 1 | INSULATOR, MICA | 64-21-023-106 | ASHVL | 3100-00-0006 | 6 |
| 3 | IC | LM317T | NSC | 7000-03-1700 | 2 |
| 4 | VOLTAGE REGULATOR | LM337T | NAT | 7000-03-3700 | 2 |
| 5 | IC | MC7905CP | HOT | 7000-79-0500 | 1 |
| 6 | VOLY REG | MA7905UC | FAIR | 8000-78-0500 | 1 |

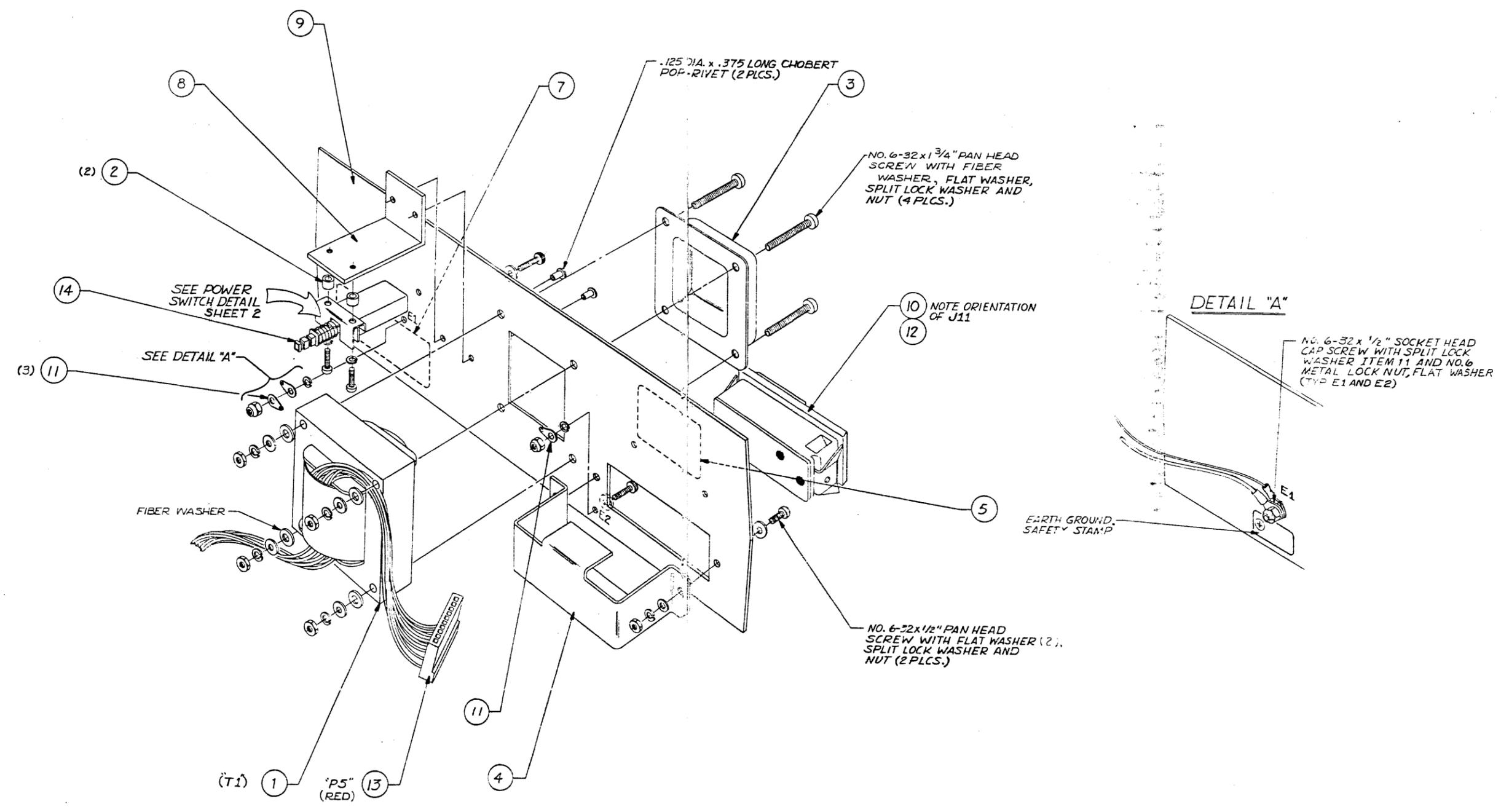
| | | | |
|---------------------------|-----------------------------------|---------------------------|-------|
| WAVETEK PARTS LIST | TITLE: SPK ASSY, BOARD MNTG ANGLE | ASSEMBLY NO. 1206-00-1024 | REV B |
| PAGE 1 | | | |

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|--|---|-------|---------------------------------------|----------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: | DATE: | WAVETEK SAN DIEGO • CALIFORNIA | |
| MATERIAL | PROJ ENGR: | | TITLE: ASSY, BOARD MNTG ANGLE | |
| FINISH: WAVETEK PROCESS | RELEASE APPROV: | | MODEL NO: 190 | DWG NO: 1206-00-1024 |
| | TOLERANCE UNLESS OTHERWISE SPECIFIED: .XXX ± .010 ANGLES ± 1° | | SCALE: NONE | REV: B |
| | DO NOT SCALE DWG | | CODE IDENT: 23338 | SHEET 1 OF 1 |

NOTE: UNLESS OTHERWISE SPECIFIED

| REV | ECN | BY | DATE | APP |
|-----|------|------|----------|--------|
| 4 | 4392 | ART | 5/28/61 | WCT |
| 5 | 6037 | WAM | 11/16/61 | A.R.T. |
| 6 | 8043 | W.C. | 5-18-67 | A.P.T. |

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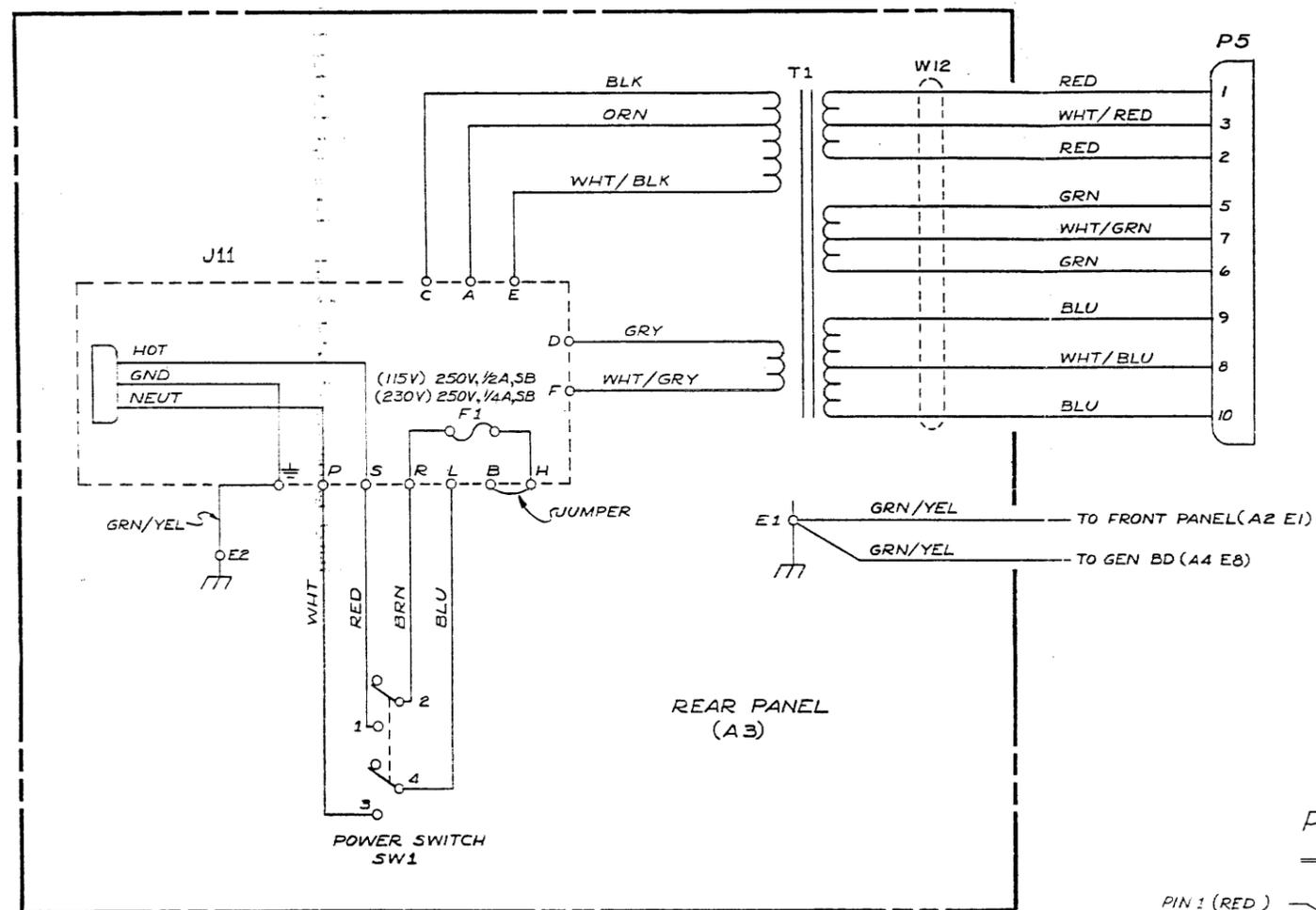


2. THIS SHEET IS INTENDED TO SHOW MECHANICAL ASSEMBLY ONLY - REFERENCE SHEET 2 OF 2 FOR WIRING.
 1. SEE PARTS LIST NO: 1101-00-0957

NOTE: UNLESS OTHERWISE SPECIFIED

| | | | | |
|--|--|-----------------------------|---------------------------------|---------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: D. COOPER | DATE: 12/10/61 | WAVETEK SAN DIEGO - CALIFORNIA | |
| MATERIAL: | PROJ ENGR: [Signature] | RELEASE APPROV: [Signature] | TITLE: ASSEMBLY REAR PANEL (A3) | |
| FINISH: WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES: 1° .XX ±.030 | | DO NOT SCALE DWG | MODEL NO: 190 |
| SCALE: | | SCALE: | DWG NO: 0102-00-0957 | REV: C |
| CODE IDENT: 23338 | | SHEET 1 OF 2 | | |

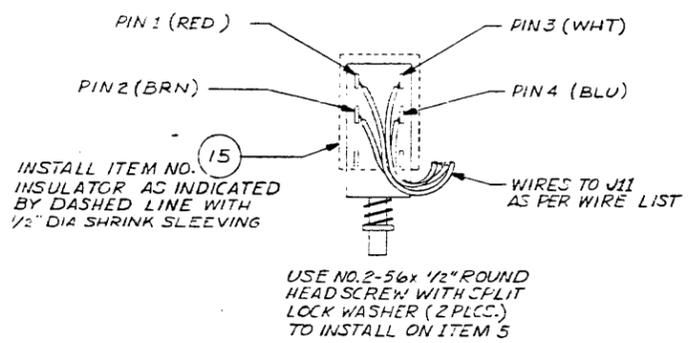
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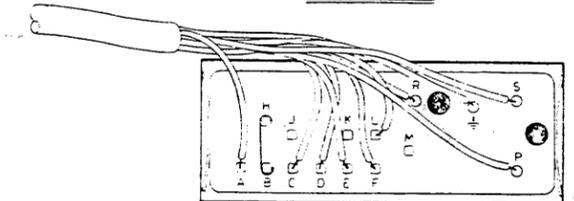
| WIRE LIST | | | | |
|-----------|---------|---------|-------|-------|
| AWG | COLOR | LENGTH | FROM | TO |
| 22 | RED | 5 1/2" | T1 | P5-1 |
| 22 | RED | 5 1/2" | T1 | P5-2 |
| 22 | WHT/RED | 5 1/2" | T1 | P5-3 |
| | | | | P5-4 |
| 22 | GRN | 5 1/2" | T1 | P5-5 |
| 22 | GRN | 5 1/2" | T1 | P5-6 |
| 22 | WHT/GRN | 5 1/2" | T1 | P5-7 |
| 22 | WHT/BLU | 5 1/2" | T1 | P5-8 |
| 22 | BLU | 5 1/2" | T1 | P5-9 |
| 22 | BLU | 5 1/2" | T1 | P5-10 |
| | | | | |
| 24 | BLK | 7" | T1 | J11-C |
| 24 | GRN | 7" | T1 | J11-A |
| 24 | WHT/BLK | 7" | T1 | J11-E |
| 24 | GRY | 7" | T1 | J11-D |
| 24 | WHT/GRY | 7" | T1 | J11-F |
| | | | | |
| 22 | WHT | 8" | J11-P | SW1-3 |
| 22 | RED | 8 1/2" | J11-S | SW1-1 |
| 22 | BRN | 7" | J11-R | SW1-2 |
| 22 | BLU | 7" | J11-L | SW1-4 |
| 22 | BUSS | — | J11-B | J11-H |
| 18 | GRN/YEL | 9" | J11-1 | A3 E2 |
| | | | | |
| 18 | GRN/YEL | 11 1/2" | A3 E1 | A2 E1 |
| 18 | GRN/YEL | 3 1/2" | A3 E1 | A4 E8 |

W1 WIRE MARKER (19)

POWER SWITCH (WIRING)



J11 (WIRING)



1. THIS SHEET IS INTENDED TO SHOW WIRE HOOK UP ONLY - REFERENCE SHEET 1 OF 2 FOR MECHANICAL ASSEMBLY.

NOTE: UNLESS OTHERWISE SPECIFIED

| | | | |
|--|---|-----------------------------|----------------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN: CHERMACK | DATE: 1-28-82 | |
| MATERIAL: | PROJ ENGR: [Signature] | RELEASE APPROV: [Signature] | |
| FINISH: WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030 | | ASSEMBLY, REAR PANEL (A3) |
| SCALE: | DO NOT SCALE DWG | MODEL NO: 190 | |
| | | 23338 | SHEET 2 OF 2 |

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REV BY DATE APP

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFOR | WAVETEK NO | QTY/PT |
|-----------------------|--|-------------------|-------|--------------|--------|
| NONE | ASSY DRWG REAR PANEL | 0102-00-0957 | WVTK | 0102-00-0957 | 1 |
| 3 | END BELL | 110-333 | WVTK | 1400-00-0174 | 1 |
| 2 | SPACER | 8480 | WVTK | 1400-00-0653 | 2 |
| 5 | LABEL, WARNING | 801-6940 | WVTK | 1400-00-6940 | 1 |
| 15 | INSULATOR PWR SWITCH REF 1400-79-0001 | 801-8370 | WVTK | 1400-00-8370 | 1 |
| 7 | I.D. LABEL | 801-9090 | WVTK | 1400-00-9090 | 1 |
| 8 | BRACKET, SWITCH MNTG | 189-3263 | WVTK | 1400-01-3263 | 1 |
| 9 | REAR PANEL | 190-3822 | WVTK | 1400-01-3822 | 1 |
| 4 | SHIELD, VOLTAGE | 191-5190 | WVTK | 1400-01-5190 | 1 |
| 13 | HOUSING | 1-640433-0 | AMP | 2100-02-0080 | 1 |
| 10 | RECEPTACLE | 6VJ1 | CORCH | 2100-03-0026 | 1 |
| 11 | SOLDER LUG | 11A144 | ZIER | 2100-04-0025 | 3 |
| 12 | FUSE, 3/4A, 250V, S-B | 313-750 | LITFU | 2400-05-0011 | 1 |
| 14 | SWITCH ASSY PB | 5103-00-0020 | WVTK | 5102-00-0005 | 1 |
| T1 | TRANSFORMER | 5600-00-0030 | COIL | 5600-00-0030 | 1 |

| | | | |
|------------------------------|---------------------------|------------------------------|----------|
| WAVETEK PARTS LIST | TITLE ASSY, REAR PANEL | ASSEMBLY NO. 1101-00-0957 | REV B |
| | PAGE 1 | | |

| | | | |
|--|--|------|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | WAVETEK SAN DIEGO • CALIFORNIA |
| MATERIAL | PROJ ENGR | | |
| FINISH WAVETEK PROCESS | RELEASE APPROV | | TITLE PARTS LIST ASSY, REAR PANEL |
| | TOLERANCE UNLESS OTHERWISE SPECIFIED XX - 011 ANGLES .1 XX - 030 | | MODEL NO. 190 |
| | SCALE AS SHOWN | | DWG NO. 1101-00-0957 |
| | | | REV B |
| | | | 23338 SHEET 1 OF 1 |

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-384

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| REV | ECN | BY | DATE | APP |
|-----|--------|------|---------|------|
| B | 4474 | | | |
| C | 4623 | | 6/2/82 | |
| D | # 8043 | M.C. | 3-12-87 | H.N. |

NO. 6-32x3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND SELF LOCKING NUT

NO. 4-40 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND SELF LOCKING NUT

NO. 4-40, 3/16" 82° FLAT HEAD SCREW APPLY A DROP OF LOCTITE 290 ADHESIVE (1600-03-0015) TO PROTRUDING THREADS AFTER ASSEMBLY. WIFE AWAY EXCESS IF NECESSARY

NOTE: P/N 2100-01-0006 BNC SHELL OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-0959

NOTE BOTTOM EDGE OF FRONT PANEL

NOTE ORIENTATION OF GROUND LUGS, AS SHOWN

INSTALL #20 AWG BUSS WIRE BETWEEN THESE GROUND LUGS, AS SHOWN

BNC GROUND LUG ORIENTATION

1. FOR FRONT PANEL PARTS LIST SEE: 1101-00-0980

NOTE UNLESS OTHERWISE SPECIFIED

| | | | | |
|--|---|------------------------|---|--------------------------------|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN <i>D. COOPER</i> | DATE <i>8/21/82</i> | WAVETEK SAN DIEGO • CALIFORNIA | |
| MATERIAL | PROLENGER <i>Kovach</i> | RELEASE APPROV. | TITLE ASSEMBLY FRONT PANEL (A2) | |
| FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX - 010 ANGLES .1 XX - 030 | | MODEL NO. 190 | DWG NO. 0102-00-0980 |
| SCALE | | DO NOT SCALE DWG | CODE IDENT 23338 | REV D |
| | | | SHEET 1 OF 1 | |

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| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|-----------------------|---------------------------------------|-------------------|---------|--------------|--------|
| NONE | ASSY DRWG, FRONT PANEL | 0102-00-0980 | WVTK | 0102-00-0980 | 1 |
| 1 | DIAL ASSY | WVTK | 190-187 | 1201-00-1873 | 1 |
| 2 | INDICATOR, DIAL | 180-303 | WVTK | 1400-00-4970 | 1 |
| 3 | FRONT PANEL | 190-3810 | WVTK | 1400-01-3810 | 1 |
| 4 | ANGLE, PANEL MNTG | 190-4523 | WVTK | 1400-01-4523 | 1 |
| 5 | ANGLE, PANEL MNTG | 190-4533 | WVTK | 1400-01-4533 | 1 |
| 6 | CONN BNC | KC-7946 | KING | 2100-01-0002 | 3 |
| 8 | SOLDER LUG | 1497 | SMITH | 2100-04-0012 | 3 |
| 9 | SOLDER LUG | 11A144 | ZIER | 2100-04-0025 | 1 |
| 10 | BUSHING NYLINER | 4L2FF | THOMN | 2800-01-0002 | 2 |
| 11 | BEARING, PANEL | 119 | SMITH | 2800-01-0004 | 1 |
| 12 | BUSHING (NYLINER) 1/B | 2L2FF | THOMN | 2800-01-0005 | 1 |
| 14 | WASHER, SHOULDER | 2668 | SMITH | 2800-27-0004 | 7 |
| 13 | NYLON FLAT WASHER | 2264-N-385 | AHTDM | 2800-28-0005 | 1 |
| NONE | WASHER, WAVE SPRING | 5804-133-1 | SEA | 2800-28-0021 | 1 |
| NONE | WASHER, FLAT, BRASS, .025 ID, .400 OD | 5714-62-32 | SESTM | 2800-28-0022 | 1 |

WAVETEK
PARTS LIST

TITLE
ASSY, FRONT PANEL

ASSEMBLY NO.
1101-00-0980

REV
A

PAGE 1

| REFERENCE DESIGNATORS | PART DESCRIPTION | ORIG-MFGR-PART-NO | MFGR | WAVETEK NO. | QTY/PT |
|-----------------------|---|-------------------------|------|--------------|--------|
| R56 | POT. DIAL, 5K +/- 5%, PRECISION, LINEAR | ECOND POT MKIII 78PF-14 | NEI | 4600-05-0212 | 1 |

WAVETEK
PARTS LIST

TITLE
ASSY, FRONT PANEL

ASSEMBLY NO.
1101-00-0980

REV
A

PAGE 2

| | | | |
|--|--|----------------|---|
| REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | TITLE PARTS LIST ASSY, FRONT PANEL |
| MATERIAL | PROJ/ENGR | RELEASE APPROV | |
| FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1 XX : 030 | | |
| DO NOT SCALE DWG | MODEL NO | DWG NO | |
| SCALE | SCALF | 23338 | REV A |
| CODE IDENT | | SHEET 1 | OF 1 |

NOTE: UNLESS OTHERWISE SPECIFIED