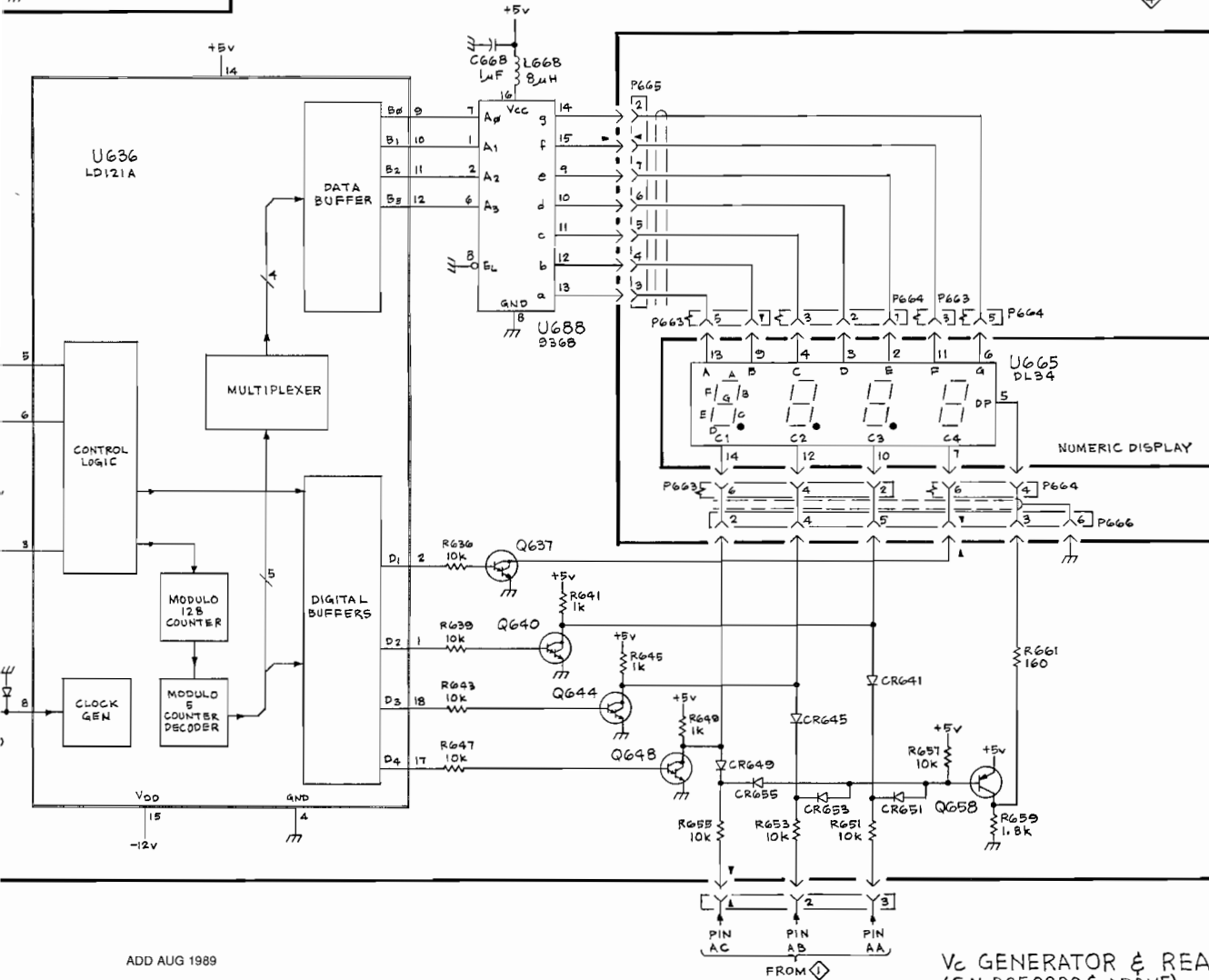
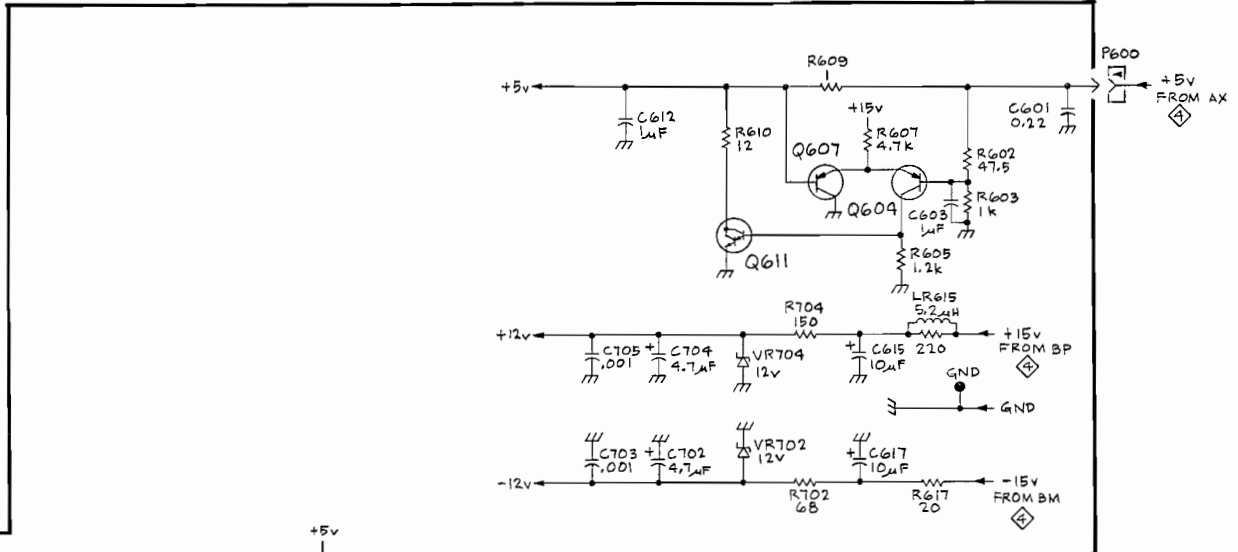
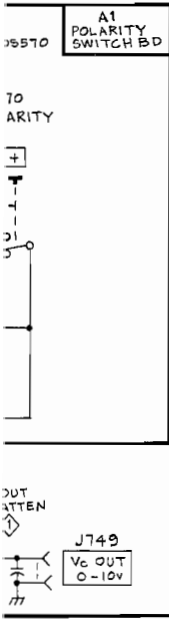


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ADD AUG 1989

Vc GENERATOR & READOUT (SN B25000 & ABOVE)

Vc GENERATOR & READOUT (SN B25000 & ABOVE)

5

Tektronix
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MANUAL CHANGE INFORMATION

Date: 5/30/90 Change Reference: M67379 Rev 2

Product: 7A13 Instruction

Manual Part No.: 070-1948-00

Product Group: 42

These changes are effective at serial number SN B250000 & above

Revised 8/25/89
Revised 5/30/90

TEXT CHANGES

Page 1-2, Table 1-1, column 2, **CHANGE TO READ:**

ACCURACY $\pm(0.1\%$ of setting +5 mV)

Page 3-8, V_c Generation and Digital Voltmeter Circuit (SN B250000 and above)

ADD:

The comparison voltage (V_c) is derived from a Zener diode reference, and is selectable by the COARSE and FINE front panel controls. The selected value of V_c is measured by the Digital Voltmeter circuit, and may be also be measured at the V_c OUT output jack on the front panel.

Zener diode VR683 sets a reference voltage, which is increased to approximately 10.8 volts by amplifier U684. Resistors R685, R686, and R687 set the output voltage level of the stage. This comparison voltage is applied to the variable voltage divider consisting of COURSE control R690A and FINE control R690B, along with R692, R693, R726, and R699. $+V_c$ ZERO control R696 sets the V_c minimum voltage level, which is applied to the V_c attenuator circuit and the V_c OUT jack.

Amplifier U728 inverts the comparison voltage and provides the $-V_c$ output to V_c POLARITY switch S570. R741 and C743 filter the V_c output voltage, which is applied through R742 to the attenuator circuit, and through R744 to the front panel V_c OUT jack. $-V_c$ CAL control R727 sets the gain for the inverter amplifier U728. $-V_c$ ZERO control R720 adjusts for the offset voltage of U728.

A to D Converter Voltmeter

The output of the variable voltage divider R690A and R690B, is fed through R692 and R693 to pin 15 (V_{in}) of U637, analog processor. During the measure interval the voltage at pin 15 U637, supplies current to the intergrator section, pin 9 of U637, that

is equal to $V_{in}/R622$. This causes the intergrator output to move away from voltage across C637, which is the average of the intergrator output. The output of comparator pin 5 U637, is sampled by the modulo 16 duty cycle counter in U636. This counter examines the state of the comparator once every 16 clock cycles during state 15. If the comparator is high the U/D control line pin 14 U637, and pin 5 U636, will be high for one cycle and low for 15 cycles. If the comparator output is low, the U/D control will be high for 15 cycles and low for one cycle. The effect of these two duty cycles is to source (or sink) a net of 14 charge parcels to C629, thus driving the intergrator output towards the voltage across C637, and accumulating counts in the Binary Coded Decimal (BCD) counter section of C636 in groups of 14 counts. The BCD count at the conversion equals the number of charged parcels necessary to cancel the input current supplied through R622. The resulting count is proportional to the voltage at V_{in} .

U638 acts as an input buffer to isolate V_{in} from the summing node at pin 9 of U637.

R635, VR635 and C635 provide a stable reference voltage for the intergrator section of U637.

The oscillator circuit consisting of Q623 and Q629 and associated circuitry provide a clock input to the digital processor U636.

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Page 3-9, V_e Readout Driver Circuit

CHANGE TO READ:

Refer to Diagram 5. U665 is a 4 digit common-cathode light-emitting-diode (LED) display. It is driven by the BCD to seven-segment decoder driver U668, the digit drivers Q637, Q640, Q644, Q648, and a Decimal Point Driver Q658. As a digit is selected by the scanner circuit within U636. The corresponding digit select output at pin D₁, D₂, D₃, D₄ goes high, turning on the appropriate digit driver. At the same time, the BCD output for that digit, at B₀, B₁, B₂, and B₃ of U636, will be decoded and buffered by U668, providing a 7 segment driving signal to U665.

Fig. 3-3a shows the time relationship of the U635 Decade Counter data output pulses, and illustrates the signals producing a readout of 1296 on the LED display. Pulses to the Step input of U636 drive the internal scanner circuit (at 1/100 of the clock frequency), causing high levels to be produced sequentially at digit selected outputs D₁, D₂, D₃, D₄ and simultaneously producing the corresponding BCD signal at B₀, B₁, B₂, and B₃. For example, while the least significant digit select output D₁ is high, outputs B₀ and B₃ are low, and B₁ and B₂ high, producing a binary coded decimal (BCD) output equivalent to number 6. This binary (0110) signal is encoded by U668 into a seven-segment driving signal for U665. To produce a 6 in the least significant position of the LED display, two conditions are met. The input signals to U665 are high at A, C, D, E, F, and G, and low at B; second, the high level at D₁ turns on Q637 providing a low at pin 7 of U665. This provides a current path to ground for the light-emitting-diodes, which forms the number 6 on the LED display. Other digits are displayed in a similar manner.

Transistors Q640, Q644, and Q648 perform two functions. First, they provide a current path to ground for the light-emitting-diodes of digit 1, 2, and 9, when turned on by the respective digit select outputs D₂, D₃, or D₄; also, they form part of a circuit to time-multiplex drive signals to Q658, producing the required decimal point placement on the LED display. For example, if the decimal placement is 129.6, the voltage produced by the Decimal Point Logic circuit will be approximately zero volt at pin AA, and approximately five volts at pins AB and AC, at P650, reverse biasing CR645 and CR649. Quietly, Q640 is cut off, causing current flow through divider R641, CR641, and R651, producing approximately 4.0 volts at the cathode of CR641. Q658 is biased at threshold by the divider R657, CR651, and CR641 cathode voltage. When the digit select output pulse D₂ arrives, Q640 turns on, its output goes low, and CR641 is cut off. This causes CR651 to conduct hard, saturating Q658, which allows current to flow through R661, to pin 5

of U665, and through the decimal point light-emitting-diode for the least significant digit, producing a decimal placement 129.6.

Large current fluctuations produced by the LED display circuit are reduced by the shunt regulator, composed of Q604, Q607, and Q611. This is achieved by the negative feedback action of Q607, with the base acting as the input, and Q611 as the output stage. R609 prevents large voltage variations from appearing in the 5-volt source supply.

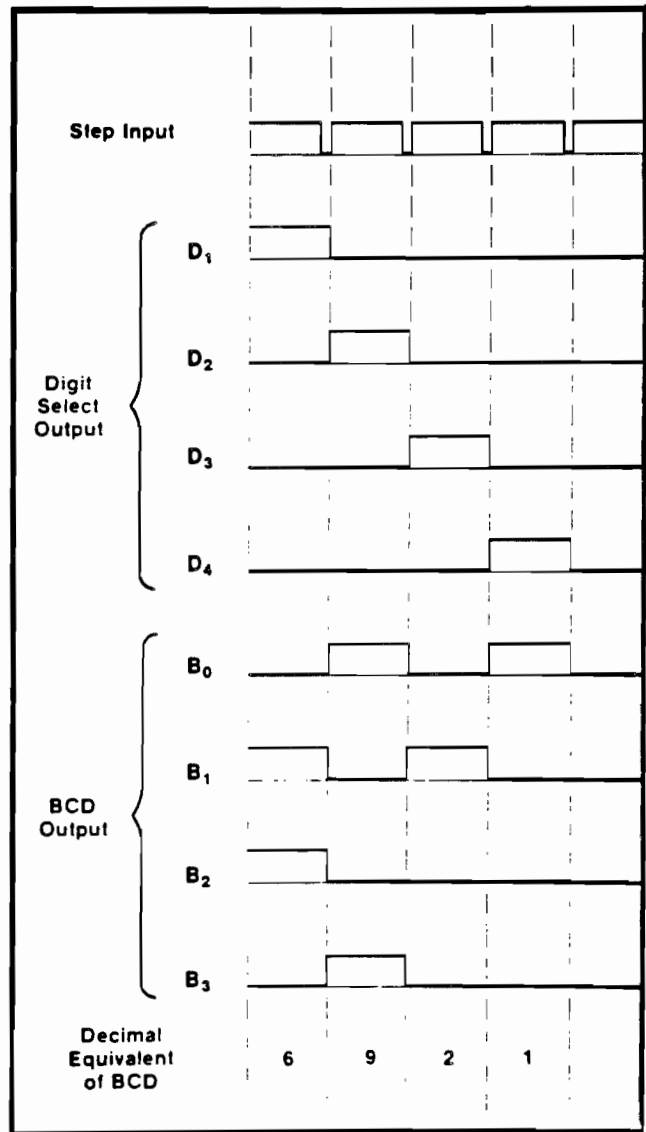


Fig. 3-3a. Time relationship of the pulses from U635. (SN B250000 & above).

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Page 5-38 and 5-39, Section 5,

Comparison Voltage Adjustments

CHANGE TO READ:

27. Check/Adjust $+V_c$ Zero

a. Make sure all adjustments are centered before starting.

b. Connect the precision DC Voltmeter between the V_c OUT JACK and GROUND on the 7A13, and set the Voltmeter to the 200mV range.

c. Using the POSITION control, position the trace to coincide with the graticule center line.

d. Change the +INPUT switch to V_c .

e. ADJUST - The $+V_c$ Zero control R696 (refer to Fig 5-19a) to set the trace 1 division below midscreen. Verify that the voltmeter measures approximately -1.00mV.

28. Check/Adjust $-V_c$ Zero

a. Change the V_c Polarity switch to -.

b. ADJUST - The $+V_c$ Zero control R720 to set the trace 1 division above midscreen. Verify that the voltmeter measures approximately -1.00mV.

c. INTERACTION - Repeat steps 27 and 28 until the voltmeter measures between -1.10mV and -0.90mV for the $+V_c$ Polarity and between +0.90mV and +1.10mV for the $-V_c$ Polarity.

29. Check/Adjust DVM Zero

a. Change the V_c Polarity switch to + and turn the COMPARISON VOLTAGE (V_c) FINE control clockwise until the voltmeter measures approximately 0.5mV and the trace is 0.5 divisions above midscreen.

b. ADJUST - DVM Zero control R644 (Fig. 3-3a) carefully so that the V_c reading decreases as R644 is turned counterclockwise, stopping exactly where the V_c reading changes from 0.001 to 0.000. When properly adjusted, the V_c reading should alternate between 0.000 and 0.001.

c. Recheck and reference set +input to ground. Re-center trace. Set + input to V_c .

d. VERIFY - Turn the COMPARISON VOLTAGE (V_c) FINE control clockwise to move the trace 0.08 divisions above midscreen. Check that the V_c reading is 0.001. Move trace to +0.02 divisions. Check that the LEDs read 0.000. Set trace 2 divisions above midscreen. Check that LEDs read 0.002.

30 Check/Adjust $+V_c$ range Control

a. Set the Precision DC Voltmeter to the 20 volt range.

b. Turn the COMPARISON VOLTAGE (V_c) COARSE and FINE controls fully clockwise.

c. ADJUST - The $+V_c$ range control R686 so the voltmeter reads between 10.015 and 10.150 volts.

31. Check/Adjust $+V_c$ Cal

a. Turn the COMPARISON VOLTAGE (V_c) COARSE and FINE controls counterclockwise for a reading of 9.900 volts on the precision DC Voltmeter.

b. ADJUST - The $+V_c$ Cal control R634 to obtain a V_c reading of 9.900 on the LEDs.

32. Check/Adjust $-V_c$ Cal

a. Change the V_c Polarity switch to -.

b. Turn the COMPARISON VOLTAGE (V_c) FINE control, if necessary, to obtain a V_c reading of 9.900 on the LEDs.

c. ADJUST - The $-V_c$ Cal control R727 to obtain a 9.900 reading on the Precision DC Voltmeter.

33. Check $+V_c$ Linearity

a. Change the front panel controls as follows:

(V_c) Polarity	+
+INPUT	GND
COMPARISON VOLTAGE,	
COARSE and FINE	Fully CCW
POSITION control	trace midscreen

b. Change the + INPUT switch to V_c .

c. Adjust the $+V_c$ Zero control R696, if necessary, to position the trace one division below midscreen.

d. Check the $+V_c$ linearity by rotating the COMPARISON VOLTAGE (V_c) COARSE and FINE controls.

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33. Check +V_c Linearity

a. Change the front panel controls as follows:

(V _{cv}) Polarity	+
+INPUT	GND
COMPARISON VOLTAGE,	
COARSE and FINE	Fully CCW
POSITION control	trace midscreen

b. Change the + INPUT switch to V_{cv}.

c. Adjust the +V_c Zero control R696, if necessary, to position the trace one division below midscreen.

d. Check the +V_c linearity by rotating the COMPARISON VOLTAGE (V_c) COARSE and FINE controls.

e. Change the V_c Polarity switch to -, and repeat part d.

f. Disconnect and turn off the precision DC Voltmeter.

34. Check Range of Comparison Voltage Fine control

a. Rotate the COMPARISON VOLTAGE (V_c) FINE control fully counterclockwise. Note V_c readout on 7A13 display.

b. Rotate the FINE control fully clockwise. Note the increased reading by at least 0.030, but no more than 0.040.

35. Check V_c OUT Resistance

a. Set the FINE and COARSE controls to the fully counterclockwise position.

b. Check for 2 kΩ to 5.5kΩ at the V_c OUT jack.

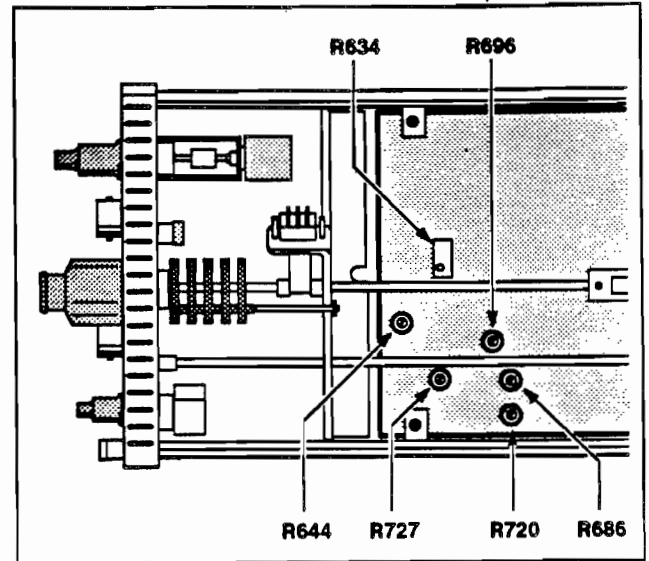


Fig. 5-19a. Comparison adjustment locations (SN B250000 and up.)

7A13 (SN B25000 & ABOVE)

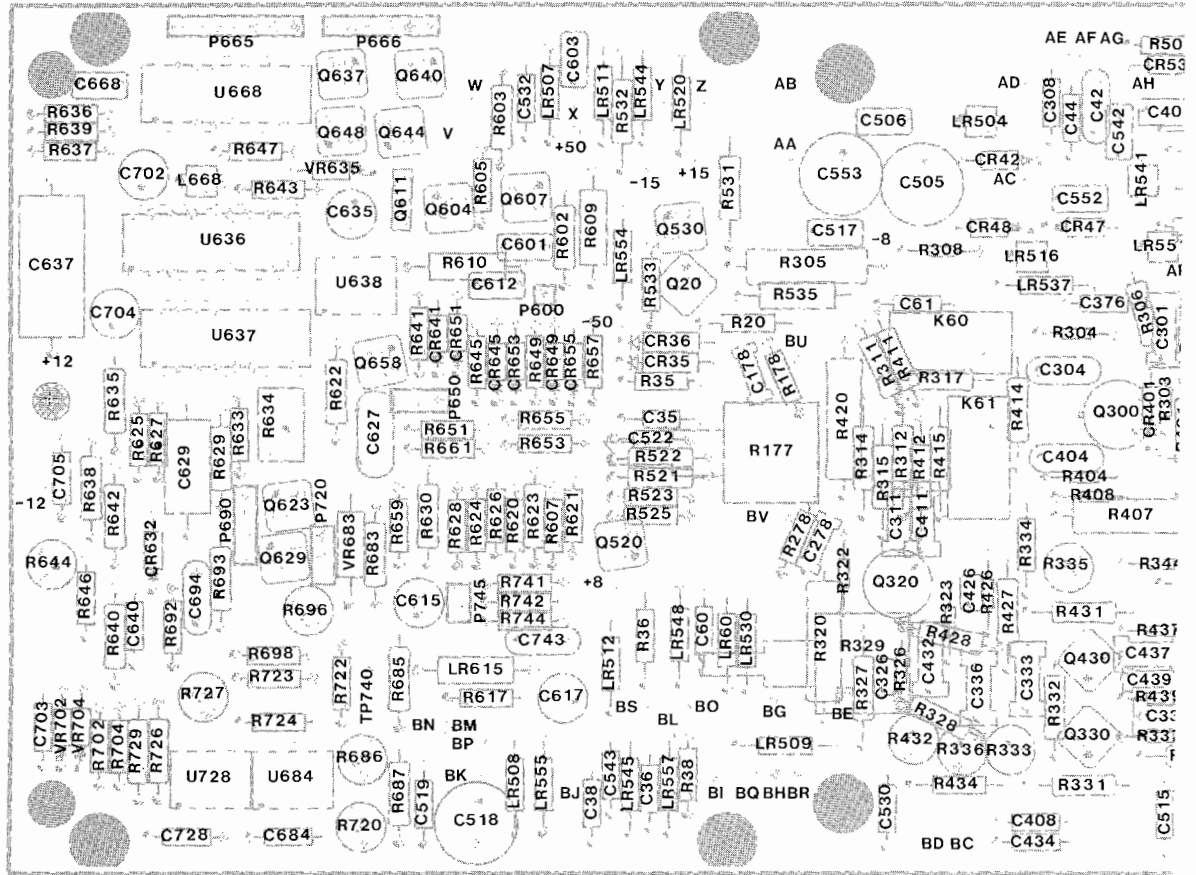


Fig. 7-4. Output Amplifier circuit board component locations (SN B250000 an

OUTPUT AMPLIFIER
COMPONENT LOCATIONS
(SN B250000 & ABOVE)

