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HP 70311A and HP 70312A Clock Sources

Operating and Calibration Manual

SERIAL NUMBERS

This manual applies directly to:

HP 70311A Clock Source with serial number(s) prefixed 3120U.

HP 70312A Clock Source with serial number(s) prefixed 3143U.

For additional important information about serial numbers, refer to SERIAL NUMBER INFORMATION in Chapter 1.

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HEWLETT PACKARD

HP Part No. 70311-90000
Microfiche Part No. 70311-90025
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WARNING

READ THE FOLLOWING NOTES BEFORE INSTALLING OR SERVICING ANY INSTRUMENT.

1. IF THIS INSTRUMENT IS TO BE ENERGISED VIA AN AUTO-TRANSFORMER MAKE SURE THAT THE COMMON TERMINAL OF THE AUTO-TRANSFORMER IS CONNECTED TO THE NEUTRAL POLE OF THE POWER SOURCE.
2. THE INSTRUMENT MUST ONLY BE USED WITH THE MAINS CABLE PROVIDED. IF THIS IS NOT SUITABLE, CONTACT YOUR NEAREST HP SERVICE OFFICE. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).
3. BEFORE SWITCHING ON THIS INSTRUMENT:
   a. Make sure the instrument input voltage selector is set to the voltage of the power source.
   b. Ensure that all devices connected to this instrument are connected to the protective (earth) ground.
   c. Ensure that the line power (mains) plug is connected to a three-conductor line power outlet that has a protective (earth) ground. (Grounding one conductor of a two-conductor outlet is not sufficient).
   d. Check correct type and rating of the instrument fuse(s).

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Documentation Description

Introduction

This manual provides information on how to install and operate the HP 70311A/HP 70312A clock source. Topics covered by this manual include specifications, installation, operation, performance tests, and programming information to enable the clock source to be operated remotely.

Reference Documentation

The following manuals are not provided with the HP 70311A/HP 70312A clock source, but provide useful reference material when installing a clock source in an HP 71600 Series Modular Measurement System.

HP 70004A Graphics Display

Operating Manual (Part Number 70004-90031)
Installation and Verification Manual (Part Number 70004-90005)

HP 70001 Mainframe

Installation and Verification Manual (Part Number 70001-90021)

HP 71600 Series of Gbit/s Testers

Installation and Verification Manual (Part Number 71600-90005)
Operating and Programming Manual (Part Number 71600-90004)

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DECLARATION OF CONFORMITY

Manufacturer's Name: Hewlett-Packard Limited
Queensferry Telecommunications Division

Manufacturer's Address: South Queensferry
West Lothian
Scotland EH30 9TG

declares, that the product

Product Name : Clock Source

Model Number(s): HP 70311A

Product Options: This declaration covers all options of the above product.

conforms to the following Product Specifications:

Safety: IEC 348 (1978)
CSA Bulletin 556B (1973)

EMC: EN 55011 (1991) Group 1, Class A
EN 50082-1 (1991)

South Queensferry, Scotland	05 March 1992	W R Pearson
Location	Date	W.R. Pearson/Quality Manager

5955-2395

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1

General Information

General Information

Introduction

This chapter provides the following information on the HP 70311A and HP 70312A clock source modules:

- A general description of clock source features.
- Serial number information
- Returning modules for service.
- ESD precautions
- Specifications

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HP 70311A/HP 70312A Clock Source

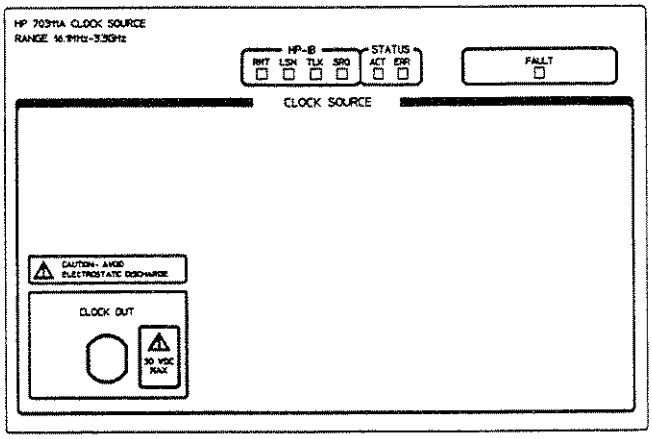

Figure 1-1. Clock Source

Description

The HP 70311A and HP 70312A modules are synthesized clock sources designed to operate from 16 to 3300 MHz and 16 to 1500 MHz respectively. Both modules are part of the Hewlett-Packard Modular Measurement System (MMS) and may be used as a clock source for the HP 71600 Series of error performance analyzers and pattern generators, or any other MMS system with a suitable display (for example HP 70004A).

The clock source contains a non-volatile memory store which can be used to store and recall 10 user-definable instrument setups.

HP 70311A Clock Source (16 to 3300 MHz)

The HP 70311A can be used with the HP 70841B pattern generator, which does not have an internal clock source, and the HP 70842B error detector, both of which are part of an HP 71600 Series System. The HP 70311A may be used with an HP 70310A precision frequency reference in applications which require greater frequency accuracy. Refer to chapter 3 for information on how to configure the HP 70310A with the clock source.

HP 70312A Clock Source (16 to 1500 MHz)

The reduced frequency range is the only specification difference between the HP 70312A and the HP 70311A; otherwise all references to the HP 70311A apply to the HP 70312A.

Front Panel Leds

The HP 70311A/70312A clock source modules include the standard HP-IB status indicators (RMT, LSN, TLK, SRQ) and MMS status indicators (ACT, ERR). It also includes a fault indicator LED; if this is on, then the instrument has detected a hardware fault.

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User Interface

The HP 70311A clock source does not itself have a display or keyboard capability. It formats information suitable for an MMS display and communicates with the display over the HP-MSIB interface. The HP 70312A clock source user interface is identical to the HP 70311A. The recommended display for use with the clock source is the HP 70004A.

Using Softkeys to Select User Functions

Clock source functions are set up using softkeys on either side of the display; refer to chapter 4 for an explanation of clock source softkeys.

Notation

Throughout this manual, hardkey indicates hardkeys and softkey indicates softkeys.

Clock Source Window Size

In an MMS display you can elect to display module status in a full size (24 lines by 53 characters), half size or quarter size window. See pages 6-3 to 6-4 of the HP 70004A display Operation Manual.

The clock source will work with a small window (down to 6 lines by 26 characters) by restricting the amount of information that is displayed. If the window is too small to display the minimal amount of information, a warning message *Window is too small* is displayed. If your clock source is part of an HP 71600 Series Error Performance Analyzer or Pattern Generator system only full or half size windows are permissible. Refer to chapter 5 of the HP 71600 Series of Gbit/s Testers Operating and Programming Manual for advice on how to display module status in two half size windows.

Serial Number Information

Attached to the clock source module is a serial number plate. A typical serial number is in the form XXXXUXXXXX. It is in two parts; the first four digits and the letter are the serial prefix and the last five are the suffix, the letter designates the country of origin - U is the United Kingdom. The prefix is the same for identical clock source modules, it only changes when a change is made to the clock source. The suffix however, is assigned sequentially and is different for each clock source module. The contents of this manual apply to clock source modules with the serial number prefix(es) listed under *SERIAL NUMBERS* on the title page.

A module manufactured after the printing of this manual may have a number prefix that is not listed on the title page. The unlisted serial number prefix indicates the module is different from the one described in this manual. The manual for this new clock source is accompanied by a *Manual Changes* supplement. This supplement contains *change information* that explains how to adapt the manual to the new clock source.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement.

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The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard. For information concerning a serial number prefix that is not listed on the Manual Changes supplement, contact your nearest Hewlett-Packard office.

Returning Modules for Service

This section explains how you return a module to Hewlett-Packard for servicing.

Packaging Requirements

Modules can be damaged as a result of using packaging materials other than those specified. Never use styrene pellets as packaging material. They do not adequately cushion the module nor prevent it from shifting in the carton. They also cause instrument damage by generating static electricity.

Preparing a Module for Shipping

1. Fill out a blue repair tag (located at the front of this manual) and attach it to the module. Include any error messages or specific performance data related to the problem. If a blue tag is not available, the following information should be noted and sent with the module:
   - Type of service required.
   - Description of the problem.
   - Whether problem is constant or intermittent.
   - Name and phone number of technical contact person.
   - Return address.
   - Model number of returned module or instrument.
   - Full serial number or returned module or instrument.
   - List of any accessories returned with the module or instrument.
2. Pack the module or instrument in the appropriate packaging materials. Original shipping or equivalent materials should be used. If the original or equivalent material cannot be obtained, follow the instructions below:

Caution

Inappropriate packaging of the instrument may result in damage to the instrument during transit.

- Wrap the instrument in anti-static plastic to reduce the possibility of damage caused by electrostatic discharge (ESD).
- Use a double-walled, corrugated cardboard carton of 159 kg (350 lb) test strength.

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Caution

If you are shipping a complete system, remove the module(s) from the Display and Mainframe, individually pack each module, then ship them to Hewlett-Packard.

- The carton must be large enough to allow 3 to 4 inches on all sides of the instrument for packing material and strong enough to accommodate the weight of the instrument.
- Surround the instrument with 3- to 4-inches of packing material, to protect the instrument and prevent it from moving in the carton.
- If packing foam is not available, the best alternative is S.D.-240 Air Cap™ from Sealed Air Corporation (Commerce, California 90001). Air Cap™ looks like a plastic sheet filled with air bubbles.
- Use the pink (anti-static) Air Cap™ to reduce static electricity. Wrapping the instrument several times in this material will protect the instrument and prevent it from moving in the carton.

3. Seal the carton with strong nylon adhesive tape.
4. Mark the carton *FRAGILE, HANDLE WITH CARE.*
5. Retain copies of all shipping papers.

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Precautions

ESD Precautions

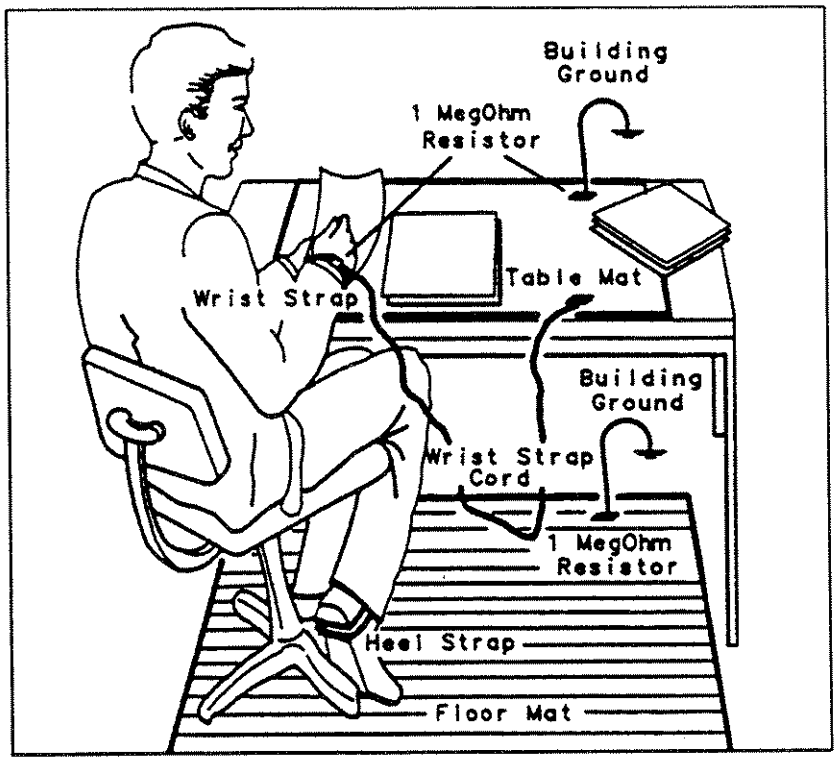
Electrostatic discharge (ESD) can damage or destroy electronic components. All work on electronic assemblies should be performed at a static-safe workstation.

Static-safe Workstation

A typical static-safe workstation is illustrated in the following diagram. There are two types of ESD protection:

- Wrist-strap (with > 1 MΩ isolation to ground) with table-mat.
- Heel-strap (with > 1 MΩ isolation to ground) with conductive floor-mat.

These two types must be used together to ensure adequate ESD protection. Isolation to ground must be provided for personnel protection.



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Static-safe Accessories

The following table lists the accessories that may be ordered through any Hewlett-Packard sales and service office.

HP Part Number	Description
9300-0797	3M static control mat 0.6 m x 1.2 m (2 ft x 4 ft) and 4.6 m (15 ft) of ground wire. (The wrist-strap and wrist-strap cord are not included. They must be ordered separately.)
9300-0980	Wrist-strap cord 1.5 m (5 ft).
9300-1383	Wrist-strap, black, stainless steel, has four adjustable links and a 7 mm post-type connection.
9300-1169	ESD heel-strap (reusable 6- to 12- months)
*92175A	Black, hard surface, static control mat, 1.2 m x 1.5 m (4 ft x 5 ft)
*92175B	Brown, soft surface, static control mat, 1.2 m x 2.4 m (4 ft x 8 ft)
*92175C	Small, black, hard surface, static control mat, 0.9 m x 1.2 m (3 ft x 4 ft)
*92175T	Table-top static control mat, 58 cm x 76 cm (23 in x 30 in)
*92176A	Natural color anti-static carpet, 1.2 m x 1.8 m (4 ft x 6 ft)
*92176B	Natural color anti-static carpet, 1.2 m x 2.4 m (4 ft x 8 ft)
*92176C	Russet color anti-static carpet, 1.2 m x 1.8 m (4 ft x 6 ft)
*92176D	Russet color anti-static carpet, 1.2 m x 2.4 m (4 ft x 8 ft)

*Can also be ordered by calling HP DIRECT Phone (800) 538 8787.

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Specifications

Introduction

Except where otherwise stated, the following parameters are warranted performance specifications. Parameters described as *typical* or *nominal* are supplemental characteristics which provide a useful indication of typical, but non-warranted, performance characteristics. All specifications are for 0 °C to 45 °C after 30 minutes warm-up.

Frequency Range

Frequency Range (HP 70311A)	16.09375 - 3300 MHz
Frequency Range (HP 70312A)	16.09375 - 1500 MHz

Frequency Bands

The exact end points and their approximations for each frequency band of the instrument are shown below.

Approx End points MHz	Exact End points Hz
16 - 32	16,093,750.00 - 32,187,499.99
32 - 64	32,187,500.00 - 64,374,999.99
64 - 128	64,375,000.00 - 128,749,999.99
128 - 257	128,750,000.00 - 257,499,999.99
257 - 515	257,500,000.00 - 514,999,999.99
515 - 1030	515,000,000.00 - 1,029,999,999.99
1030 - 2060 (70311A)	1,030,000,000.00 - 2,059,999,999.99
2060 - 3300 (70311A)	2,060,000,000.00 - 3,300,000,000.00
1030 - 1500 (70312A)	1,030,000,000.00 - 1,500,000,000.00

Signal paths are switched when changing from one band to another. Signal paths are also switched within frequency bands. This is done to select the correct filtering so that the instrument specifications are met.

Frequency Resolution

Resolution	0.01 Hz
Min frequency step size	0.01 Hz
Max frequency step size	1 GHz

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Stability (typical)

Using Internal Reference Source:

Aging, after 1 year	± 2 ppm/year
Temperature, 0 to 45 °C	± 6 ppm

Settling Times (typical)

To within 100 Hz of final frequency and to within level spec: <200 mS

Output Characteristics

Connector	N type, female
Output impedance	50 ohms, ac coupled
Output Waveform	Sine wave
Protection	No damage with any load VSWR
Maximum applied power	+20 dBm
Maximum applied DC voltage	30 V
Output Return Loss (typical)	6 dB
Output Level, dBm	
Output on	0 dBm ± 3 dB
Output off (typical)	<-50 dBm

Sub Harmonics

Frequency Band	
16 - 515 MHz	None
515 - 1030 MHz	<-55 dBc
1030 - 2060 MHz (70311A)	<-40 dBc
2060 - 3300 MHz (70311A)	<-35 dBc
1030 - 1500 MHz (70312A)	<-40 dBc

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Multiplied Sub Harmonics

(Output frequency 1.5)

Frequency Band	
16 - 1030 MHz	None
1030 - 2060 MHz (70311A)	<-40 dBc
2060 - 3300 MHz (70311A)	<-35 dBc
1030 - 1500 MHz (70312A)	<-40 dBc

Harmonics

Frequency Band	
16 - 3300 MHz (70311A)	<-30 dBc
16 - 1500 MHz (70312A)	<-30 dBc

Non-Harmonic Spurious Tones at >15 kHz offset

Frequency Band	
16 - 1030 MHz	<-100 dBc
1030 - 2060 MHz (70311A)	<-94 dBc
2060 - 3300 MHz (70311A)	<-88 dBc
1030 - 1500 MHz (70312A)	<-94 dBc

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Phase Noise Using Internal Reference Source

Frequency Band MHz	Offset 1 kHz	20 kHz	100 kHz
	dBc/Hz	dBc/Hz	dBc/Hz
16 - 32	-113	-140	-140
32 - 64	-108	-140	-140
64 - 128	-103	-140	-140
128 - 257	-98	-138	-140
257 - 515	-93	-134	-140
515 - 1030	-88	-128	-138
1030 - 2060 (70311A)	-81	-121	-131
2060 - 3300 (70311A)	-75	-115	-125
1030 - 1500 (70312A)	-81	-121	-131

Broadband Noise Floor

At >10 MHz offset from carrier <-140 dBc/Hz (typical)

External Reference Input

Connector	SMB male, rear panel
Input impedance	50 ohms, ac coupled
Maximum input power	+20 dBm
Frequency	10 MHz +/-1 kHz
Amplitude	0.224/2 V rms

Module control

May be controlled using an MMS display, for example the HP 70004A display.

General

Form: 4/8 width MMS module

MMS configuration: Can be MMS master, or slave to HP 70841A, HP 70841B or HP 70845A pattern generator modules. The HP 70310A precision frequency reference module may be slaved to the HP 70311A or HP 70312A.

Non-volatile set-up stores: Save and recall 10 instrument set-ups.

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Status indicators:

HPIB: RMT, LSN, TLK, SRQ
MMS: ACT, ERR
FAULT: On when the instrument has detected a hardware fault.

Weight: 8.9 kg (20 lbs)

Power requirements: All module power requirements are provided by the MMS mainframe or display.

HP-IB interface and capability

The HP 70311A and HP 70312A clock source modules can be operated under HP-IB control when fitted in an MMS display or mainframe.
Operates according to IEEE standard 488.1 and 488.2, 1987. Conforms, where appropriate, to the Standard Commands for Programmable Instruments (SCPI) standard 1990.0.

Capability: SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT0, C0, E1.

Addressable operation: An external controller can control all module functions except HP-IB, HP-MSIB addresses and power switch, and has access to all status and alarm codes.

Environmental

Operating temperature range: 0 to 45 °C

Storage temperature range: -40 to 65 °C

Humidity: 95% RH @ 40 °C

EMC: Conducted and radiated interference is in compliance with CISPR Pub 11, FTZ 526/1979 and MIL-STD 461B RE02/part 7 when operated in an MMS rack.

Safety: Complies with IEC 348 and CSA Bulletin 556B when operated in an MMS rack.

Noise:

LpA < 70 dB	LpA < 70 dB
operator position	am Arbeitsplatz
normal operation	Normaler Betrieb
per ISO 7779	nach DIN 45635 T. 19

Calibration interval: Recommended 1 year

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2

Installation

This chapter enables you to install your clock source ready for use. The information is presented under the following headings:

Preparation for Use	Provides information you should read before you install your clock source. It contains information on initial inspection, power requirements, and address switches.
Module Installation	Shows you how to install your clock source into an HP 71600 Series of Gbit/s Testers Error Performance Analyzer or Pattern Generator System.
Selftest at Power-on	Describes the events at power-on.
Module Verification	Describes where to find procedures to verify instrument operation.
Installing/Removing Modules	Describes how you install modules into an MMS display and mainframe.

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Preparation for Use

This section should be read before you install your system. It contains the following:

- Initial Inspection
- Operating Requirements
- HP-MSIB Address Switches
- HP-IB Address Switches

Initial Inspection

Warning **To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosure (covers, panels, meters).**

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the clock source module has been checked both mechanically and electrically. Procedures for checking the electrical operation are given in chapter 5 of this manual.

If the clock source module appears damaged or is defective, contact the nearest Hewlett-Packard service office. Hewlett-Packard will arrange for repair or replacement of the equipment without waiting for a claim settlement. Retain the shipping materials for the carrier to inspect.

Undamaged shipping materials should be kept. Original HP or equivalent shipping materials are required for module re-shipment, as substandard packaging may result in damage. Refer to *Returning Modules for Service* in chapter 1 for information on re-shipment.

Operating Requirements

Operating and Storage Environment

The clock source module can be operated in temperatures from 0 °C to +45 °C. For storage, the temperature range is −40 °C to +65 °C.

The module should be protected against temperature extremes which can cause condensation within the elements in your system.

Physical Specifications

The HP 70311A/HP 70312A clock source is packaged in a 4/8 size MMS module. Its weight is approximately 8.9 Kg.

Power Requirements

The clock source derives its power from the MMS display or mainframe in which it is installed.

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Electrical Specifications

Refer to chapter 1 for detailed clock source specifications.

Warning

Before turning the system on, make sure it is grounded through the protective conductor of the power cable to a socket outlet with protective earth contact. Any interruption of the protective (grounding) conductor inside or outside the instrument, or disconnection of the protective earth terminal, can result in personal injury.

HP-MSIB Address Switches

The HP-MSIB address switches are factory preset to configure your clock source as a slave in a master/slave Modular Measurement System (MMS). For example, in an HP 71600 Series Error Performance Analyzer or Pattern Generator system.

If you want to change the master/slave addressing or want to change to master/master configuration, ensure you are fully aware of the HP-MSIB address protocol, see chapter 6 of the HP 71600 Series of Gbit/s Testers Installation and Verification Manual, or refer to the HP 70004A Display Installation and Verification Manual.

In an HP 71600 Series Error Performance Analyzer system the error detector master module controls the slave pattern generator module and the clock source. The pattern generator module (a slave to the error detector) is a sub-master to the clock source. The clock source is controlled directly by the pattern generator, and indirectly by the error detector (through the pattern generator).

In a pattern generator system the master module is the pattern generator, it controls the slave clock source.

Factory Preset HP-MSIB Addresses

The clock source factory preset HP-MSIB addresses (row,column) are listed below:

Clock Source :Row 2, Column 19

* The column value defines the factory preset HP-IB addresses.

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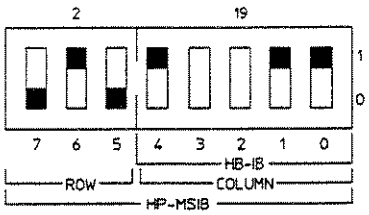
Clock Source Address Switches

The factory preset switch settings are shown in the following diagram:



HP-IB Address Switches

The HP-MSIB address switches in a master module (one whose row address is 0) also act as HP-IB switches. If you want your system to communicate over the HP-IB the *row* switches must be set to *0*. The *column* switches define the *HP-IB* address.

If you want to change the HP-IB address (use an address that is different from that defined by the *column* switch settings), it is recommended that you use the Display *HP-IB Address* function, see the *HP 70004A Display Operating Manual*.

Caution

It is not recommended that you change the HP-IB address using the HP -MSIB/HP-IB switches, as these also change the HP-MSIB address. If the HP-MSIB address protocol is violated your system will fail to operate.

Factory Preset HP-IB Addresses

The Clock Source HP-IB address is factory preset to 19 (column part of HP-MSIB switch setting).

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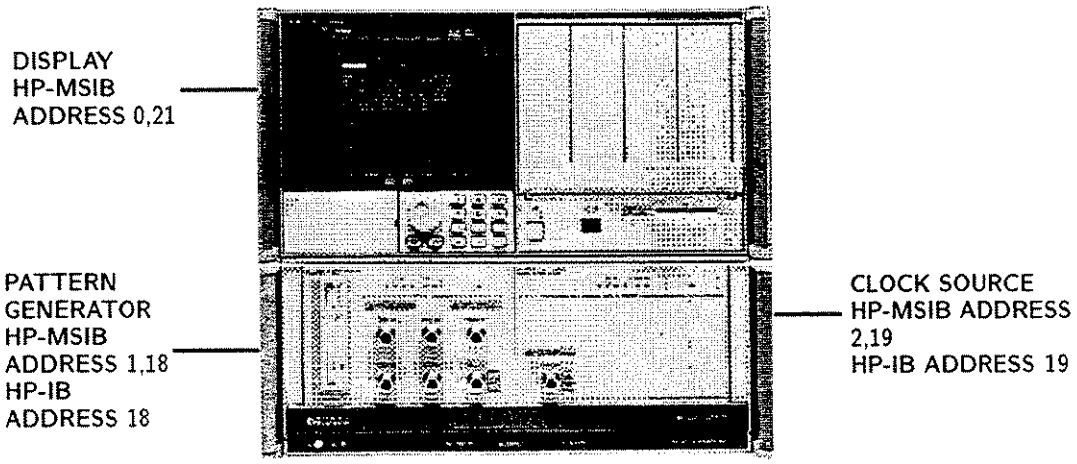
Module Installation

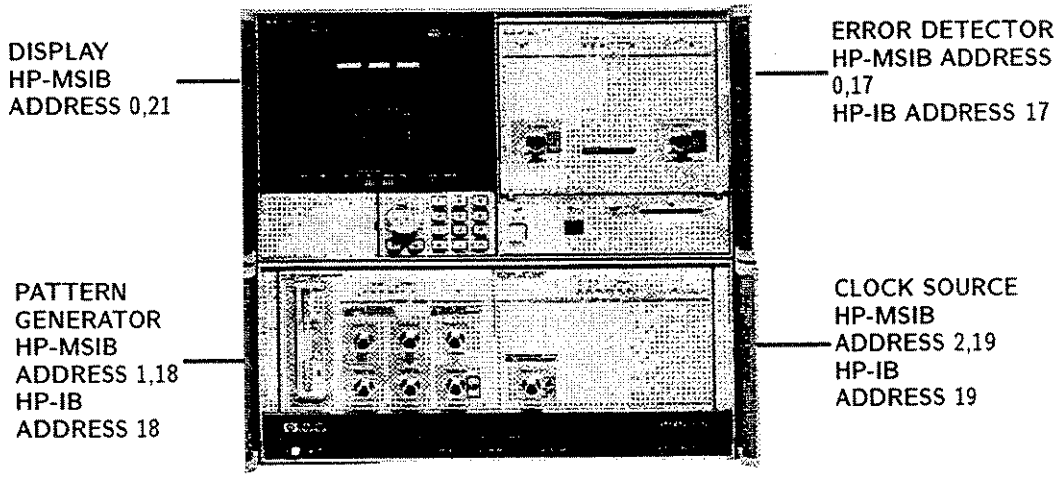
Your HP 70311A or HP 70312A clock source can be installed as part of the HP 71600 Series Error Performance Analyzer, or Pattern Generator systems. The recommended addresses for HP 71600 Series Modules configured in master/slave format are as follows:

- Display: row 0, column 21
- Error Detector: row 0, column 17
- Pattern Generator: row 1, column 18
- Clock Source: row 2, column 19
- Precision Frequency Reference: row 3, column 20

A graphic example is given below of each system.



Pattern Generator System



Error Performance Analyzer System

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Selftest at Power-on

At power-on the HP 70004A display will carry out a number of internal self-test routines lasting approximately five seconds.

On the clock source module all LEDs are lit for approximately two seconds, and then extinguished. If a fault occurs the *FAULT* LED on the clock source front panel is illuminated, and a red letter *E* is displayed at the top left of the HP 70004A display. The *FAULT* LED will remain on until the fault is cleared.

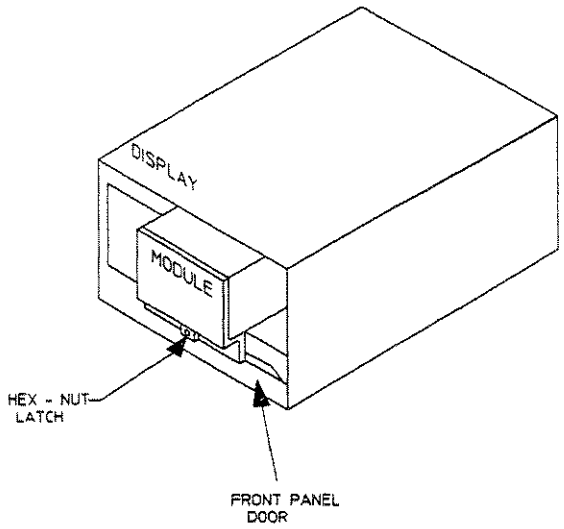
Module Verification

If you wish to verify that the clock source module is operating correctly, refer to the Operational Verification procedures given in chapter 6 of this manual.

Installing/Removing Modules

Use the following procedures to install your module into the Display or Mainframe. To remove a module, perform the steps in the reverse order.

Installing a Module into a Display



1. Switch off the power to the display.
2. Open the front panel door then insert the module.
3. Secure the module by pressing against its front panel while tightening the hex-nut latch with an 8 mm hex-ball driver.
4. Close the front panel door.
5. Turn on the power to the display.

When removing a clock source module, disconnect any cable connected to the rear panel *EXT REF* port.

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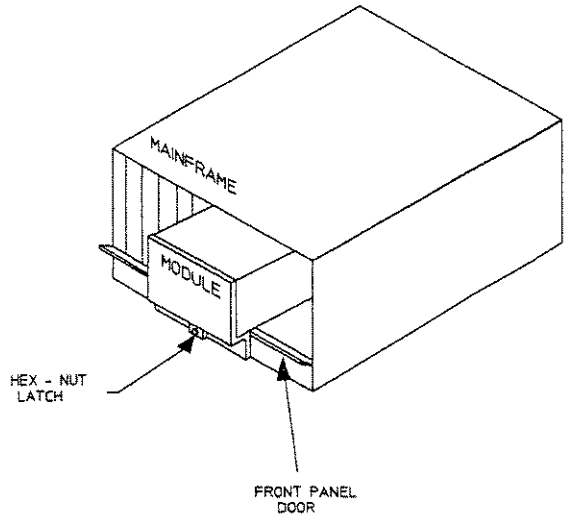
Installing a Module into a Mainframe



1. Switch off the power to the mainframe.
2. Open the front panel door, then insert the module into the mainframe (the module can operate in any location).

Caution The Mainframe LINE power switch must be set to off before the front panel door will open.

3. Secure the module by pressing against its front panel while tightening the hex-nut latch with an 8 mm hex-ball driver.

When removing a clock source module, disconnect any cable connected to the rear panel *EXT REF* port.

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3

Operating Guide

Operating Guide

Introduction

The method of selecting the clock frequency and the display presented to the user differs, depending upon whether the clock module is configured as a slave, or a master. There are separate procedures given here for setting clock frequency in modules configured as a slave or master; refer to the appropriate one for your clock source.

If you are unsure how your clock source is configured refer to the procedure titled *How to Check Your Clock Source HP-MSIB Address* on page 3-5.

Note

Clock Source modules are normally shipped from the factory configured as slaves.

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To Set Up Clock Frequency and Step Size (Clock Source a slave)

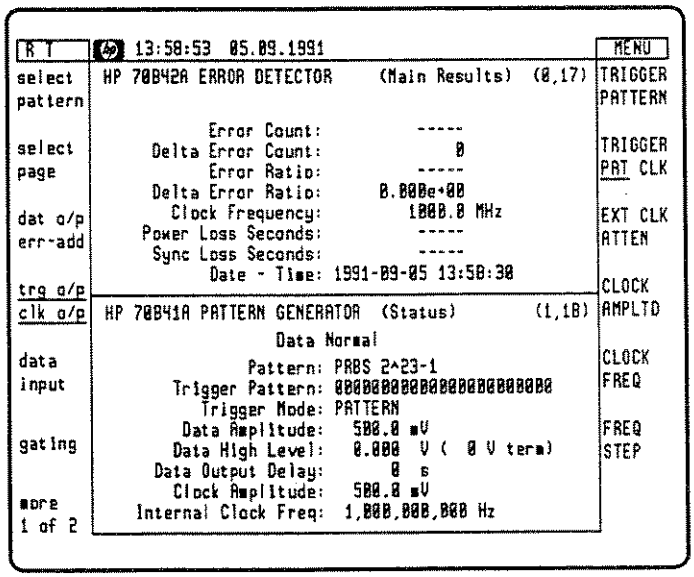
In the following procedure it is assumed that the clock source is installed in an HP 71600 Series Error Performance Analyzer system, which is configured in master/slave format. See page 3-6 for an example of master/slave configuration in such a system.

It is assumed that the display used is an HP 70004A.

To Set Up Clock Frequency

Procedure

1. Press (DISPLAY), then press the `NEXT INSTR` right-menu softkey until the error detector, or pattern generator or both are selected.
2. Press the (MENU) hardkey.
3. Select the `trg o/p, clk o/p` left-menu softkey. The right-menu changes to reveal `CLOCK FREQ` and `FREQ STEP` softkeys as shown below (ignore the module status given in the center of the display).



4. Select the `CLOCK FREQ` right-menu softkey.
5. There are three methods of selecting clock frequency as follows:
   - Use the Display knob.
   - Use the ▲,▼ keys (increments or decrements frequency by a preset amount).
   - Enter a number via the keypad, then select a unit of frequency from the right menu.

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To Select Frequency Step Size

The frequency step size is the amount that the clock frequency is incremented or decremented when using the ▲,▼ keys or display knob.

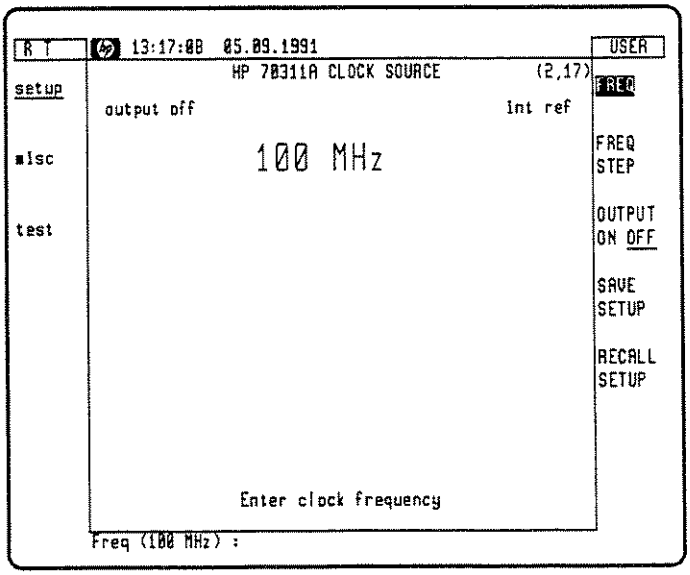
6. Select FREQ STEP.
7. Enter the frequency step using the numeric keypad, then select one of the units of frequency from the right-menu.

To Set Up Clock Frequency and Step Size (Clock Source a Master)

Use the following procedure when your clock source is configured as a master. It is assumed that the display used is an HP 70004A.

Procedure

1. At power-on the display will show the module/instrument selected before power-down. If the clock source is not displayed, press (DISPLAY), then press the NEXT INSTR right-menu softkey until the clock source is selected.
2. Press the (MENU) hardkey to display the clock source softkeys.
3. The display should look similar to the following when setup is selected.



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To Set Up Clock Frequency

4. Select FREQ (key shown in inverse video when selected). There are three methods of selecting clock frequency as follows:
   - Use the Display R.P.G knob.
   - Use the ▲,▼ keys (increments or decrements frequency by a preset amount).
   - Enter a number via the keypad, then select a unit of frequency from the right menu.

To Select Frequency Step Size

The frequency step size is the amount that the clock frequency is incremented or decremented when using the ▲,▼ keys or display knob.

5. Select FREQ STEP.
6. Enter the frequency step using the numeric keypad, then select one of the units of frequency from the right-menu.

Switch Clock Output On/Off

7. To switch the CLOCK OUTPUT ON, set the OUTPUT ON OFF softkey to ON.

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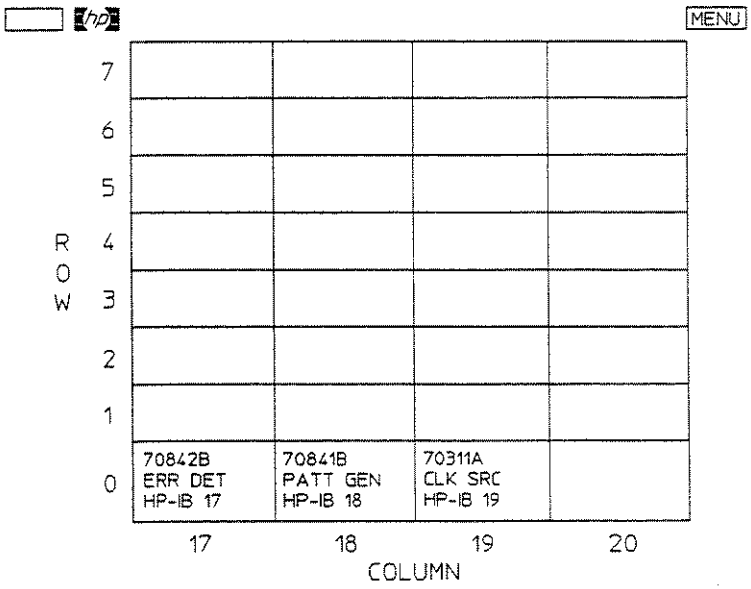
How to Check Your Clock Source HP-MSIB Address

In the following procedure it is assumed that you are using an HP 70004A display.

Procedure

1. Press the DISPLAY hardkey.
2. Select the left-menu `Address Map` softkey.
3. Rotate the display knob clockwise and observe the *Row Address* of each module in your system. If each module (ERR DET, PAT GEN or CLK SRC) row address is 0, the system is configured for master/master operation, as shown below.



Master/Master Configuration

If the error detector module is the only module on row 0 (except for the HP 70004A display) the system is configured for master/slave operation. An example of master/slave address setup is as follows.

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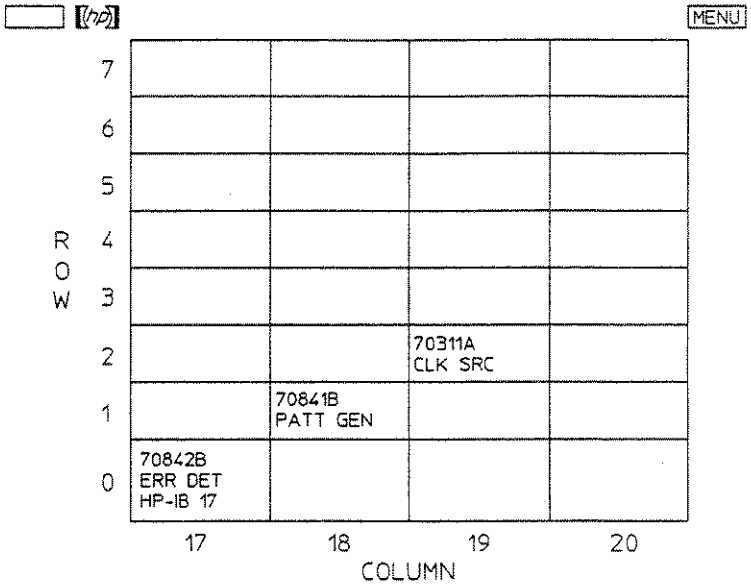
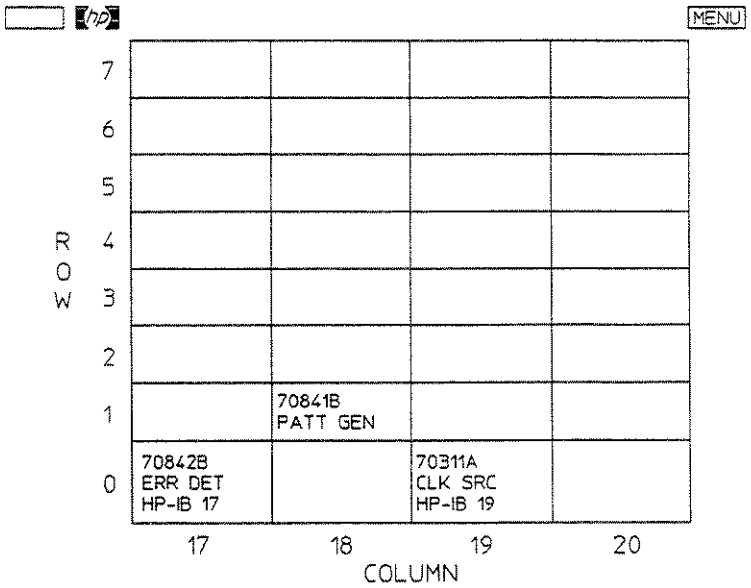


Master/Slave Configuration



Master/Slave/Master Configuration

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To Assign Both Display and Keyboard to the Clock Source

Why Should I Need to Do This?

To gain access to all clock source softkeys in order to perform calibration, performance tests or diagnostics when the clock source is configured as a slave.

Further Explanation

Your clock source may be configured as a master or a slave, depending upon your application or system, a brief description of each follows:

- When configured as a master the clock source operates as an independent instrument, and all primary softkey menus `setup`, `misc`, `test` may be accessed by the user; there is therefore no need to use the following procedure. To access the clock source simply press (DISPLAY), then the `NEXT INSTR` softkey until the clock source status is displayed.
- When configured as a slave the clock source is setup via its master (Error Detector or Pattern Generator in an HP 71600 Series system), and only the `CLOCK FREQ` and `FREQ STEP` softkeys are visible; accessed via the `trg o/p, clk o/p` softkey. To gain access to all softkeys while configured as a slave, you must assign both display and keyboard to the clock source. The following procedure explains how to assign both display and keyboard to the clock source.

Procedure

To Assign the Display and Keyboard to the Clock Source

1. Press (DISPLAY) then `Address Map`.
2. Rotate display knob clockwise until the green box is resting on the same column as the clock source.
3. Press `ADJUST ROW`. Using the display knob move the green box up to rest on the `CLK SRC`.
4. Press the `ASSIGN BOTH` softkey. This assigns both the keyboard and display exclusively to the clock source.
5. Press (MENU), the display should now look similar to the following:

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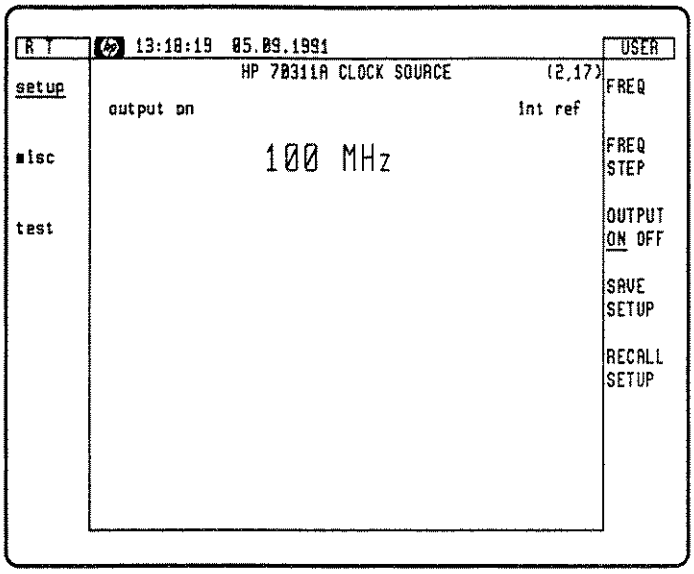

Clock Source Status

6 You can now access the clock source `setup`, `misc` and `test` softkey menus.

7. To return the keyboard and display to independent operation press (DISPLAY), then `NEXT INSTR`. The instrument status displayed will be the first master on row 0 of the address map (excluding the HP 70004A display) moving from left to right from column 0 to column 31.

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Using an HP 70310A Precision Freq Ref with Your Clock Source

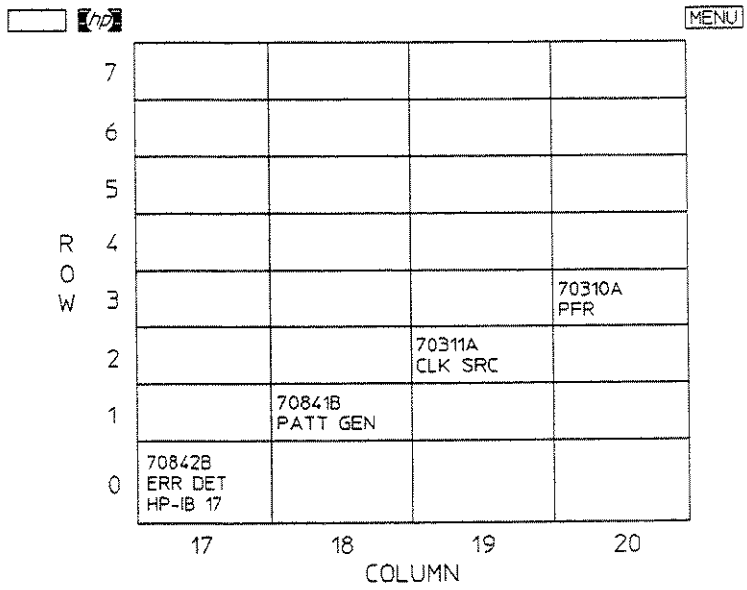
Introduction

The HP 70310A may be used in applications where a more accurate, clock frequency is required.

Procedure

1. Connect a suitable cable from the HP 70310A rear panel 10 MHz O/P port to the clock source rear panel EXT REF I/P port.
2. Set the HP 70310A HP-MSIB address switches to: Row 3; Column 20.

The following figure illustrates an HP 71600 Series Error Performance Analyzer System with an HP 70310A Precision Freq Ref, configured in master/slave format.



HP 70310A in Master/Slave Configuration

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4

Softkey Descriptions and Menu Maps

Softkey Menus

Introduction

Clock source functions/parameters are setup via softkeys on either side of the display. This chapter explains the structure of softkey menus, gives graphic representations of softkey functions, and explains how the softkeys visible to the user differ depending upon module configuration.

How Softkeys are Structured and Displayed

The display has two columns of seven keys, one on either side of the display window. Softkey labels are assigned to keys and change as new menus or functions are selected.

The left-menu softkeys known as *PRIMARY* softkeys are used to select major functions or groups of functions. The right-menu softkeys are known as *SECONDARY* softkeys and are used to select functions or parameters relevant to the PRIMARY softkey currently selected.

Softkey Notation

- Keys labelled by lower-case text are *navigation* keys which give access to lower level menus.
- Keys labelled by upper-case text are *configuration* keys which cause an attribute of the instrument to change.
- Some keys are *toggle* keys (for example OUTPUT ON/OFF). These keys cause an attribute to toggle between one of two states. The current state is indicated by underlining.

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User Softkeys in Master and Master/Slave Configuration

The range of softkeys visible to the user differ depending on whether the clock source is configured as a slave (in perhaps an HP 71600 Series Error Performance or Pattern Generator system), or as an independent master. Information on master and master/slave concepts is given in the HP 71600 Series of Gbit/s Testers Installation and Verification Manual.

Clock Source Softkeys in Slave Configuration

When the clock source is configured as a slave, softkeys are accessed using the `trg o/p, clk o/p` menu (in HP 71600 Series systems) and only `CLOCK FREQ` and `FREQ STEP` clock functions are available. See Figure 4-1.

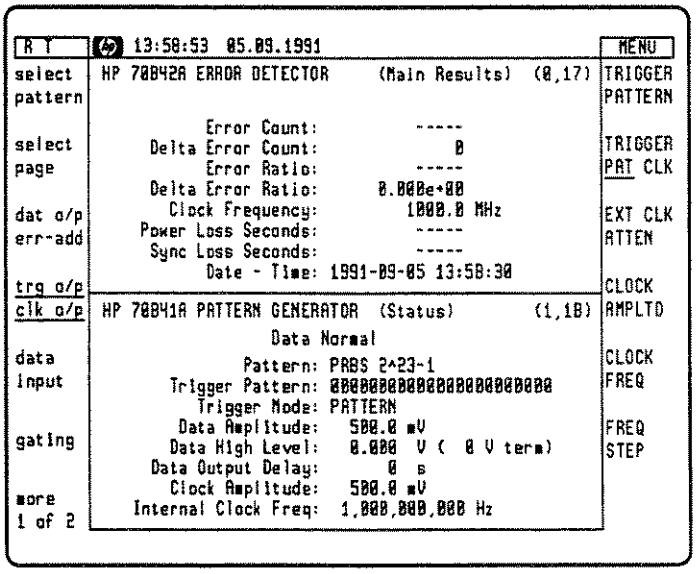

Figure 4-1. Clock Source Softkeys in Slave Configuration

To access the full range of clock source softkeys in order to perform instrument performance tests, calibration or diagnostics, you must either configure the clock source as a master, or assign both display and keyboard to the clock source. Refer to chapter 3 for advice on how to assign keyboard and display to the clock source.

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Clock Source Softkeys in Master Configuration

When configured as a master all clock source functions may be accessed by the three primary softkey menus `setup`, `misc` and `test`. An example is given below.

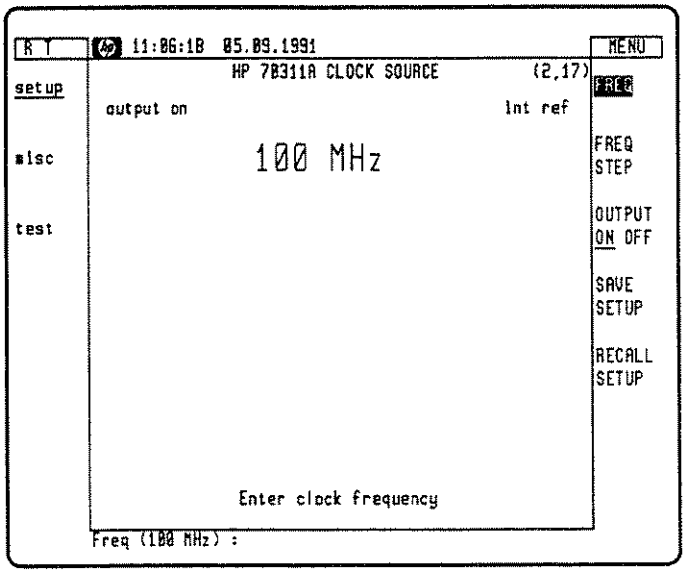

Figure 4-2. Clock Source Softkeys in Master Configuration

Note

The `setup`, `misc` and `test` softkey menus are explained in the following pages.

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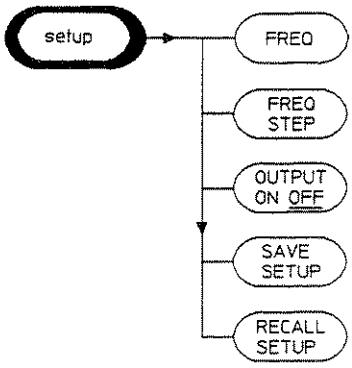
setup menu



Description

The `setup` softkey enables five softkeys in the right-menu, which allow the clock frequency and frequency step to be set, the clock output to be switched on or off, and the current instrument state to be saved into one of ten storage registers, to be recalled later.

`FREQ`

Alters the clock frequency. The message *Enter clock frequency* is shown on the bottom of the display window and the message *Freq (current value):* is shown on the bottom line of the display screen. You can set the clock frequency in the following three ways:

- Use the display RPG knob to adjust clock frequency.
- Increment or decrement clock frequency by a set amount using the ▲,▼ keys.
- Use the display numeric keypad to set the clock frequency. When a numeric key on the keypad is hit, the right menu shows the units keys (GHz, MHz, kHz, Hz) and the `CLEAR` softkey. Enter the desired number then select a unit of frequency.

`FREQ STEP`

The clock frequency may be incremented or decremented by a fixed amount (or step). The `FREQ STEP` key enables you to define the size of this fixed amount or step.

Press `FREQ STEP`, (shown in inverse video when selected). Enter step size using the numeric keypad, then select a unit of frequency from the right-menu.

`OUTPUT ON/OFF`

Switches the clock source RF output on or off. The output status on the display window is updated as the key is toggled.

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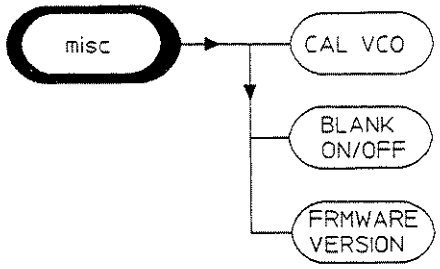
`SAVE SETUP` Enables the user to store the current clock source configuration in one of ten storage registers. This includes clock frequency, step size, output blanking state and whether the clock output is switched on or off.

Press the `SAVE SETUP` softkey; enter the *setup* number using the numeric keypad, then press the `ENTER` softkey.

`RECALL SETUP` Recalls the clock configuration from one of ten storage registers.

Press the `RECALL SETUP` softkey; enter the *setup* number using the numeric keypad, then press the `ENTER` softkey.

misc menu



Description

The `misc` menu allows the user to call up various miscellaneous instrument functions. The `misc` right menu has three softkeys. These are:

`CAL VCO` Causes the clock source to do a self calibration of the VCO loop. This process takes about five minutes to complete. While the calibration is in progress, the message *Calibrating VCO* is displayed and a progress marker moves across the screen from left to right then back again. An audible beep is sounded when the calibration is completed. No other instrument action is allowed during calibration.

`BLANK ON/OFF` Turns the RF output blanking ON or OFF. With blanking ON, the RF output is temporarily turned off during changes in frequency. With blanking OFF, the RF output remains on during frequency changes. Note that there may be indeterminate transients in output frequency and level while a new frequency value is being set.

`FMWARE REV` Shows the instrument firmware revision. A message is displayed in the format: *Firmware revision:A.01.01*

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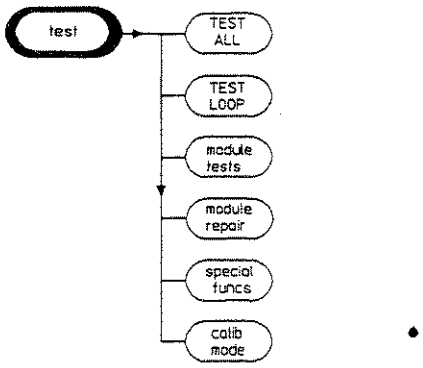
test menu



Description

The selftest features of the clock source are controlled by a hierarchy of test menus accessed using the six softkeys shown above. The module repair, special function, and calibration mode menus are only for use by qualified service personnel. Further information on these keys is given in the HP 70311A/70312A Service Manual

Error Messages

The grouped tests (TEST ALL and TEST LOOP) and individual module tests run automatically until completed. If they run successfully a *No error* message is shown on the bottom line of the display.

If an error occurs, an error message is shown on the bottom line of the display and an audible bleep is sounded. Hardware errors are grouped into non-fatal and fatal errors. For non-fatal errors, the test continues to run.

Top Level Menu

`TEST ALL` — Runs a group of module tests in a defined order. The tests are: CPU, MEMORY, MFPC, MSIB, HP-IB, DAC, PSU, MOD I/F, REF OSC, VCO, FRAC N, RF O/P and SWEEP.

`TEST LOOP` — Turns the test loop mode ON or OFF. When the instrument is in test loop mode a sequence of tests is run continuously until the loop mode is turned off. The tests which are run are:
CPU, MEMORY, MFPC, MSIB, HPIB, DAC, PSU, MOD I/F, REF OSC, VCO, FRAC N, RF O/P, and SWEEP tests.
If any error occurs during the test, an error message is displayed and an audible bleep is sounded. No further tests are run, but the `TEST LOOP` key is still selected.

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module tests There are three pages of softkeys joined by **more** keys for performing individual module tests. The module test selected is displayed in inverse video and a message *Busy testing (module name)* is displayed. The module tests are as follows:

CPU Tests the 68000 Processor.

MEMORY Tests the RAM, ROM and EEROM memories.

MFPC Tests the multi-function Peripheral chip.

MSIB Tests the MSIB interface chip.

HPIB Tests the HP-IB interface chip.

DAC Tests the analog measurement circuitry on the processor board.

PSU Checks the power supply voltages.

MOD I/F Tests the module interfaces on the processor board, for example the serial and parallel interfaces.

REF OSC Tests the reference oscillator module.

VCO Tests the voltage controlled oscillator module.

FRAC N Tests the fractional N divider module.

RF O/P Tests the RF output board.

SWEEP Sweeps the clock source frequency from 515 to 1029 MHz in 1 MHz steps, and checks that the frequency locked loop stays in lock at each frequency.

LED ON/OFF Causes a rotating test pattern to be displayed on the front panel LEDs. This menu key is a toggle key which alternately turns the test on and off. Note that the test is not included in the power-on test because it conflicts with standard power-on LED settings.

TEST STATUS Calls up a display of the status of all the individual module tests, as illustrated by the following figure. The test status values are:

- good. . . . . the test has run successfully.
- bad. . . . . .the test has failed.
- unknown. . . . . .the test has not yet been run.

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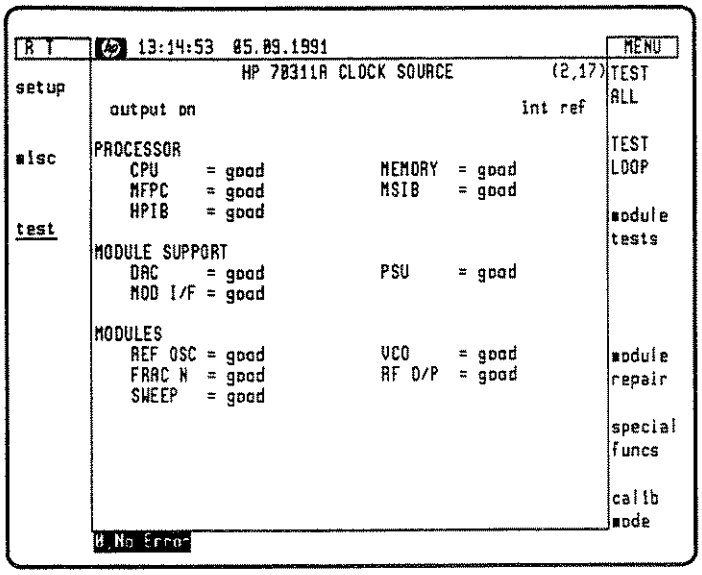

Special Service Only Keys

The `module repair`, `special funcs` and `calib mode` softkeys are intended for use by qualified service personnel, and may only be accessed by keying in the correct password. Information on these keys is given in the HP 70311A/70312A Service Manual.

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5

Programming Information

Introduction

This document defines the remote interface specification for the HP 70311A and HP 70312A clock sources. It covers the HP-IB/HP-MSIB commands, the device status reporting structure, error messages and the power-on/reset conditions. As far as interface commands are concerned, the two instruments are identical.

References

All commands are assumed to be compatible with the following documents :

- ANSI/IEEE std 488.2-1987 - IEEE Standard Codes, Formats, Protocols and Common Commands.
- ANSI/IEEE std 488.1-1987 - IEEE Standard Digital Interface for Programmable Instrumentation.
- Standard Commands for Programmable Instruments (SCPI) Version 1991.0 May 1991.

IEEE Std 488.2-1987 Device Capability

Device Interface Functions

IEEE 488.1 Interface Functions

The following Interface functions, as defined in IEEE std 488.1-1987, are implemented :

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Interface function	Identification	Description
Source Handshake	SH1	complete capability
Acceptor Handshake	AH1	complete capability
Talker	T6	basic talker, serial poll, unaddress if MLA
Extended Talker	TE0	no capability
Listener	L4	basic listener, unaddress if MTA
Extended Listener	LE0	no capability
Service Request	SR1	complete capability
Remote Local	RL1	complete capability
Parallel Poll	PP0	no capability
Device Clear	DC1	complete capability
Device Trigger	DT0	no capability
Controller	C0	no capability
Electrical Driver Characteristics	E1	open collector drivers

HPIB Address Outside Legal Range

If the module is configured as a row-address zero device then it is illegal to set the column address (that is, the HPIB address) to 31. As hardware switches are used to set these addresses, it is possible to set an illegal address. In this case, the device will generate an HP-MSIB error.

HPIB Address Change

The user can change the HPIB address either by module hardware switches or from the DISPLAY menu. Hardware switch changes are only recognised at power-on. DISPLAY menu changes are recognised immediately.

Device Setting at Power-On

All device settings are preserved through a power off/on cycle.

Message Exchange Control Protocol

Multiple <RESPONSE MESSAGE UNITS>

There are no <QUERY MESSAGE UNITS> that return more than one <RESPONSE MESSAGE UNIT>.

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Generation of Response Message Data

The generation of the bytes of a <RESPONSE MESSAGE> always occurs at the time when the query message is parsed, rather than delaying the generation until the response is read.

Parser Errors

When the parser detects a Command Error the device does not discard any prior parsable elements of the same <PROGRAM MESSAGE>.

Coupled Commands

There are no coupled commands in the device.

Functional Elements Used

The complete list of functional elements defined in IEEE 488.2 is shown below together with statements showing which elements are used in this device.

<PROGRAM MESSAGE>	used in this device
<PROGRAM MESSAGE TERMINATOR>	used in this device
<PROGRAM MESSAGE UNIT>	used in this device
<PROGRAM MESSAGE UNIT SEPARATOR>	used in this device
<COMMAND MESSAGE UNIT>	used in this device
<QUERY MESSAGE UNIT>	used in this device
<COMMAND PROGRAM HEADER>	used in this device
<PROGRAM HEADER SEPARATOR>	used in this device
<PROGRAM DATA>	used in this device
<PROGRAM DATA SEPARATOR>	used in this device
<QUERY PROGRAM HEADER>	used in this device
<CHARACTER PROGRAM DATA>	used in this device
<DECIMAL NUMERIC PROGRAM DATA>	used in this device
<NON-DECIMAL NUMERIC PROGRAM DATA>	not used in this device
<ARBITRARY BLOCK PROGRAM DATA>	not used in this device
<EXPRESSION PROGRAM DATA>	not used in this device
<SUFFIX PROGRAM DATA>	used in this device
<STRING PROGRAM DATA>	not used in this device
<COMPOUND COMMAND PROGRAM HEADER>	used in this device

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Device Talking Formats

Device-to-Device Messages

All the device-to device message transfer traffic conforms to IEEE 488.2 conventions.

Common Commands and Queries

The IEEE 488.2 common commands which are implemented by the device are listed below. A fuller description of the device's response to these commands and queries is given in pages 5-7 and 5-8.

IEEE Mandatory Commands

The following IEEE 488.2 mandatory commands are implemented :

*CLS Clear Status Command

*ESE Standard Event Status Enable Command

*ESE? Standard Event Status Enable Query

*ESR? Standard Event Status Register Query

*IDN? Identification Query

*OPC Operation Complete Command

*OPC? Operation Complete Query

*RST Reset Command

*SRE Service Request Enable Command

*SRE? Service Request Enable Query

*STB? Read Status Byte Query

*TST? Self-Test Query

*WAI Wait-to-Continue Command

IEEE Optional Commands

The following IEEE 488.2 optional commands are implemented :

*CAL? Calibration Query

*OPT? Option Identification Query

*PSC Power-on Status Clear Command

*PSC? Power-on Status Clear Query

*RCL Recall Command

*SAV Save Command

Command overlapping

The device does not implement overlapped commands; all commands are executed sequentially.

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HP-IB/HP-MSIB Commands

Notes on Terms

<freq term> When found in a command, indicates that "Hz", "kHz", "MHz", "GHz" or no termination is required in the command statement. If the command statement is not terminated, then "HZ" is assumed.

<NRf> When found in a command, indicates that an ASCII representation of a number is required in the command statement. The number may be integer or floating point, and may include a decimal exponent. A numeric suffix may be added to <NRf> when a command contains more than one numeric parameter.

<boolean> When found in a command, the following boolean values are recognized : 1 | 0 | ON | OFF

Caution No HP-IB activity should take place within 15 seconds of system power up, as this will effect the system power up routine and may result in system hang up.

Frequency Subsystem

[SOURce:] FREQuency

[:[CW | FIXed]]? [MINimum | MAXimum | DEFault]

Query the RF output frequency, or MIN/MAX allowable values of frequency, or the default frequency.

[:[CW | FIXed]] <NRf> [<freq term>] | UP | DOWN | MINimum | MAXimum | DEFault

Set the RF output frequency to a specified value, or UP/DOWN a frequency step, or set to MAX/MIN allowable frequency, or set to the default frequency. The *RST value and default values are both 100 MHz.

:STEP

[:INCRement]? [MINimum | MAXimum | DEFault]

Query the step size for RF frequency steps, or MAX/MIN allowable step sizes, or the default step size.

[:INCRement] <NRf>[<freq term>] | MINimum | MAXimum | DEFault

Set the STEP size for RF frequency to a specified value, or to the MAX/MIN step size, or to the default step size.

The *RST and default values of step size are both 1MHz.

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Output Subsystem

OUTPut

STATe?

Query the RF output power state.

[:STATe] <boolean>

Turns the RF output ON or OFF. The *RST value is ON.

:BLANk?

Query the RF output blanking state.

:BLANk <boolean>

Turns the RF output blanking ON or OFF. The *RST value is OFF. With blanking ON, the RF output is temporarily turned off during changes in frequency. With blanking OFF, the RF output remains on during frequency changes. Note that there may be indeterminate transients in output frequency and level while a new frequency value is being set.

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IEEE 488.2 Common Commands and Queries

***CAL?** **Self calibration query**

Causes the HP 70311A to perform a calibration of the instrument's internal VCO circuitry. An integer error code is returned when the calibration is completed. An error code of zero indicates successful calibration. If errors are present one or more specific error messages are put into the error message queue. This command is equivalent to activating the CAL VCO command from the display subsystem.

***CLS** **Clear status command**

Clears the status register and associated status data structures summarized in the Status Byte, such as the Event Status Register. Clears all event registers and the error message queue.

***ESE** **<NRf> Event status enable command**

Sets the Standard Event Status Enable Register.

***ESE?** **Event status enable query**

Queries the Standard Event Status Enable Register.

***ESR?** **Event status register query**

Queries the Standard Event Status Register.

***IDN?** **Identification query**

Returns an identification string which is 4 fields separated by commas.

Field 1 : Is always HEWLETT-PACKARD
Field 2 : Is the model number, 70311A.
Field 3 : Is the serial number field. The 70311A returns a value of 0.
Field 4 : Is the firmware version number, in the format : A.01.01.
For example : HEWLETT-PACKARD,70311A,0,A.01.01

***OPC** **Operation complete command**

The OPC bit is set in the Standard Event Status Register but no other operation is performed. Note that the instrument does not implement overlapped commands.

***OPC?** **Operation complete query**

Always causes an ASCII 1 to be returned. Note that the instrument will not accept a second HP-IB command until the previous command has completed execution. The *OPC? command can therefore be used to indicate when a previous command has been fully completed, for example when a new frequency has been set and the output has settled.

***OPT?** **Option identification query**

No options are currently defined. The instrument returns the single character 0.

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***PSC** **<NRf> Power-on status clear command**

Sets or clears the power-on status clear flag. A non-zero value of <NRf> sets the flag and a zero value clears the flag.

***PSC?** **Power-on status clear query**

Queries the power-on status clear flag.

***RCL** **<NRf> Recall instrument state**

Recalls the instrument state which was stored in the specified register number. The parameters recalled are : frequency, frequency step, RF output state and RF output blanking state. The HP 70311A has 10 available storage registers, numbered 0 to 9.

***RST** **Reset command**

Causes the HP 70311A to do an instrument preset. Sets all operating parameters to the known states listed on page A-5 (Instrument reset). It does not affect the status reporting information, nor does it clear the error message queue, and does not affect the contents of the 10 storage registers.

***SAV** **<NRf> Save instrument state**

Saves the current instrument state in the specified register number. The parameters saved are : frequency, frequency step, RF output state, and RF output blanking state. The HP 70311A has 10 available storage registers, numbered 0 to 9.

***SRE** **<NRf> Service request enable command**

Sets the Service Request Enable Register.

***SRE?** **Service request enable query**

Queries the Service Request Enable Register.

***STB?** **Read status byte query**

Queries the HP-IB Status Byte.

***TST?** **Self-test query**

Causes the HP 70311A to perform internal instrument level tests and returns an integer error code. An error code of zero indicates no failures, other numbers indicate an error. In addition, one or more specific error messages are put into the error message queue. A list of specific error codes is defined in appendix B. This command is equivalent to activating the TEST ALL function from the display subsystem.

The tests which are run are : cpu, memory, mfpc, msib, hpib, D/A converter, power supply, module interfaces, reference oscillator, fractional N divider, VCO, RF output, sweep and LED tests.

***WAI** **Wait-to-continue command**

The command is recognized by the instrument but no operation is performed. Note that the instrument does not implement overlapped commands.

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Reference Oscillator Subsystem

[SOURce:] ROSCillator

:SOURce? A SOURce? query returns the status of the reference source: INT, EXT or NO that is (internal, external or no reference source). The query reply is equivalent to the *int/ext/no ref* status display on the display subsystem. Note that the reference source cannot be selected under program control.

:IDN? Returns an identification string for the slaved external Precision Frequency Reference (PFR), if fitted. The string format is identical to that for the *IDN? command.
For example : HEWLETT-PACKARD,70310A,0,A.01.01
If a PFR is not fitted, a null string is returned and a Slave not present error is put into the error message queue.

Calibration Subsystem

CALibration

[:ALL]? Causes the HP 70311A to perform a calibration of the instrument's internal VCO circuitry. An integer error code is returned when the operation is completed. An error code of zero indicates successful calibration. If errors are present one or more specific error messages are put into the error message queue. This command is equivalent to activating the CAL VCO command from the display subsystem.

Status Subsystem

STATus

:OPERation	(Operational Status register)
[:EVENt]?	Return contents of event register
:CONDition?	Return contents of condition register
:ENABle <NRf>	Set register enable mask
:ENABle?	Return contents of event enable register
:PTRansition <NRf>	Set positive transition filter
:PTRansition ?	Return contents of positive transition filter
:NTRansition <NRf>	Set negative transition filter
:NTRansition ?	Return contents of negative transition filter
:QUEStionable	(Questionable Status register)
[:EVENt]?	Return contents of event register
:CONDition?	Return contents of condition register
:ENABle <NRf>	Set register enable mask
:ENABle?	Return contents of event enable register
:PTRansition <NRf>	Set positive transition filter
:PTRansition ?	Return contents of positive transition filter
:NTRansition <NRf>	Set negative transition filter
:NTRansition ?	Return contents of negative transition filter

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:FREQuency	(Frequency Status register)
[:EVENt]?	Return contents of event register
:CONDition?	Return contents of condition register
:ENABle <NRf>	Set register enable mask
:ENABle?	Return contents of event enable register
:PTRansition <NRf>	Set positive transition filter
:PTRansition ?	Return contents of positive transition filter
:NTRansition <NRf>	Set negative transition filter
:NTRansition ?	Return contents of negative transition filter

:CALibration	(Calibration Status register)
[:EVENt]?	Return contents of event register
:CONDition?	Return contents of condition register
:ENABle <NRf>	Set register enable mask
:ENABle?	Return contents of event enable register
:PTRansition <NRf>	Set positive transition filter
:PTRansition ?	Return contents of positive transition filter
:NTRansition <NRf>	Set negative transition filter
:NTRansition ?	Return contents of negative transition filter

:HARDware	(Hardware Status register)
[:EVENt]?	Return contents of event register
:CONDition?	Return contents of condition register

:PRESet The PREset command configures the SCPI and device-dependent status reporting structure, such that device-dependent events are reported at a higher level through the mandatory part of the status-reporting mechanism.

This means that:

1. Operational Status Register and Questionable Status Register - the enable register is set to 0's and the transition filters are set to recognize only positive transitions.
2. Frequency Status Register, Calibration Status Register, Hardware Fail Status Register - the enable register is set to 1's and the transition filters are set to recognize only positive transitions.
3. Status Byte Register and Standard Event Status Register - these registers are not affected.

System Subsystem Commands

SYSTem

:ERRor? Reads an error from the system error queue. If the error queue is empty the instrument returns with 0, No error. If there is more than one error, the instrument returns with the first one in its error queue. Subsequent responses to ERR? continue with the error queue until it is empty. The format of error messages is :

<error number>,"<error description>"

For example: -222, "Data out of range"

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:PRESet Causes the HP 70311A to do an instrument preset. Sets all operating parameters to the known states listed on page A-5 (Instrument reset). It does not affect the status reporting information, nor does it clear the error message queue, and does not affect the contents of the 10 storage registers.

:VERSion? Returns a formatted numeric value corresponding to the SCPI version number with which the instrument complies. The response is in the form YYYY.V where YYYY represents the year and V represents an approved revision number for that year. If no approved revisions are claimed then the number shall be 0. For example, 1990.0

Test Subsystem

All the tests in this section return an integer error code. A returned value of 0 indicates that the test completed successfully. If an error occurs, an error number is returned and a message is put into the error message queue.

After a test, the instrument restores the previously set values of frequency and output state.

TEST

:MODule

:CPU?	Tests the 68000 processor.
:MEMory?	Tests the RAM and ROM memories.
:MFPC?	Tests the multi-function peripheral chip.
:MSIB?	Tests the MSIB interface chip.
:HPIB?	Tests the HP-IB interface chip.
:DAC?	Tests the D/A converter chip on the processor board.
:PSU?	Checks the power supply voltages.
:MINTerface?	Tests the module serial and parallel interfaces on the processor board.
:ROSCillator?	Tests the reference oscillator module.
:VCO?	Tests the voltage controlled oscillator module.
:NF?	Tests the fractional N divider module.
:RFOP?	Tests the RF output board.
:SWEEP?	Sweeps the instrument frequency from 515 to 1029 MHz in 1 MHz steps and checks for any synthesizer loop errors at each frequency.
:LED <boolean>	Turns the front panel LED test ON or OFF. The test causes a rotating "1" pattern to be displayed on the LEDs.

:LOOP?

Queries if the instrument is in test loop mode. Note that if this command is issued while the MEMORY test is running, the response will be delayed until the end of the MEMORY test.

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:LOOP <boolean>

Turns the test loop mode ON or OFF. When the instrument is in test loop mode a sequence of tests is run continuously until the loop mode is turned off or an error occurs. The tests which are run are : CPU, MEMORY, MFPC, MSIB, HPIB, DAC, PSU, MODIF, ROSC, VCO, NF, RFOP and SWEEP tests.

If any error occurs during the test, an error message is put into the error message queue. No further tests are run and test loop mode is automatically turned off.

As the :LOOP? command could take a long time to respond to, it is recommended that the user checks for errors during the loop test by either of the following:
(a) serial poll the instrument status byte
(b) program the instrument so that it generates an SRQ signal on error.

Command Overlapping and Timing

The instrument does not implement command overlapping. Each command must run to completion before the next command will be accepted. The *OPC, *OPC? and *WAI commands are, however, recognized by the instrument. See the description of the *OPC command for further details.

The instrument accepts one message containing several commands, separated by semicolons. The commands are executed sequentially. The response message, if any, is not returned until after the last command in the message has been executed.

The user should be aware that some commands take a long time to execute and generate a response. These commands and their approximate timings are listed below.

*CAL?	5 minutes 5 seconds
*TST?	2 minutes 40 seconds
CAL:ALL?	5 minutes 5 seconds
TEST LOOP?	60 seconds (maximum)
TEST:MOD:MEM?	60 seconds
TEST:MOD:VCO?	6 seconds
TEST:MOD:NF?	8 seconds
TEST:MOD:SWEEP?	1 min 6 seconds

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Device Status Reporting

The device status reporting structure is shown in figure 5-1 (page 5-16). The register model follows the structure described in *IEEE 488.2*, section 11. The registers and their bit functions are defined below.

Status Byte Register

The Status Byte Register contains the instrument's single-bit summary messages as defined in *IEEE 488.2* section 11.

0 - HWF - Hardware Fail Register summary bit.
1 - SLV - Slave instrument summary bit.
3 - QSR - Questionable Status Register summary bit.
4 - MAV - Message Available summary bit.
5 - ESB - Standard Event Status Register summary bit.
6 - RQS - Request Service bit.
7 - OSR - Operational Status Register summary bit.

Standard Event Status Register

The Standard Event Status Register contains the instrument's standard event status as defined in *IEEE 488.2* section 11.5.

0 - OPC - Operation Complete
1 - RQC - Request Control
2 - QYE - Query Error
3 - DDE - Device Dependent Error
4 - EXE - Execution Error
5 - CME - Command Error
6 - URQ - User Request
7 - PON - Power On

Operational Status Register

The Operational Status Register contains conditions which are part of the instrument's normal operation. Note that this register can be read if the instrument is calibrating on power-up or if calibration has been initiated from the front panel. The register cannot be read if the user has initiated calibration remotely, by a *CAL? or CAL:ALL? command.

0 - CAL - The instrument is currently performing a calibration.
1 - TST - The instrument is currently performing a self-test or calibration.

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Questionable Status Register

The Questionable Status Register contains conditions which indicate that the instrument's signal is of questionable quality.

5 - QFRE - The frequency of the instrument is of questionable quality, that is the frequency-locked loop is out of lock.
8 - QCAL - The calibration of the instrument is of questionable quality, that is an error has been detected in the instrument's calibration data.

Frequency Status Register

The Frequency Status Register contains conditions which indicate errors during the normal operation of the instrument.

0 - FVCO - Out-of-lock error in the VCO module.
1 - FNF - Out-of-lock error in the Fractional-N module.

Calibration Status Register

The Calibration Status Register contains conditions which indicate errors during the normal operation of the instrument.

0 - CREF - The internal Reference Oscillator is not calibrated.
1 - CLOP - The frequency-locked loop is not calibrated.
2 - COL - The output power level is not calibrated.

Hardware Fail Status Register

The Hardware Fail Status Register contains conditions which indicate errors detected during self-test or power-up of the instrument.

0 - HCPU - Hardware error detected in the microprocessor.
1 - HROM - Hardware error detected in the ROM memory.
2 - HRAM - Hardware error detected in the RAM memory.
3 - HNVM - Hardware error detected in the non-volatile RAM memory.
4 - HEEP - Hardware error detected in the EEPROM memory.
5 - HMFP - Hardware error detected in the Multi-Function Peripheral chip.
6 - HMSI - Hardware error detected in the MSIB interface chip.
7 - HPIB - Hardware error detected in the HP-IB interface.
8 - HDAC - Hardware error detected in the D/A converter.
9 - HPSU - Hardware error detected in the power supply.
10 - HMIF - Hardware error detected in the module interfaces.
11 - HREF - Hardware error detected in the reference oscillator module.
12 - HVCO - Hardware error detected in the VCO module.
13 - HNF - Hardware error detected in the Fractional-N module.
14 - HOUT - Hardware error detected in the RF output module.

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Status Register Initialization

The following table defines the initialization values for all the device status reporting registers. The values are set when the instrument is powered up for the first time. All values are given in hexadecimal code.

Register	Enable Mask	PTransition	NTransition
Status Byte	F9	00	00
Standard Event	FF	FF	00
Operational	01	01	01
Questionable	0120	0120	0000
Frequency	03	03	00
Calibration	07	07	00
Hardware	3FFF	3FFF	0000

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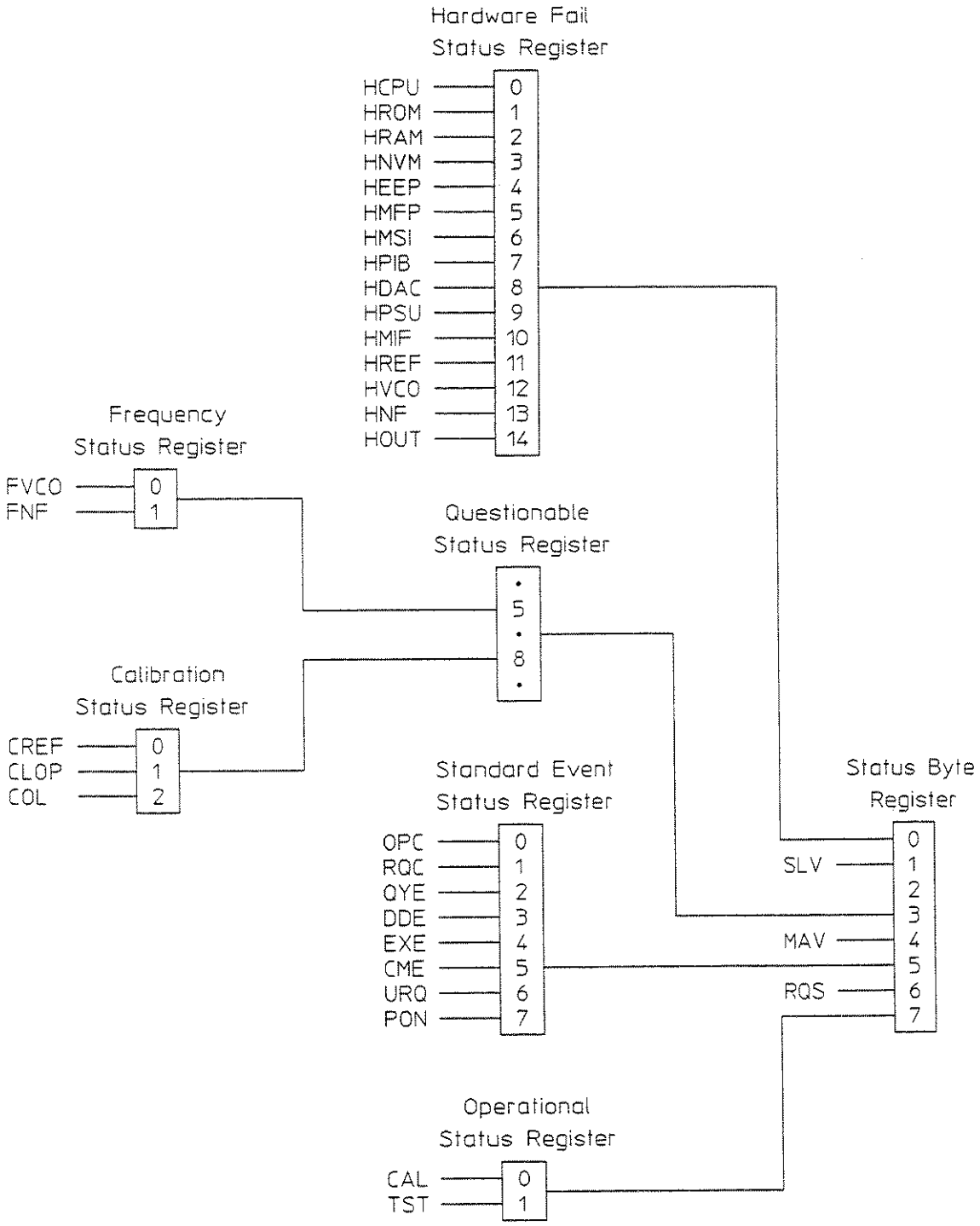

Figure 5-1. TMSL Status Reporting Structure

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6

Performance Tests

Introduction

The procedures in this section test the instrument's electrical performance to the specifications listed in chapter 1. All tests are performed without accessing the interior of the instrument.

Note

If the clock source has been in transit or otherwise stored outwith its normal environment, a 24 hour acclimatization period should be allowed before beginning the performance tests. The clock source should be installed in the MMS System and a 30 minute warm-up period allowed after switch on.

Test Levels

There are two levels of performance testing:

Operational Verification

Provides >90% confidence that the module is operating to its full warranted specification.

Full Performance Test

Ensures that the module is operating to its full warranted specification.

Note

The clock source output must be terminated with a 50 ohm impedance when performing operational verification or performance tests. The equipment specified for these tests meets this requirement.

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Recommended Test Equipment

The test equipment required is listed in Table 6-1. Any equipment that satisfies the critical specifications provided in the table may be substituted for the recommended model(s).

Table 6-1. Recommended Test Equipment

Instrument	Critical Specification	Recommended Model	Use *
Display Unit **	Unique	HP 70004A	PO
Microwave Counter	Frequency Range 10 Hz-3.3 GHz	HP 5343A	PO
Power Meter	−10 to +10 dBm ±0.03 dB; 50 MHz to 3.3 GHz.	HP 435A	PO
Phase Noise Test Set	Unique	HP 3048A	PO
Signal Generator	Phase Noise <-113 dBc 1 kHz offset	HP 8662A	PO
Signal Generator	Phase Noise <-140 dBc 20 kHz offset	HP 8642B	PO
Spectrum Analyzer	Frequency 1 MHz to 7 GHz Sensitivity 110 dBc - 110 dB	HP 8566B	PO
Cable Adaptor	Unique	HP 11500B (1250-0671)	PO

*P=Performance Tests; O=Operational Verification

Performance Test Record

Results of the performance tests may be tabulated on the Performance Tests Record at the end of the procedures. The Performance Tests Record lists all of the tested specifications and their acceptable limits. The results recorded at Incoming Inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

Calibration Cycle

This instrument requires periodic verification of performance depending on its use and environmental conditions. The instrument should be checked using the following performance tests every three years.

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Operational Verification

The following Operational Verification tests give a 90% confidence check that the clock source meets the specifications listed in chapter 1.

Procedure

1. Install the clock source into the display, setup the equipment as shown in Figure 6-1 and switch on.

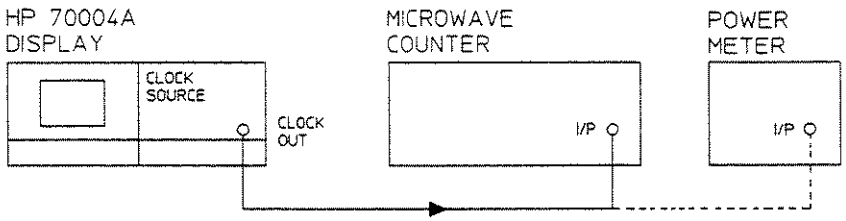

Figure 6-1. Operation Verification Hook-up Diagram

2. The display will carry out some self test routines lasting approximately five seconds (these are explained fully in the HP 70004A operating manual).
3. The front panel leds on the clock source should all be lit for approximately two seconds and then extinguish.

To Assign both Display and Keyboard to the Clock Source

To ensure that all clock source softkeys are accessible to the user, the display and keyboard are assigned exclusively to the clock source as follows:

4. Press (DISPLAY) then `Address Map`.
5. Rotate the display knob clockwise until the green box is resting on the same column as the clock source.
6. Press `ADJUST ROW`. Using the display knob move the green box to rest on the `CLK SRC`.
7. Press the `ASSIGN BOTH` softkey. This assigns both the keyboard and display exclusively to the clock source.

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8. Press (MENU), the display should now look similar to the following:

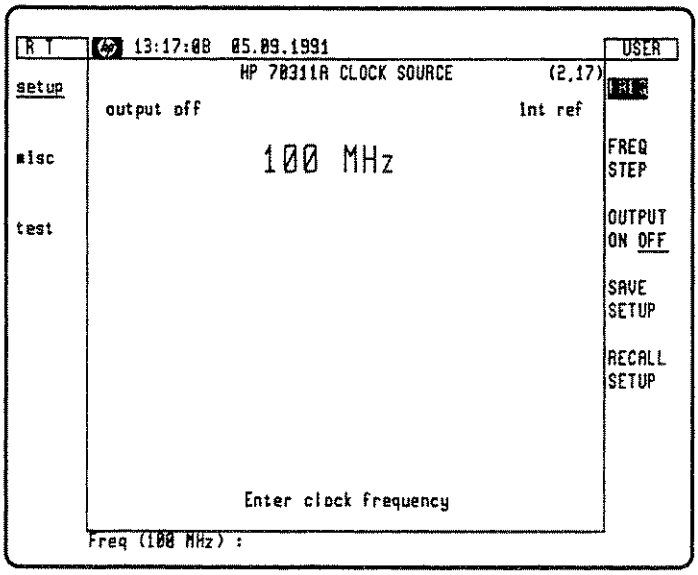

Figure 6-2. Clock Source Status (with `setup` selected)

9. You may now access the clock source `setup`, `misc` and `test` softkey menus.

10. Press the `Test` softkey on the lefthand menu followed by the `test All` softkey on the righthand menu. The clock source now executes a series of module tests, and at completion gives a display similar to Figure 6-3.

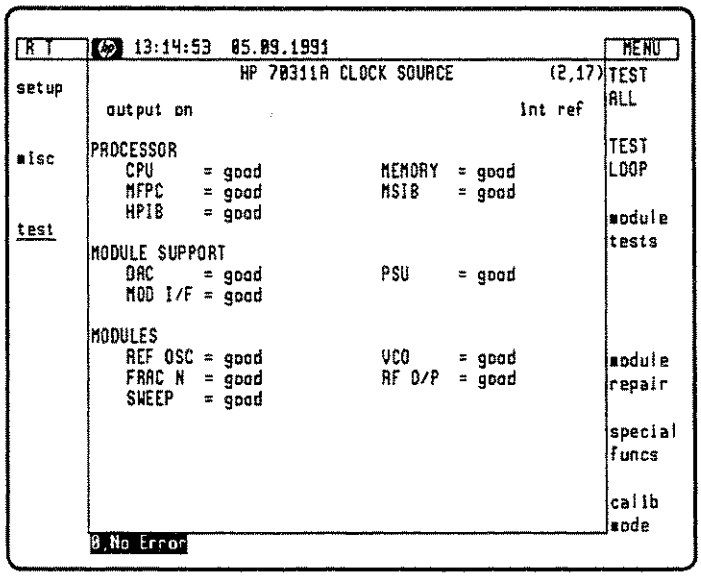

Figure 6-3. Module Tests Display

11. Press the `Setup` softkey on the lefthand menu. The output frequency which appears at the top of the display should correspond with that shown on the frequency meter.

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12. Change the clock source output frequency to 16.09375 MHz and ensure that the reading on the frequency meter is the same.
13. Change the frequency to 1.5 GHz (in the case of the HP 70312A clock source) or 3.3 GHz (in the case of the HP 70311A clock source). Ensure that the reading on the frequency meter corresponds to the value set in the clock source.
14. Connect the power meter in place of the frequency meter. Ensure that the reading is in the range -3 dBm to +3 dBm for the three frequencies given in steps 11, 12 and 13.

Note

If any of the above steps cannot be executed or any of the readings should be incorrect, refer to the Troubleshooting section of the HP 70311A/70312A Service Manual.

This completes the Operational Verification tests.

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Performance Tests

Introduction

The following tests assume that the clock source is installed correctly in the display (HP 70004A recommended) and that both display and keyboard are assigned to the clock source. Steps 4 to 8 of the Operation Verification procedures explain how to assign the display and keyboard to the clock source.

Note

The clock source output must be terminated with a 50 ohm impedance when performing any of the following tests. The equipment specified for these tests meets this requirement.

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LED Test

Procedure

1. Switch on the display.
2. Assign the display and keyboard to the clock source (see steps 4 to 8 of Operation Verification procedure, page 6-4).
3. Check that the display is similar to Figure 6-4, and that no errors are present.

Note

If errors are present in the system a red letter E will appear in the top lefthand box of the display. To identify the source of errors press the DISPLAY hardkey, followed by the right-menu `REPORT ERRORS` softkey. Refer to Appendix A at the end of chapter 5 for advice on error reporting. Correct any errors before proceeding to step 4.

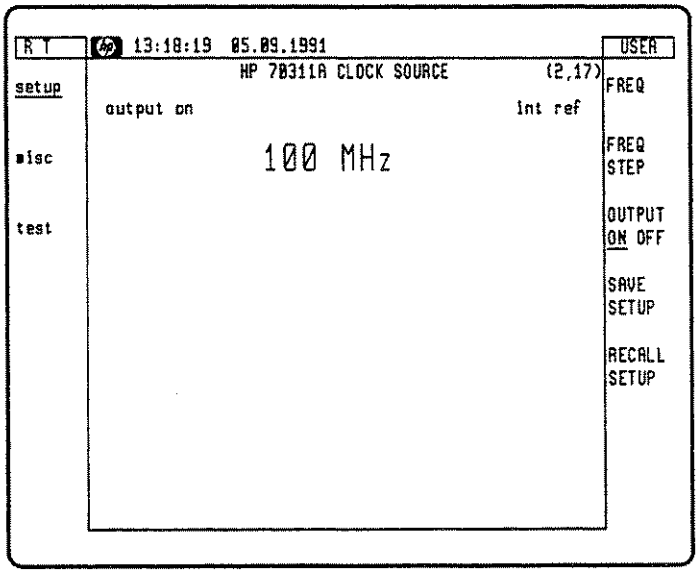

Figure 6-4. HP 70004 Graphics Display

4. Select `Test` from the left hand menu and then `module tests` from the right hand menu.
5. Use the `MORE` softkey on the right menu to select page 3 and then select `LED Test ON/OFF` to be `ON`.
6. Ensure that the leds on the front panel of the clock source light sequentially from left to right and then back again. Press the `LED Test ON/OFF` softkey to stop the test.

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Module Tests

Procedure

1. Select `Test` from the lefthand softkey menu, and then `Test All` from the right hand menu.
2. A display similar to the following should appear, and each module label should be highlighted as its test is performed. The module tests will take approximately 3 minutes after which the displayed condition of all modules should be *good*.

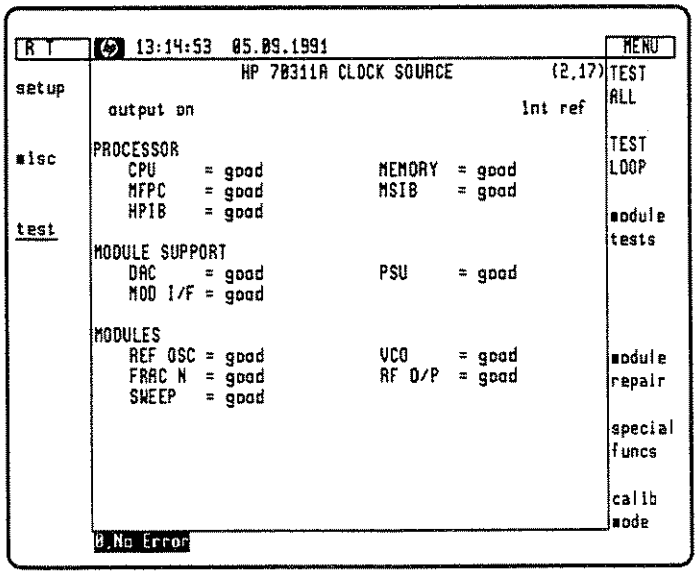

Figure 6-5. Module test display

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VCO Calibration

Introduction

The VCO module can be re-calibrated against internally stored parameters.

1. Press the left-menu `misc` softkey, then the right-menu `Cal VCO` softkey.
2. A display similar to the following will appear and the `>` symbol will be seen to move from left to right across the screen. On reaching the righthand side, the symbol changes to a `<` and moves towards the left until calibration is complete. Calibration takes approximately six minutes. No errors should have occurred during this time.

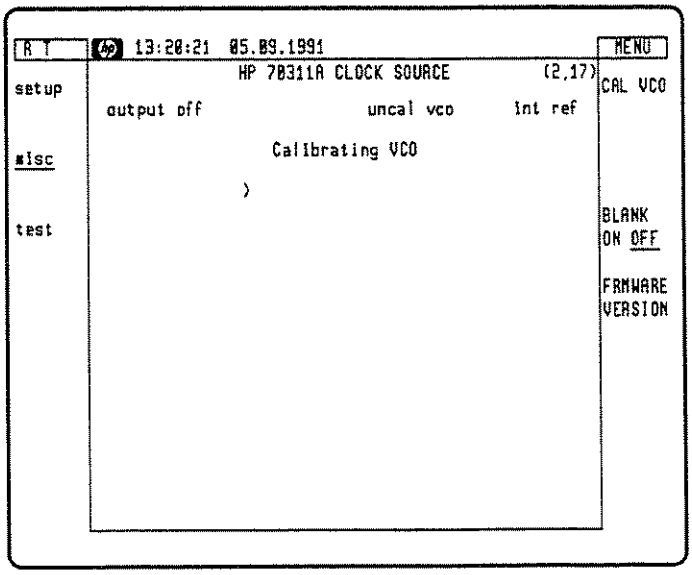

Figure 6-6. VCO Calibration

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Carrier Frequency Accuracy.

Specification

16.09375 MHz to 1.5 GHz for HP 70312A
16.09375 MHz to 3.3 GHz for HP 70311A

Frequency Resolution

Resolution 0.01 Hz.

Stability (typical)

Using internal reference source

Aging ppm/year after 1 year ±2
Temperature ppm, 0 to 45°C ±6

Description

The carrier frequency of the clock source is verified with a frequency counter. Various frequencies are checked to ensure that the Clock Source output frequency can be adjusted over the 16 MHz to 1.5 GHz frequency range for the HP 70312A and 16 MHz to 3.3 GHz in the case of the HP 70311A.

Equipment

MMS Display/Mainframe	HP 70004A
Frequency Counter	HP 5343A

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Procedure

1. Connect the equipment as shown.

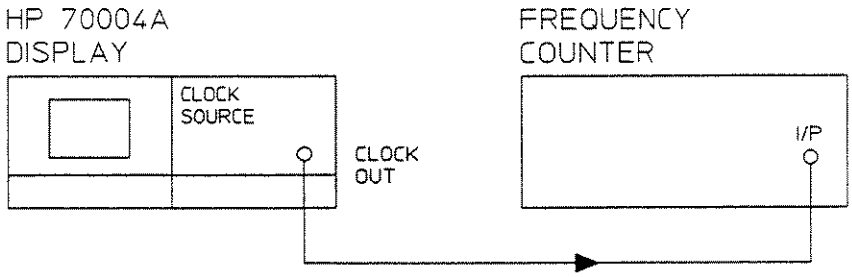

Figure 6-7. Initial Setup

2. Press the `setup` softkey, then set the right-menu `OUTPUT ON/OFF` softkey to `ON`.

3. Enter each of the following frequencies, ensuring they appear on the display exactly as entered, and record the actual frequency (as read from the frequency counter) in the test record.

   515 MHz

   750 MHz

   1,029,999,999.99 MHz

   1.5 GHz

   3.3 GHz (HP 70311A only)

All frequencies are typical and may vary in accordance with the reference stability specification.

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Power Level Flatness.

Specification

Output Level 0dBm ±3dB.

Description

The clock source output power is checked for level flatness from 16.09375 MHz to 1.5 GHz (in the case of the HP 70312A) and from 16.09375 MHz to 3.3 GHz (in the case of the HP 70311A).

Equipment

MMS Display/Mainframe	HP 70004A
Power Meter	HP 435A
Power Sensor	HP 8481D

Procedure

1. Connect the equipment as shown.

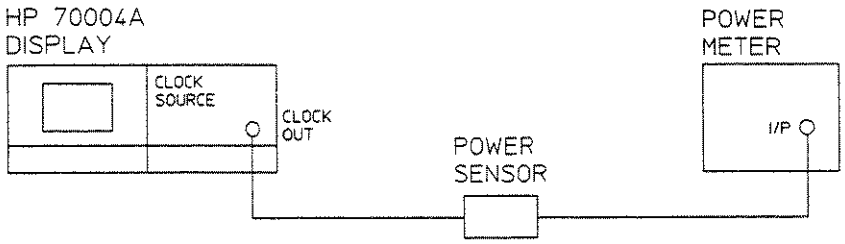

Figure 6-8. Power Level Test setup

2. Ensure that the power meter is calibrated as explained in its Operating Manual.
3. Enter each of the frequencies shown in the Test Record at the rear of this section and record the power level as read from the power meter.

Any readings outside the permissible limits shown in the test record will necessitate re-calibration of the instrument. This is covered in the Adjustments section of the Service manual.

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Spectral Purity (Harmonics and Subharmonics)

Specification

Table 6-2. Harmonics

Frequency Band	
16 - 3300 MHz (70311A)	<-30 dBc
16 - 1500 MHz (70312A)	<-30 dBc

Table 6-3. Sub Harmonics

Frequency Band	
16 -515 MHz	None
515 - 1030 MHz	<-55 dBc
1030 - 2060 MHz (70311A)	<-40 dBc
2060 - 3300 MHz (70311A)	<-35 dBc
1030 - 1500 MHz (70312A)	<-40 dBc

Table 6-4. Multiplied Sub Harmonics

Frequency Band	
16 - 1030 MHz	None
1030 - 2060 MHz (70311A)	<-40 dBc
2060 - 3300 MHz (70311A)	<-35 dBc
1030 - 1500 MHz (70312A)	<-40 dBc

Table 6-5. Spurious Noise

Frequency Band	at 15 kHz offset
16 - 1030 MHz	<-100 dBc
1030 - 2060 MHz (70311A)	<-94 dBc
2060 - 3300 MHz (70311A)	<-88 dBc
1030 - 1500 MHz (70312A)	<-94 dBc

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Description

Harmonics and subharmonics (including multiplied sub harmonics) are observed directly on an RF spectrum analyzer while the clock source is swept over its frequency range.

Equipment

MMS Display/Mainframe	HP 70004A
RF Spectrum Analyzer	HP 8566B

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Harmonics

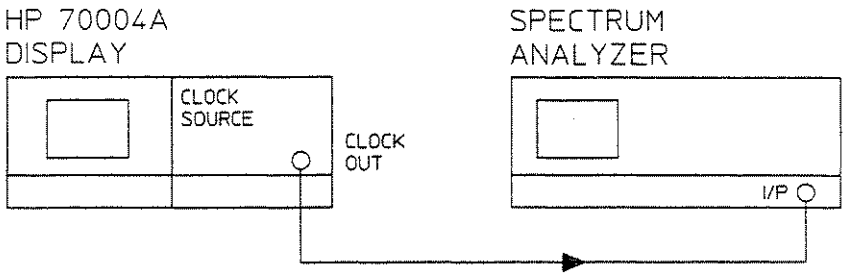

Figure 6-9. Harmonics and Subharmonics Test setup

Note

When using the HP 8566B spectrum analyzer to do harmonic and subharmonic tests, it may be necessary to switch bands during the tests such that the complete span may be swept.

Procedure

1. The equipment is connected as shown in Figure 6-9.
2. Select `Setup` on the HP 70004A display and then setup the conditions given in the first row of Table 6-6, that is, a frequency value of 16.09375 MHz, a frequency step value of 1 MHz and select `output ON/OFF` to ON.
3. Set the spectrum analyzer for a span width of 200 MHz or greater with compatible resolution and display bandwidth smoothing. Set the vertical sensitivity and attenuation to view a 0 dBm signal with at least 40 dB of uncompressed range. Adjust the sensitivity until the Clock Source carrier peak is at a convenient horizontal graticule.
4. Use the RPG control knob to increment the output frequency of the clock source to 100 MHz. Observe the fundamental and harmonics of the carrier on the spectrum analyzer. The level of any harmonics should be in accordance with the specifications given in chapter 1.
5. Repeat the above procedure for the conditions shown in the following table.

Table 6-6. Harmonic Test Conditions

Carrier Frequency Fundamental	Frequency Step	Spectrum Anal. Span	Highest Harmonic Level	Highest Actual Level
16.09375 - 100 MHz	1 MHz	10 - 300 MHz	<-30 dBc	
100 MHz - 1.5 GHz	10 MHz	150 MHz - 5 GHz	<-30 dBc	
1 GHz - 1.5 GHz (HP 70312A)	10 MHz	2 GHz - 5 GHz	<-30 dBc	
1 GHz - 3.3 GHz (HP 70311A)	10 MHz	2 GHz - 10 GHz	<-30 dBc	

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Subharmonics

Procedure

1. With the equipment still connected as in Figure 6-9, setup the first row of conditions as specified in Table 6-7, that is, output frequency to 16.09375 MHz and frequency step to 1 MHz. Set the spectrum analyzer for a span width of 200 MHz.
2. Increment the clock source output frequency and observe the fundamental, subharmonics and multiplied subharmonics (1.5 times the fundamental) of the clock source on the spectrum analyzer.
3. Repeat the above procedure for all of the conditions shown in Table 6-7, subharmonic levels should be as specified in Table 6-7.

Table 6-7. Subharmonic test conditions

Carrier Frequency Fundamental	Frequency Step	Spectrum Anal. Span	Highest Subharmonic Level	Highest Actual Level
16.09375 - 100 MHz	1 MHz	0 - 200 MHz	None	
100 - 515 MHz	10 MHz	50 - 800 MHz	None	
515 - 1029 MHz	10 MHz	100 MHz - 4 GHz	<-55 dBc	
1030 MHz - 1.5 GHz	10 MHz	100 MHz - 4 GHz	<-40 dBc	
1.5 - 2060 MHz (HP 70311A)	10 MHz	2 - 6 GHz	<-40 dBc	
2060 - 3.3 GHz 70311A)	10 MHz	2 - 6 GHz	<-35 dBc	

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Spurious Noise

Procedure

1. With the equipment still connected as in Figure 6-9, setup the first row of conditions as shown in Table 6-8, that is, Carrier Frequency 16.09375 MHz, Frequency step 1 MHz, Span 0 - 20 MHz.
2. Use the display knob to sweep the clock source through its full range. Spurious signal levels should not be above those shown in Table 6-8. Repeat the above procedure for all the conditions shown in Table 6-8.

Note

Spurious signals should not be confused with harmonically (and sub-harmonically) related outputs. These will normally be of much higher magnitude (-55 to -40 dBc) typically.

Table 6-8. Spurious Noise

Carrier Frequency	Frequency Step	Spectrum Anal. Span	Highest Spurious Level	Highest Actual Level
16.09375 MHz - 1030 MHz	1 MHz	0 - 1030 MHz	<-100 dBc	
1030 MHz - 1.5 GHz	1 MHz	0 - 1.5 GHz	<-94 dBc	
1.5 GHz- 2060 MHz (70311A)	1 MHz	0 - 2.5 GHz	<-94 dBc	
2060 MHz - 3.3 GHz (70311A)	1 MHz	2 - 4 GHz	<-88 dBc	

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Spectral Purity (SSB Phase Noise)

Specification

Table 6-9. Phase Noise

Frequency Band MHz	Offset kHz		
	1	20	100
	dBc/Hz	dBc/Hz	dBc/Hz
16 - 32	-113	-140	-140
32 - 64	-108	-140	-140
64 - 128	-103	-140	-140
128 - 257	-98	-138	-140
257 - 515	-93	-134	-140
515 - 1030	-88	-128	-138
1030 - 2060 (70311A)	-81	-121	-131
2060 - 3300 (70311A)	-75	-115	-125
1030 - 1500 (70312A)	-81	-121	-131

Description

The single sideband (SSB) phase noise and non-harmonic spurious signals are measured by a system that is specifically designed to measure these parameters-the HP 3048A phase noise measurement system. Measurements are made using a phase detector in a phase lock loop. This method requires a reference signal generator that must have lower phase noise than the source being tested. To this end, an HP 8662A signal generator is used as a reference from 1 kHz out to 20 kHz offset from the carrier and an HP 8642B signal generator is used for frequencies from 20 kHz to 100 kHz offset from the carrier.

Equipment

Phase Noise Test Set	HP 3048A
Signal Generator	HP 8642B
Signal Generator	HP 8662A
MMS Display/Mainframe	HP 70004A

Note

The following steps are a procedure for making a single-sideband phase noise measurement on a 1GHz carrier. For other frequencies the procedure is similar. If these measurements are to be repeated in the future for this or other clock sources, it will be advantageous to record the entries for each carrier frequency, the test files can then be recalled as needed instead of having to re-enter them each time.

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Procedure

1. Connect the equipment as shown.

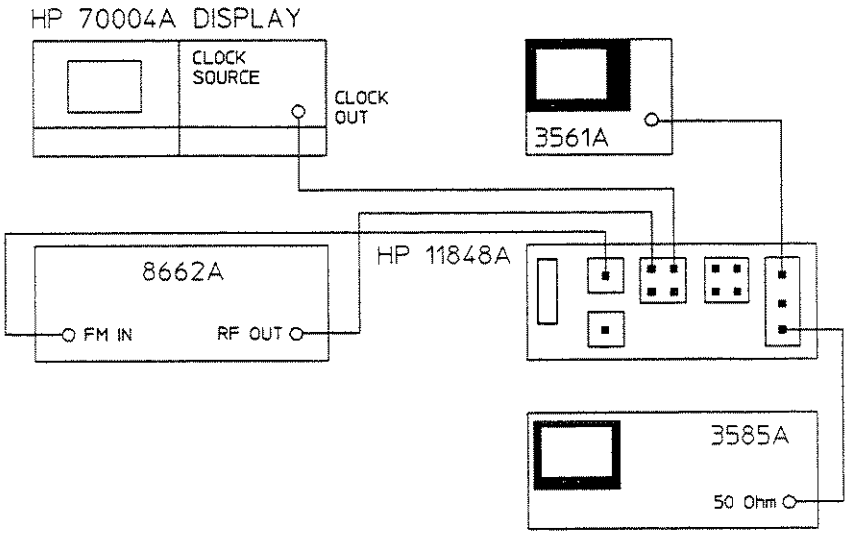

Figure 6-10. Phase Noise Test setup

2. Set the clock source under test as follows:-
3. Set the `OUTPUT ON/OFF` softkey to `ON`.
4. Key in 1 GHz.
5. Set the HP 3048A to the Main Software Level menu. Refer to Figure 6-11.

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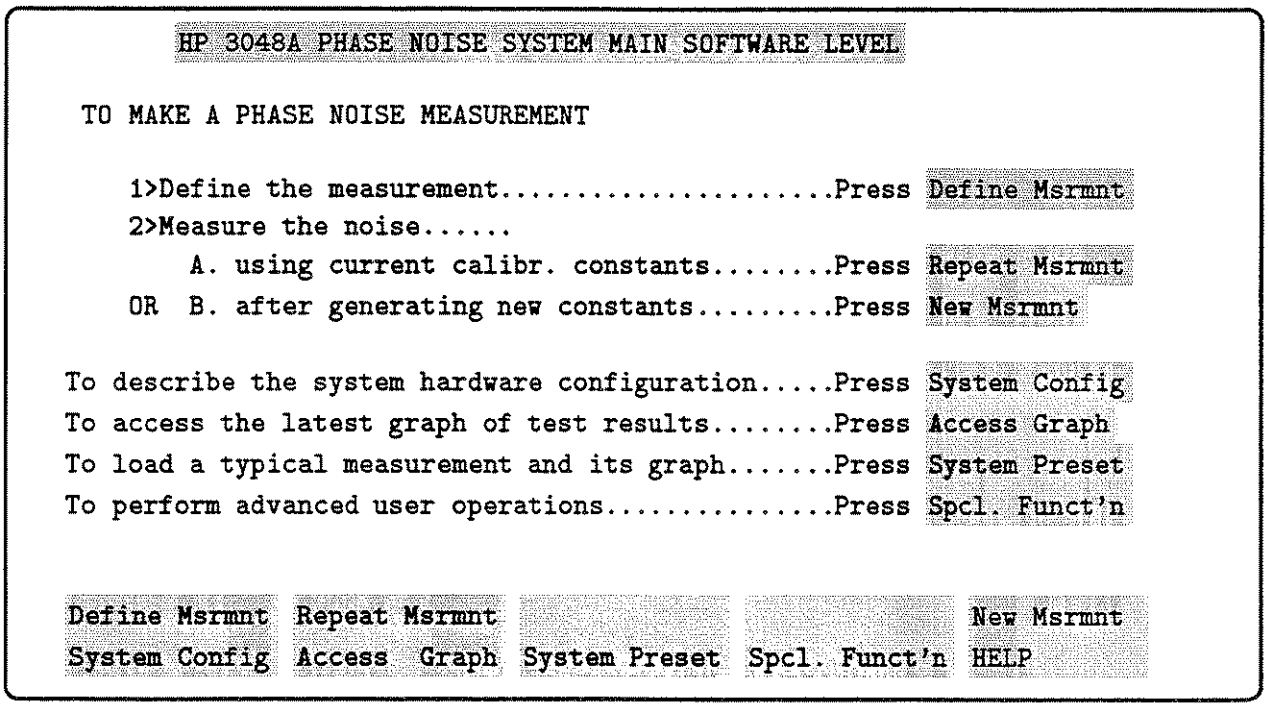

Figure 6-11. HP 3048A Phase Noise System Main Software Level

6. On the HP 3048A press the `Define Msrmnt` softkey to obtain the Measurement Definition menu as in Figure 6-12.

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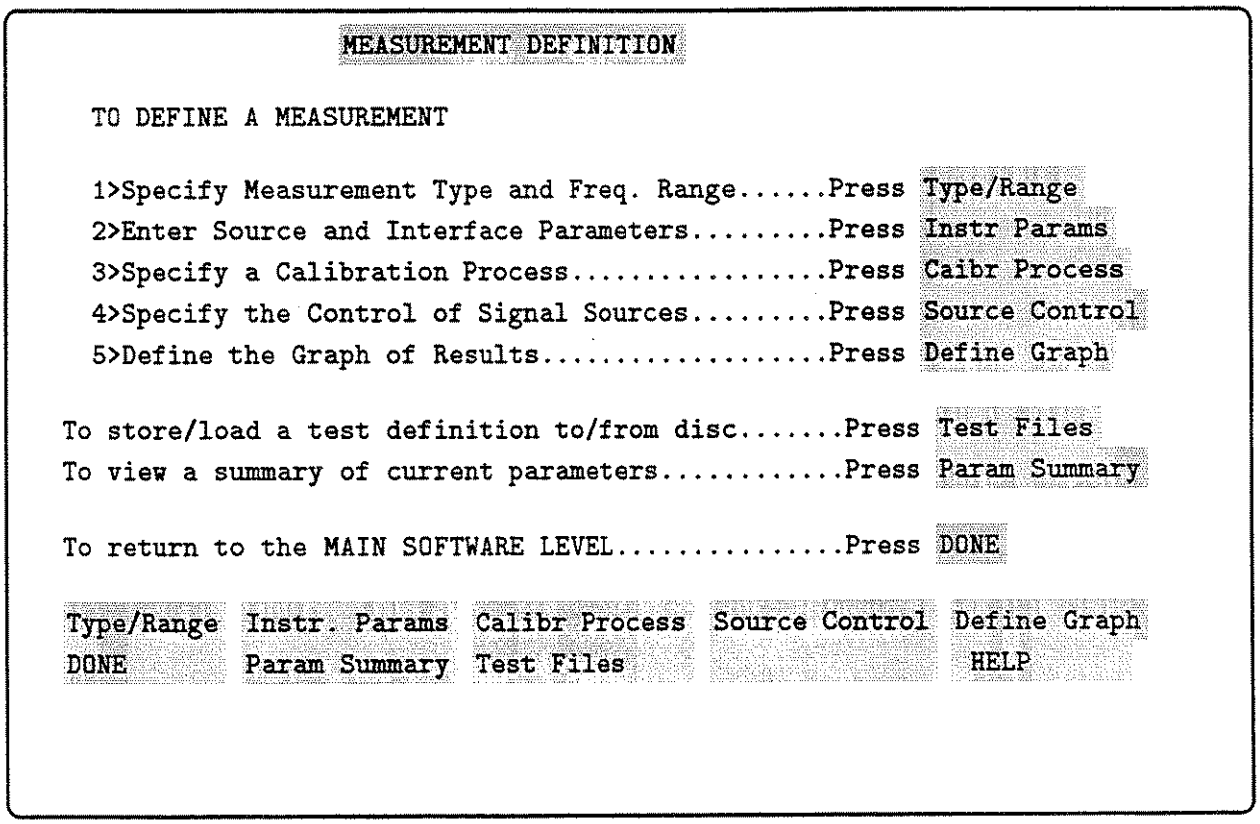

Figure 6-12. Measurement Definition Menu

7. On the HP 3048A press the TYPE/RANGE softkey to obtain the Measurement Type and Frequency Range Specification menu. Set the Measurement Type and Offset Frequency Range as shown in Figure 6-13. When done press the DONE softkey.

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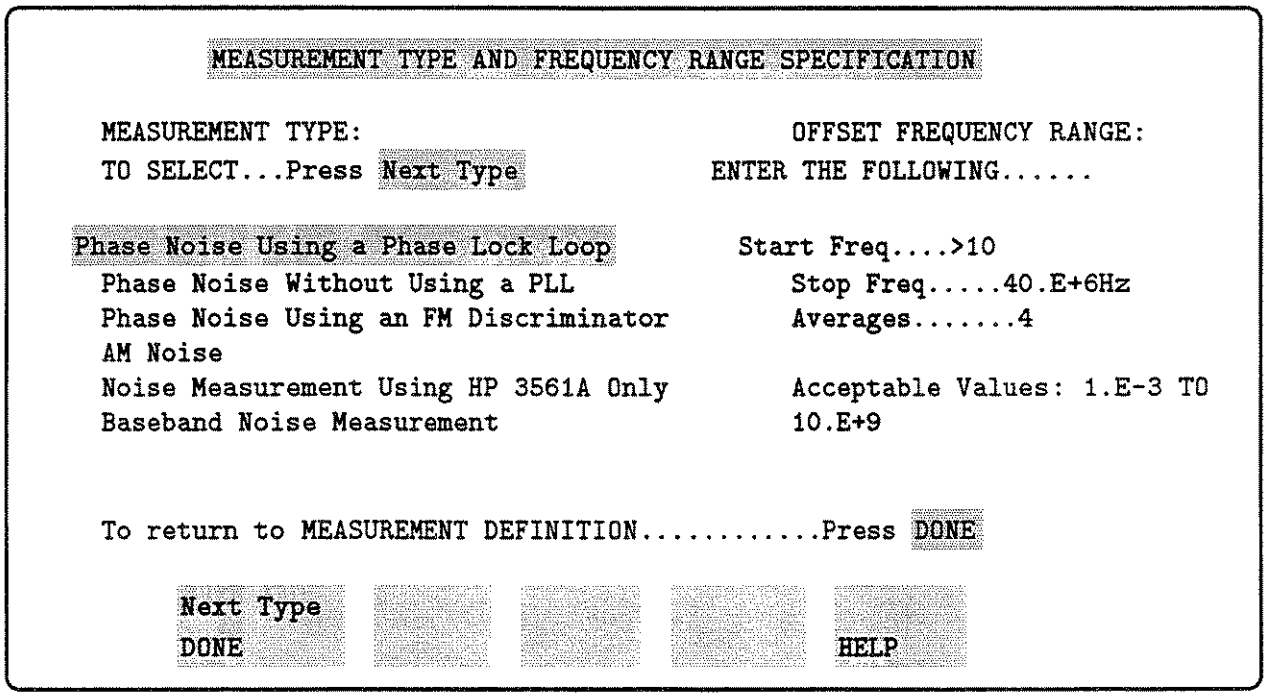

Figure 6-13. Measurement Type and Frequency Range Specification

8. On the HP 3048A press the `Instr. Params` softkey to obtain the Source and Interface Parameter Entry menu. Set the parameters and phase detector as shown in Figure 6-14. When done press the `DONE` softkey.

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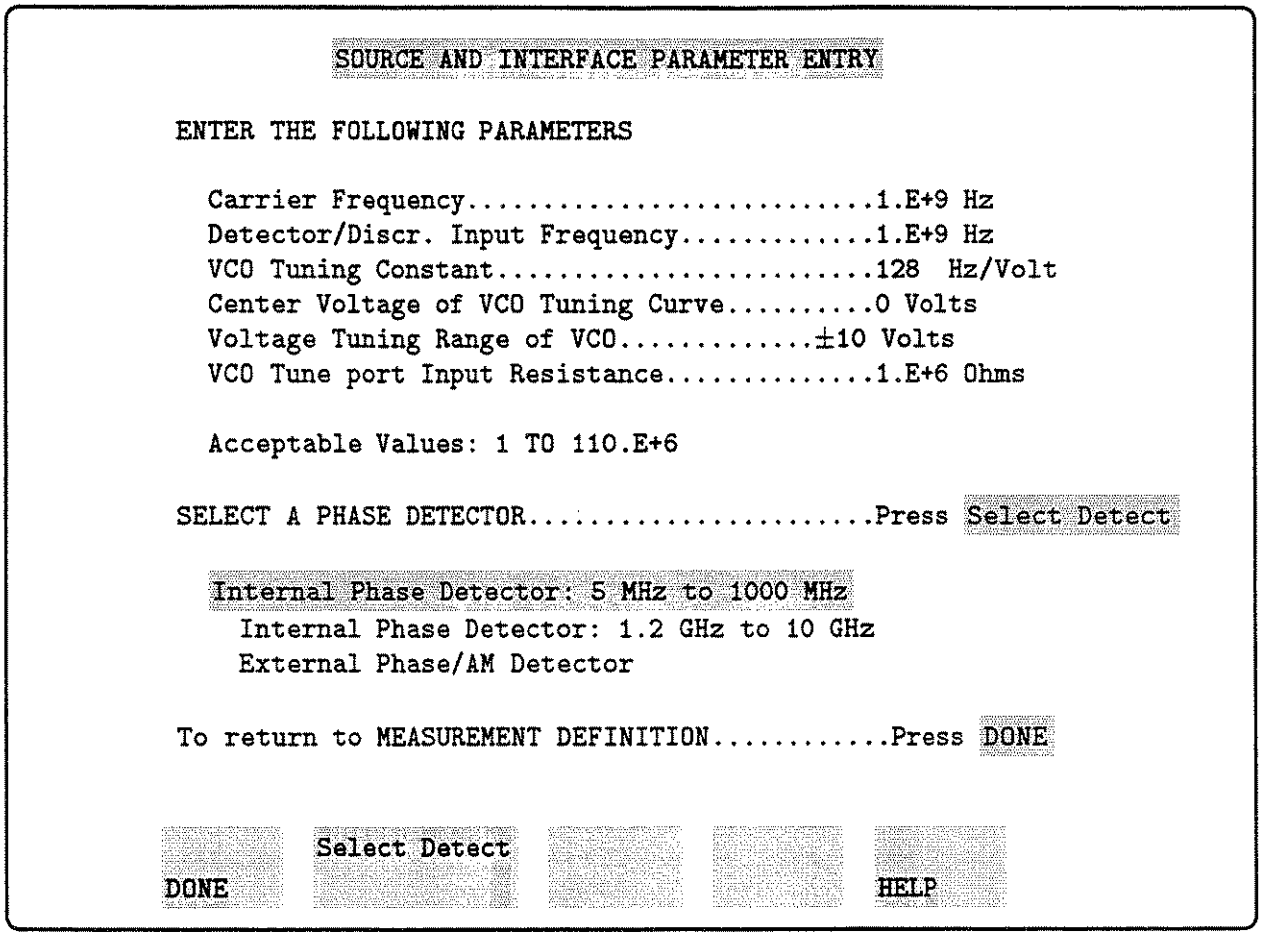

Figure 6-14. Source and Interface Parameter Entry Menu

9. On the HP 3048A press the `Calibr Process` softkey to obtain the Definition of Phase Detector Constant and VCO Tuning Constant menu. Set the method of determining the phase detector and VCO tuning constants and the verification of the phase lock loop suppression as shown in Figure 6-14 (the displayed Computed Constant may be quite different from the one in Figure 6-15, it will be updated later.) When done press the `DONE` softkey.

10. On the HP 3048A press the `Source Control` softkey to obtain the Source Control for Measurement Using a Phase Lock Loop menu. Set the various devices in the system as shown in Figure 6-16. When done press the `DONE` softkey.

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```
DETERMINATION OF PHASE DETECTOR CONSTANT AND VCO TUNING CONSTANT

Select a method for determining the PHASE DETECTOR CONSTANT.

Use the current Tuning Constant
Measure the Detector Constant

Select a method for determining the VCO TUNING CONSTANT.

Use the current Tuning Constant
 Measure the VCO Tuning Constant
Compute from expected T. Constant

The computed PLL suppression WILL NOT be verified.

To return to the previous menu.............Press DONE

                Detect Const                    Verify Suppr
DONE            Tuning Constant                 HELP
```

Figure 6-15. Determination of Phase Detector and VCO Timing Constant

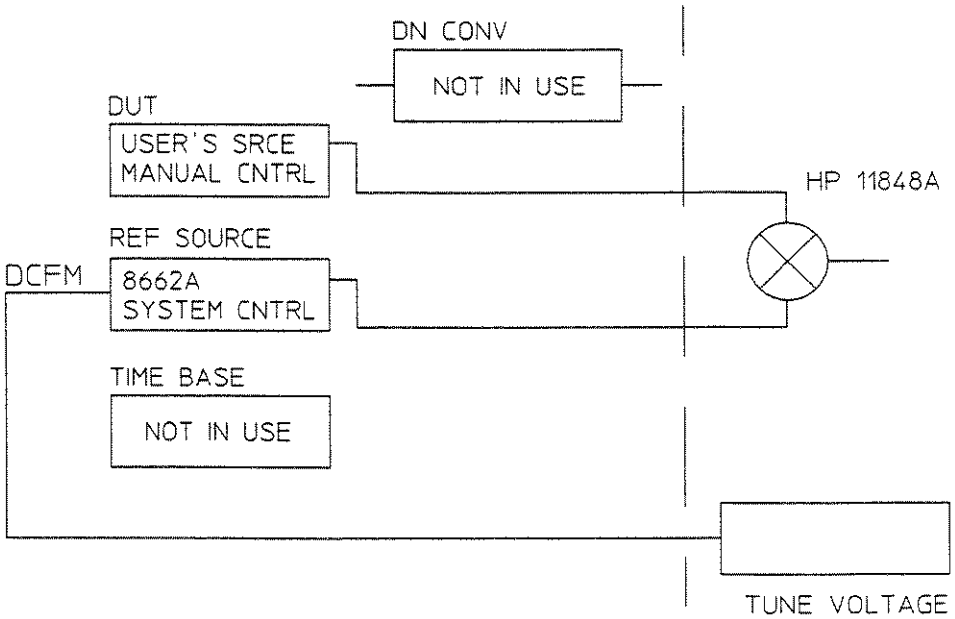

Figure 6-16.
Source control for Measurement Using a Phase Lock Loop Menu

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11. On the HP 3048A press the `Define Graph` softkey to obtain the Graph Definition Menu. Set the graph parameters and graph type as shown in Figure 6-17. Change the title as appropriate for your particular setup. (You may wish to include the serial number of the clock source under test for example.)

```
                    GRAPH DEFINITION

ENTER THE FOLLOWING PARAMETERS:

  Title.....TYPICAL SSB PHASE NOISE AT 1 GHz
  Minimum X coordinate.................1.E+3   Hz
  Maximum X coordinate.................100.E+3 Hz
  Minimum Y coordinate.................-40
  Maximum Y coordinate.................-170

 SELECT A GRAPH TYPE...................Press Graph Type
Single Sideband Phase Noise (dBc/Hz)
  Phase Modulation Spectral Density (dB/Hz)
  FM Spectral Density (Hz/SQR(Hz))
  Spectral Density of Fractional Freq. Fluctuations (1/SQR (Hz))

 To return to MEASUREMENT DEFINITION......Press DONE

                                                Graph Type
DONE                    Spec Lines              HELP
```

Figure 6-17. Graph Definition Menu

Note

The date, time and carrier frequency information will automatically appear on the measurement result graph.

12. When done press the `DONE` softkey.
13. On the HP 3048A press the `DONE` softkey again to obtain the Main Software Level Menu.
14. On the HP 3048A press the `New Msrmnt` softkey then press the `Yes, Proceed` softkey.
15. When the connect diagram appears on the display, verify that the instrument connections are properly made then press the `Proceed` softkey. The phase noise measurement should proceed without error.
16. Steps 5 to 14 should be repeated for the offset frequency range 10 kHz to 100 kHz using the HP 8642B signal generator.

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Note

At the 20 kHz offset frequency, the phase noise value entered in the performance test results sheet should be the lowest of the two values obtained with the HP 8662A and HP 8642B signal generators.

Note

Spurious signals can also be generated by the reference signal generator or may be picked up by interconnecting cables. Figure 6-19 shows a listing of measurement parameters. This listing with the graph itself can be printed by holding down the keyboard's SHIFT key and pressing the `Hard Copy` softkey.

A plot of typical phase noise is shown in figure 6-18. This plot was obtained using an external precision frequency reference, and EFC control of the reference generator.

If you intend to make measurements of this type frequently, the setup information (carrier frequency, tuning constant, source control etc.) can be easily stored as test files, then loaded as needed. Refer to the HP 3048A Reference Manual for information on storing and loading test files.

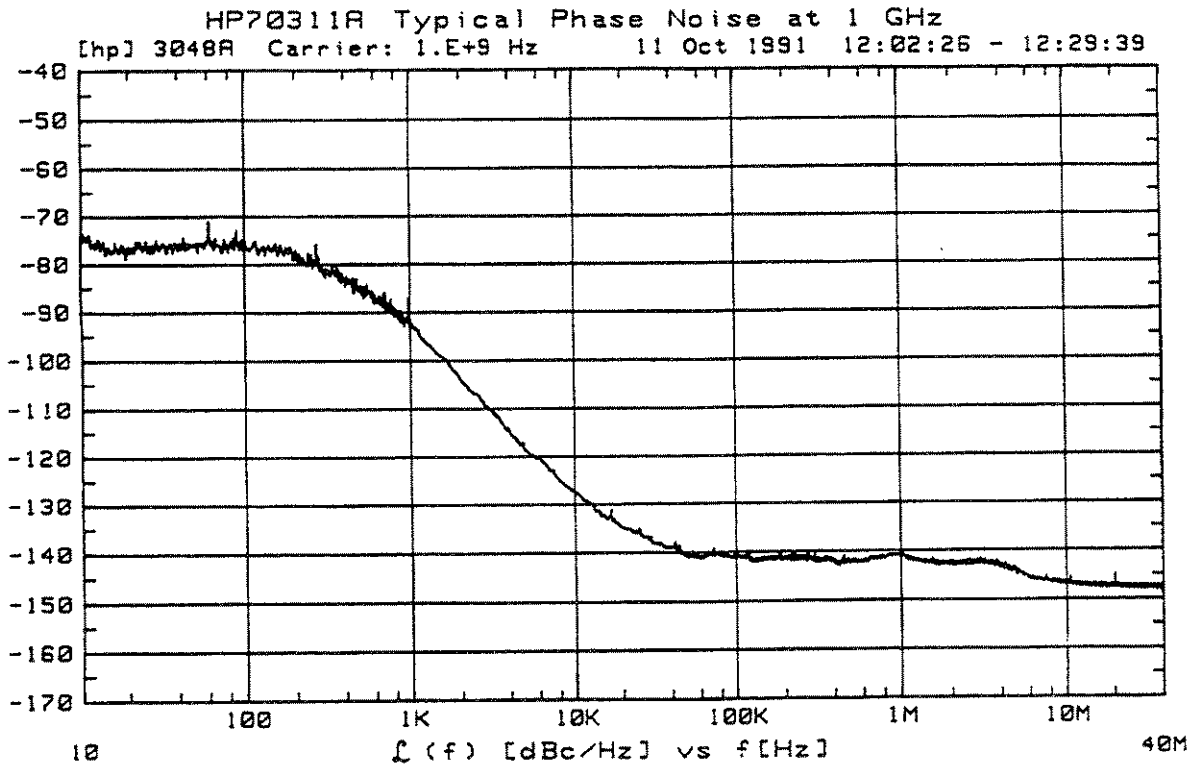

Figure 6-18. Phase Noise Plot

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```
                PERTINENT MEASUREMENT PARAMETERS

Measurement  Type: PHASE LOCKED    K_VCO Method      :COMPUTED
Start Offset Freq: 10 Hz           VCO Tune Constant: 11.8 Hz/Volt
Stop  Offset Freq:40.E+6 Hz
Minimum  Averages:10               Loop Suppression : NOT VERIFIED
                                   Closed Pll Bandw.: 216.2 Hz
Carrier Frequency: 1.E+9 Hz        Peak Tuning Range: 1.003E+3 Hz
Detect. Input Frq: 1.E+9 Hz        Assumed Pole      : 4.E+3 Hz

Entered K_VCO     : 128 Hz/Volt     Dev. Under Test  : USER'S SRCE, MAN
Center Voltage    : 0 Volts         Reference Source : 8662A, SYS, VCO, DCFM

Tune-voltage Rnge: +/- 10 Volts    Ext. Timebase     : NOT IN USE
Phase Detector    : 5 TO 1600 MHz  Down Converter    : 11729C, SYS

K_Detector Method: MEASURED        HP 11848A LNA     : OUT
Detector Constant: 244.7E-3 V/Rad
```

Figure 6-19. Pertinent Measurement parameters.

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External Reference Input

Specification

Input Impedance	50 ohms, AC coupled
Frequency	10 MHz ±1 kHz
Amplitude	0.224/2V rms

Description

A signal generator is used to check the external reference input on the rear panel of the clock source.

Equipment

Signal Generator	HP 8662A
Cable	HP 11500B
Adaptor	HP Part Number 1250-0671

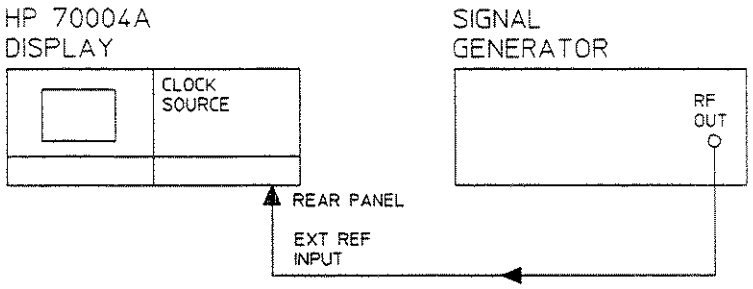

Figure 6-20. Connecting Diagram

Procedure

1. Connect the equipment as shown in Figure 6-20.
2. Switch on the power to both the MMS system and to the signal generator.
3. Set the signal generator for an output of 10 MHz at 0 dBm.
4. Press `INSTR PRESET` on the display and the display in Figure 6-21 should appear.

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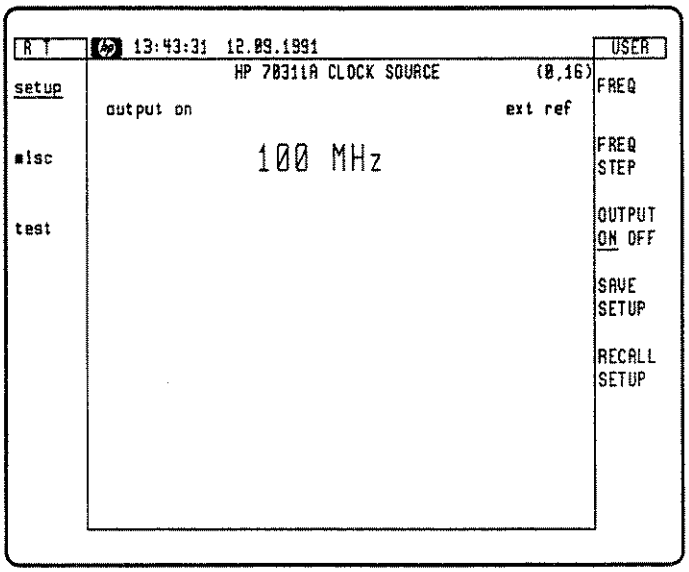

Figure 6-21. Graphics display with External reference

5. Ensure that the "ext ref" message is present at the top righthand corner of the display.
6. Switch off the function generator. The "ext ref" message should now change to "int ref".

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Performance Test Record

Hewlett-Packard Model 70311A/70312A Clock Source	
Location:	*Serial No.:*
	Tested by:
Temperature:	*Certified by:*
Humidity:	*Date:*

Performance Test Record

Page No.	Test Description	Result		
		Min	*Max*	*Actual*
6-3	**Operation Verification Test**			PASS (√)
	Performance Tests			
6-7	**LED Test**			PASS (√)
6-8	**Module Test**			PASS (√)
6-9	**VCO Calibration**			PASS (√)
6-10	**Carrier Frequency Accuracy**			
	515 MHz	514,996,910 Hz	515,003,090 Hz	
	750 MHz	749,995,500 Hz	750,004,500 Hz	
	1,029,999,999 MHz	1029,993,821 Hz	1030,006,180 Hz	
6-12	**Power Level Flatness**			
	20 MHz at 0 dBm	-3 dBm	+3 dBm	
	30 MHz at 0 dBm	-3 dBm	+3 dBm	
	40 MHz at 0 dBm	-3 dBm	+3 dBm	
	60 MHz at 0 dBm	-3 dBm	+3 dBm	
	70 MHz at 0 dBm	-3 dBm	+3 dBm	
	120 Mhz at 0 dBm	-3 dBm	+3 dBm	
	140 MHz at 0 dBm	-3 dBm	+3 dBm	
	250 MHz at 0 dBm	-3 dBm	+3 dBm	
	260 MHz at 0 dBm	-3 dBm	+3 dBm	
	500 MHz at 0 dBm	-3 dBm	+3 dBm	
	530 MHz at 0 dBm	-3 dBm	+3 dBm	
	1 GHz at 0 dBm	-3 dBm	+3 dBm	
	1.5 GHz at 0 dBm	-3 dBm	+3 dBm	
	2.0 GHz at 0 dBm (HP 70311A only)	-3 dBm	+3 dBm	
	2.2 GHz at 0 dBm (HP 70311A only)	-3 dBm	+3 dBm	
	3.3 GHz at 0 dBm (HP 70311A only)	-3 dBm	+3 dBm	

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Performance Test Record (continued)

Page No.	Test Description	Result		
			Max	*Actual*
6-13	**Spectral Purity (Harmonics)**			
6-15	**Harmonics**			
	HP 70312A only			
	16 to 1500 MHz < -30 dBc		-30 dBc	
	HP 70311A only			
	16 to 3300 MHz < -30 dBc		-30 dBc	
6-16	**Subharmonics**			
	16 to 515 MHz (None)			
	515 to 1030 MHz		-55 dBc	
	1030 to 1500 MHz		-55 dBc	
	1500 to 3300 MHz (HP 70311A)		-55 dBc	
6-17	**Spurious Noise**			
	0 to 1030 MHz		-100 dBc	
	1030 to 1500 MHz		-94 dBc	
	1500 to 2060 Mhz (HP 70311A)		-94 dBc	
	2060 to 3300 MHz (HP 70311A)		-88 dBc	
6-18	**SSB Phase Noise**			
	Frequency.... ... Offset			
	24 MHz.... ... 1 kHz		-113 dBc	
	24 MHz.... ... 20 kHz		-140 dBc	
	24 MHz.... ... 100 kHz		-140 dBc	
	48 MHz.... ..1 kHz		-108 dBc	
	48 Mhz.... ..20 kHz		-140 dBc	
	48 MHz.... ..100 kHz		-140 dBc	
	96 Mhz.... ..1 kHz		-103 dBc	
	96 Mhz.... ..20 kHz		-140 dBc	
	96 MHz.... ..100 kHz		-140 dBc	
	192 MHz.... ..1 kHz		-98 dBc	
	192 MHz.... ..20 kHz		-138 dBc	
	192 Mhz.... ..100 kHz		-140 dBc	
	384 MHz.... ..1 kHz		-93 dBc	
	384 MHz.... ..20 kHz		-134 dBc	
	384 MHz.... ..100 kHz		-140 dBc	
	768 MHz.... ..1 kHz		-88 dBc	
	768 MHz.... ..20 kHz		-128 dBc	
	768 MHz.... ..100 kHz		-138 dBc	

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Performance Test Record (continued)

Page No.	Test Description	Result		
	HP 70311A only			
	1536 MHz. . . . ..1 kHz		-81 dBc	
	1536 MHz. . . . ..20 kHz		-121 dBc	
	1536 MHz. . . . ..100 kHz		-131 dBc	
	3072 MHz. . . . ..1 kHz		-75 dBc	
	3072 MHz. . . . ..20 kHz		-115 dBc	
	3072 MHz. . . . ..100 kHz		-125 dBc	

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A

Error Messages

Error Messages

Each error message is comprised of an error number and an error description. The format of error messages is :

<error number>,"<error description>"

The errors are grouped into classes of error numbers as defined below.

The Error Queue

As errors are detected they are placed in an error queue. The queue is first in, first out. When all errors have been read from the queue, further error queries return : 0, No error.

If the error queue overflows, the last error in the queue is replaced with the error : -350, Too many errors. On queue overflow the least recent errors remain in the queue and the most recent error is discarded. The queue has space for 12 errors.

If one or more permanent error conditions occur, successive error queries will return the error messages, followed by : 0, No error. Further error queries will repeat the sequence of permanent error messages followed by : 0, No error. This sequence informs the user that the whole error queue has been read but the error conditions still exist.

No Error

0, No error

Command Errors

An error number in the range [-199, -100] indicates that an *IEEE 488.2* syntax error has been detected by the instrument's parser.

-100, Command error
-101, Invalid character
-102, Syntax error
-103, Invalid separator
-104, Data type error
-108, Parameter not allowed
-109, Missing parameter

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-110, Command header error
-111, Header separator error
-112, Program mnemonic too long
-113, Undefined header
-114, Header suffix out of range

-120, Numeric data error
-121, Invalid character in number
-123, Exponent too large
-124, Too many digits
-128, Numeric data not allowed

-140, Character data error
-141, Invalid character data
-144, Character data too long
-148, Character data not allowed
-150, String data error
-151, Invalid string data
-158, String data not allowed

Execution Errors

An error number in the range [-299, -200] indicates that an error has been detected in the instrument's execution control block.

-200, Execution error
-222, Data out of range

Device-Specific Errors

An error number in the range [-399, -300] indicates that the instrument has detected an error which is not a command error, an execution error, or a query error.

-300, Device-specific error
-350, Too many errors

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Query Errors

An error number in the range [-499, -400] indicates that the output queue control of the instrument has detected a problem with the message exchange protocol.

-400,	Query error
-410,	Query interrupted
-420,	Query unterminated
-430,	Query deadlocked
-440,	Query unterminated after indefinite response

Hardware Failure Errors

An error number in the range [100, 500] indicates that the instrument has detected an internal fault condition. The error messages are listed in Appendix B.

Grouping of Error Messages

For the purpose of slaving the clock source to other instruments, the error messages may be divided into three groups : controller induced errors, user induced errors and instrument induced errors.

Controller Induced Errors

These are caused by errors in the syntax of commands given to the instrument.

-199 to -100	All command errors
-499 to -400	All query errors

User Induced Errors

These are caused by command data which is outwith the operating range of the instrument.

-222	Data out of range (execution error)

Instrument Induced Errors

These are caused by errors detected in the instrument's hardware/firmware.

-200	Execution error
-399 to -300	All device-specific errors
100 to 500	All hardware failure errors

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Power-on / Reset Conditions

Initial Power-on or NVM RAM Error

This condition occurs when the instrument is powered up for the very first time, or when the contents of the non-volatile RAM memory have previously been lost. The condition can be caused by a battery failure, the installation of a new revision of firmware, or the replacement of the processor board.

a. The operating frequency is set to 100 MHz.

b. The RF output is turned ON.

c. The RF output blanking is turned OFF.

d. The 10 instrument state storage registers are all set to 100 MHz frequency, 1 MHz step size, RF output ON, RF output blanking OFF.

e. The device status registers are initialized to the values given in Table 5-1.

f. The VCO loop is recalibrated.

g. The error message queue is cleared.

h. The EEPROM data may also be initialized, as described in the following paragraph.

Power-on after an EEPROM Error

This condition occurs if an EEPROM checksum error is detected when the instrument is powered up. The condition can be caused by powering up the instrument for the very first time, or the replacement of the processor board.

a. The calibration of the internal reference oscillator and output level control are set to the default values stored in ROM memory.

b. The other power-on conditions are as described in the previous and next paragraphs.

Normal Power-on

This condition occurs when the instrument is powered up after previous normal operation.

a. The operating frequency and the 10 instrument state storage register values are preserved through a power fail.

b. The RF output ON/OFF state is preserved through a power fail.

c. The Service Request Enable Register and Standard Event Status Enable Register are cleared if the power-on-status-clear flag is true, otherwise they are preserved through a power fail.

d. The enable states of all status registers apart from the Service Request Enable Register and Standard Event Status Enable Register are preserved through a power fail.

e. The Standard Event Status Register is cleared.

f. The error message queue is cleared.

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Instrument Reset

This condition occurs when a *RST command is received, a SYSTem:PRESet command is received, or when the front panel PRESET key is operated.

a. The operating frequency is set to 100 MHz.

b. The frequency step size is set to 1 MHz.

c. The RF output is turned ON.

d. The RF output blanking is turned OFF.

e. Any currently running self tests are turned off.

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B

Hardware Error Messages

There are three groups of hardware errors; fatal hardware, non-fatal and soft errors.

Fatal hardware errors are caused by hardware failures in the instrument. They cause any self-tests to stop immediately. An associated bit is set in the Hardware Fail Status register; the DDE bit is set in the Standard Event Status register and a message is put into the error message queue.

Non-fatal hardware errors are caused by transient or correctable hardware errors in the instrument. Any self-tests, apart from the loop test, continue to run to check for further errors. The error reporting is the same as for fatal errors.

Soft errors are caused by lack of calibration of a module or transient errors. The DDE bit is set in the Standard Event Status register and a message is put into the error message queue. Subsequent self tests of the uncalibrated module will not show an error condition.

Hardware Errors

100, Cpu condition code
101, Cpu register bit/decode error
102, Cpu move instruction error
103, Cpu math instruction error
104, Cpu bit manipulation error
105, Cpu program control error
106, Cpu data bus error
107, Cpu address mode error
108, Cpu noise test error
109, Cpu ram check error
110, Cpu hi ports data bus error
111, Cpu lo ports data bus error
112, Cpu bad led status latch

120, Ram U25 data error
121, Ram U25 addr error
122, Ram U26 data error
123, Ram U26 addr error
124, Ram U27 data error
125, Ram U27 addr error
126, Ram U28 data error
127, Ram U28 addr error

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130, Rom U16 error
131, Rom U17 error
132, Rom bad datecodes

140, Nvm battery error

150, Eerom bad control latch
151, Eerom verify error
152, Eerom cycle error
153, Eerom checksum error

160, Mfp bad mfp controller
161, Mfp aer verify error
162, Mfp ddr verify error
163, Mfp iera verify error
164, Mfp ierb verify error
165, Mfp imra verify error
166, Mfp imrb verify error

167, Mfp tadr verify error
168, Mfp tacr verify error
169, Mfp timer a, stuck
170, Mfp timer a, count too fast
171, Mfp timer a, count too slow
172, Mfp timer a, int pending error
173, Mfp timer a, reload error

174, Mfp tbdr verify error
175, Mfp tbcr verify error
176, Mfp timer b, stuck
177, Mfp timer b, count too fast
178, Mfp timer b, count too slow
179, Mfp timer b, int pending error
180, Mfp timer b, reload error

181, Mfp tddr verify error
182, Mfp tcdcr verify error
183, Mfp timer d, stuck
184, Mfp timer d, count too fast
185, Mfp timer d, count too slow
186, Mfp timer d, int pending error
187, Mfp timer d, reload error

188, Mfp uart tx error
189, Mfp uart rx error
190, Mfp uart overrun error
191, Mfp uart parity error
192, Mfp uart frame error
193, Mfp uart data error

200, Msib bad msib controller

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201, Msib module at address 31
202, Msib external loop broken
203, Msib test pkt lost
204, Msib test pkt type error
205, Msib test pkt size error
206, Msib test pkt data error

210, Hpib bad hpib controller
211, Hpib bad hpib data lines
212, Hpib bad atn line
213, Hpib bad srq line
214, Hpib bad eoi line
215, Hpib bad ren line
216, Hpib bad ndac line
217, Hpib bad int line
218, Hpib bo int error
219, Hpib source handshake error

230, Voltmeter mux. error
231, Voltmeter dc gnd error
232, Voltmeter rms gnd error
233, Voltmeter reference error

234, Cal dac dc gnd error
235, Cal dac reference error
236, Cal dac 0V, dc vco o/p error
237, Cal dac +3V, dc vco o/p error
238, Cal dac 0V, dc nf o/p error
239, Cal dac 0V, ac nf o/p error
240, Cal dac +3V, dc nf o/p error
241, Cal dac +3V, ac nf o/p error
242, Cal dac -3V, dc nf o/p error
243, Cal dac -3V, ac nf o/p error

250, Psu + 5V error
251, Psu +10V error
252, Psu +15V error
253, Psu +38V error
254, Psu - 5V error
255, Psu -15V error

260, Modif serial control latch error
261, Modif serial latch error
262, Modif serial clock error
263, Modif serial data error
264, Modif parallel bus latch error
265, Modif parallel bus buffer error
266, Modif parallel bus data error

270, Ref. osc latch error

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271, Ref. osc dac error
272, Ref. osc o/p disable error
273, Ref. osc o/p enable error

280, Vco communication error
281, Vco mux. error
282, Vco mux. gnd error
283, Vco 0V fm drive, dc error
284, Vco 0V fm kv, ac error
285, Vco 0V fm kv, dc error
286, Vco ext discr. error
287, Vco 0V pl drive, dc error
288, Vco 0V vco tune, dc error
289, Vco 0V pretune dac, dc error
290, Vco 0V pretune dac, ac error
291, Vco pretune dac mid range error
292, Vco pretune dac error bit 0
292, Vco pretune dac error bit 1
292, Vco pretune dac error bit 2
292, Vco pretune dac error bit 3
292, Vco pretune dac error bit 4
292, Vco pretune dac error bit 5
292, Vco pretune dac error bit 6
292, Vco pretune dac error bit 7
292, Vco pretune dac error bit 8
292, Vco pretune dac error bit 9
293, Vco pretune dac max error
294, Vco pretune dac max, filter error
295, Vco osc rf o/p error bit 0
295, Vco osc rf o/p error bit 1
295, Vco osc rf o/p error bit 2
295, Vco osc rf o/p error bit 3
295, Vco osc rf o/p error bit 4
295, Vco osc rf o/p error bit 5
295, Vco osc rf o/p error bit 6
295, Vco osc rf o/p error bit 7
295, Vco osc rf o/p error bit 8
295, Vco osc rf o/p error bit 9
296, Vco pl rf error bit 0
296, Vco pl rf error bit 1
296, Vco pl rf error bit 2
296, Vco pl rf error bit 3
296, Vco pl rf error bit 4
296, Vco pl rf error bit 5
296, Vco pl rf error bit 6
296, Vco pl rf error bit 7
296, Vco pl rf error bit 8
296, Vco pl rf error bit 9

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297, Vco low pretune mixer offset error
298, Vco low pretune mixer zero error
299, Vco high pretune mixer offset error
300, Vco high pretune mixer zero error
301, Vco t_comp +ve offset error
302, Vco t_comp -ve offset error
303, Vco +ve lna fll kd 1 error
303, Vco +ve lna fll kd 2 error
303, Vco +ve lna fll kd 3 error
304, Vco -ve lna fll kd 1 error
304, Vco -ve lna fll kd 2 error
304, Vco -ve lna fll kd 3 error
305, Vco lna o/p +ve polarity error
306, Vco lna o/p -ve polarity error
307, Vco slow integrator error
308, Vco phase dac 0V, dc error
309, Vco phase dac 0V, ac error
310, Vco phase dac mid range error
311, Vco phase dac error bit 0
311, Vco phase dac error bit 1
311, Vco phase dac error bit 2
311, Vco phase dac error bit 3
311, Vco phase dac error bit 4
311, Vco phase dac error bit 5
311, Vco phase dac error bit 6
311, Vco phase dac error bit 7
312, Vco phase dac max error
313, Vco phase dac pretune error
314, Vco +3V fm drive, dc error
315, Vco fm kv fm mode off error
316, Vco fm kv fm mode 40 dB error
317, Vco fm kv fm mode 20 dB error
318, Vco fm kv fm mode 0 dB error
319, Vco 0V fm fll, dc error
320, Vco 0V fm fll, ac error
321, Vco fm dac error bit 0
321, Vco fm dac error bit 1
321, Vco fm dac error bit 2
321, Vco fm dac error bit 3
321, Vco fm dac error bit 4
321, Vco fm dac error bit 5
321, Vco fm dac error bit 6
321, Vco fm dac error bit 7
322, Vco fm dac max error
323, Vco fm fll polarity error
324, Vco fm fll off error
325, Vco fll lock kv error
326, Vco fll lock lna error

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327, Vco +5V pl drive, dc error
328, Vco +ve pl drive, kv dac error
329, Vco +ve pl drive, kv filter error
330, Vco +ve pl drive, kv dac error bit 0
330, Vco +ve pl drive, kv dac error bit 1
330, Vco +ve pl drive, kv dac error bit 2
330, Vco +ve pl drive, kv dac error bit 3
330, Vco +ve pl drive, kv dac error bit 4
330, Vco +ve pl drive, kv dac error bit 5
330, Vco +ve pl drive, kv dac error bit 6
330, Vco +ve pl drive, kv dac error bit 7
331, Vco fll kv +ve offset error
332, Vco fll lna +ve offset error
333, Vco -5V pl drive, dc error
334, Vco -ve pl drive, kv dac error
335, Vco -ve pl drive, kv filter error
336, Vco -ve pl drive, kv dac error bit 0
336, Vco -ve pl drive, kv dac error bit 1
336, Vco -ve pl drive, kv dac error bit 2
336, Vco -ve pl drive, kv dac error bit 3
336, Vco -ve pl drive, kv dac error bit 4
336, Vco -ve pl drive, kv dac error bit 5
336, Vco -ve pl drive, kv dac error bit 6
336, Vco -ve pl drive, kv dac error bit 7
337, Vco fll kv -ve offset error
338, Vco fll lna -ve offset error

339, Vco 0V fm drive i/p, dc error
340, Vco bad fm cable
341, Vco +3V fm drive i/p, dc error
342, Vco +5V pl drive i/p, dc error
343, Vco bad pl drive cable
344, Vco nf +5V pl drive o/p, dc error
345, Vco -5V pl drive i/p, dc error
346, Vco nf -5V dc pl drive o/p, dc error
347, Vco osrf o/p error
348, Vco rfop osrf i/p error
349, Vco bad osrf cable
350, Vco plrf o/p error
351, Vco nf plrf i/p signal error
352, Vco bad plrf cable
353, Vco rf cx i/p error
354, Vco bad delay line o/p cable
355, Vco bad delay line
356, Vco bad delay line i/p cable
357, Vco rx cx o/p error

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358, Vco bad vco error
359, Vco bad nf error
360, Vco pretune cal. error
361, Vco kv control error
362, Vco kv max. gain error
363, Vco fll kd error
364, Vco kd control error
365, Vco kd min. gain error
366, Vco kd max. gain error
367, Vco calibration time out

368, Vco pl kv null error
369, Vco fll ool error
370, Vco realtime adj. error
371, Vco rev 133, no realtime adj.

380, Nf communication error
381, Nf mux. error
382, Nf phase detector, divider on error
383, Nf phase detector, divider off error
384, Nf phase detector, clear error
385, Nf phase detector, ref. error
386, Nf 0V fm drive, dc error
387, Nf 0V fm drive, ac error
388, Nf phase detector, reset error
389, Nf +3V fm drive, dc error
390, Nf +3V fm drive, ac error
391, Nf -3V fm drive, dc error
392, Nf -3V fm drive, ac error
393, Nf phase detector, set error
394, Nf phase detector, vco error
395, Nf integrator sh +ve rail error
396, Nf integrator sh -ve rail error
397, Nf kn dac +ve dc min. error
398, Nf kn dac +ve ac min. error
399, Nf kn dac +ve max. error
400, Nf kn dac +ve mid range error
401, Nf kn dac +ve error bit 0
401, Nf kn dac +ve error bit 1
401, Nf kn dac +ve error bit 2
401, Nf kn dac +ve error bit 3
401, Nf kn dac +ve error bit 4
401, Nf kn dac +ve error bit 5
401, Nf kn dac +ve error bit 6
401, Nf kn dac +ve error bit 7
402, Nf kn dac -ve max. error
403, Nf kn dac -ve mid range error
404, Nf kn dac -ve error bit 0

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404, Nf kn dac -ve error bit 1
404, Nf kn dac -ve error bit 2
404, Nf kn dac -ve error bit 3
404, Nf kn dac -ve error bit 4
404, Nf kn dac -ve error bit 5
404, Nf kn dac -ve error bit 6
404, Nf kn dac -ve error bit 7
405, Nf +ve ool error
406, Nf -ve ool error
407, Nf irq latch error
408, Nf irq mask on error
409, Nf irq mask off error
410, Nf test dac 0V, dc error
411, Nf test dac 0V, ac error
412, Nf test dac, mid range error
413, Nf test dac, error bit 0

413, Nf test dac, error bit 1
413, Nf test dac, error bit 2
413, Nf test dac, error bit 3
413, Nf test dac, error bit 4
413, Nf test dac, error bit 5
413, Nf test dac, error bit 6
413, Nf test dac, error bit 7
414, Nf plrf i/p error
415, Nf bad plrf cable
416, Nf vco plrf o/p error
417, Nf bad pl ref cable
418, Nf pl ref missing
419, Nf 0V fm drive i/p, dc error
420, Nf 0V fm drive i/p, ac error
421, Nf +3V fm drive i/p, dc error
422, Nf bad fm drive cable
423, Nf +3V fm drive i/p, ac error
424, Nf -3V fm drive i/p, dc error
425, Nf -3V fm drive i/p, ac error

426, Nf api1 offset too large error
427, Nf api2 offset too large error
428, Nf api1 stuck at high rail
429, Nf api1 stuck at low rail
430, Nf api1 too low error
431, Nf api1 too high error
432, Nf api1 gain too high
433, Nf api1 can't adjust error

434, Nf pll ool error

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440, Rfop communication error
441, Rfop agc power too high
442, Rfop agc power too low
443, Rfop o/p power too high
444, Rfop o/p power too low

Soft Errors

450, Nvm ram error
460, Eerom cal data error
470, Ref. osc calibration error
471, Ref osc ext. ref. missing
480 Vco fll ool transient error
481, Vco calibration error
482 Vco calibration temp drift
490, Nf pll ool transient error
500, Rfop calibration error
510, Slave needs service
511 Slave not present
512 Unrecognized slave found
513 Too many slaves found
514 Slaved pfr f/w incompatible
515 Slaved clock f/w incompatible

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