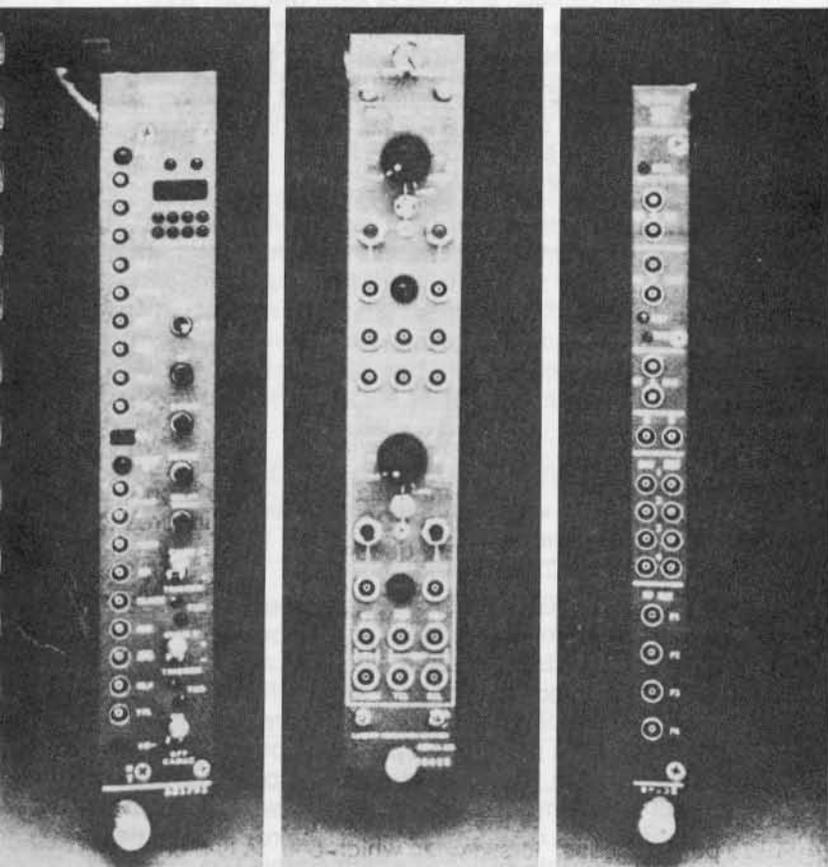


222 DUAL CHANNEL, MANUAL CONTROL
2323A DUAL CHANNEL, MANUAL/PROGRAMMABLE
4222 QUAD, PROGRAMMABLE CONTROL



- Gate, Delay and Delayed Gate Functions
- High Precision, Wide Range
- NIM and CAMAC Packaging
- NIM, TTL, and ECL Level Compatibility
- Minimum Dearthime
- Manual and CAMAC Programming Options

PRECISE TIME PERIODS GENERATED

Gate and Delay Generators are designed to provide precisely timed logic windows and level transitions. Applications employing Gate and Delay Generators may require that a logic transition occur immediately and have a given duration. Others require that a delay elapse prior to the logic transition, or that a precise gate be generated after some fixed delay. All these functions of Gate Generator, Delay Generator, and Delayed Gate Generator are performed by any LeCroy Gate and Delay Generator module.

FEATURES

Versatile Product Family— Two of the most popular modular instrumentation standards used are NIM and CAMAC. Continuous manual control and high resolution programmable digital delay adjustment are selected by choice of Modules.

Minimum Deadtime— Any of these Gate and Delay Generators may be retrigged immediately after the delay has elapsed.

Delayed Outputs— At the end of any gate, a delayed output issues a pulse.

Independent Gate and Delay Functions— Each LeCroy Gate and Delay Generator provides precision gate lengths which can be used as a precision delay as well. Since each unit has at least two such gate generators, one can be used as a delay which starts the second generator that provides the gate signal.

Wide Dynamic Range— Ranges from under 100 nsec to 10 sec are provided by either the Model 222 or 2323A. Model 4222 maintains 1 nsec resolution up to its range of 16.7 msec.

FUNCTIONAL DESCRIPTION

LeCroy Gate and Delay Generators allow both manual and CAMAC programmability for gate durations ranging from a few nanoseconds to several seconds. NIM Standard compatibility is provided by the Model 222 while CAMAC IEEE-583 (See LeCroy Application Note AN-33) is employed for the Models 2323A and 4222.

Each of these modules has its own unique advantages that enhance its service in certain applications. For example, Model 222 has manual pushbuttons for Start and/or Stop. When a "trigger" is not available, these may be used to simulate missing signals. Model 2323A has an ECL output for compatibility with LeCroy ECLine trigger processor and data handling modules. Model 4222 has four time generators in a single-width module, making it a superior choice in high density systems where space is at a premium.

Arbitrary gate widths are provided for in the Models 222 and 2323A via a latch-mode operation where the gate duration is determined by externally applied Start and Stop signals. Further versatility is incorporated into these modules by including a delayed output pulse which occurs at the end of each gate output pulse and has a preset width.

Precision delayed gates can be produced with any LeCroy Gate and Delay Generator Module. Gate signals can be used to set coincidence time windows, provide veto signals, or generate fast clear signals after some preset delay. Latch Mode operation, available in either the Model 222 or the Model 2323A, permits gating-off front-end electronics after receipt of a valid trigger signal and maintaining this state until data acquisition is complete. For example, discrimi-

nators may be vetoed immediately after the trigger electronics generates the ADC gates. This insures that no further ADC gates are generated.

Since each LeCroy Gate and Delay Generator Module has at least two independent generators, one generator can be used as a precision delay. A delayed output pulse, occurring at the end of the gate pulse, is applied to the Start of a second generator. The second generator then produces a precision pulse that is delayed by the first generator. Both Model 222 and Model 2323A may be configured this way. Delayed gate operation of the Model 4222 is provided by side-panel accessible switches which couple two channels together, providing either one or two such generators.

NIM MODEL 222

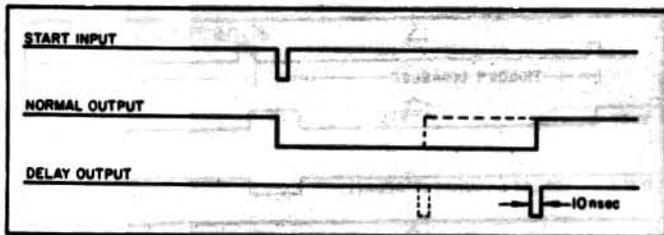
The LeCroy Model 222 Dual Gate and Delay Generator provides two complete delay/gate channels in a single NIM module. This combines many important features formerly requiring separate expensive circuits into one compact package.

The Model 222 eliminates the problems exhibited by previously available gate generators. There is negligible recovery time associated with the unit at any width setting; it may be retrigged immediately after the gate returns to its quiescent state in all ranges. Each channel of this single module can also be used to provide delays and gate outputs and to drive bin gates in its own NIM bin (LeCroy Model 1403) and

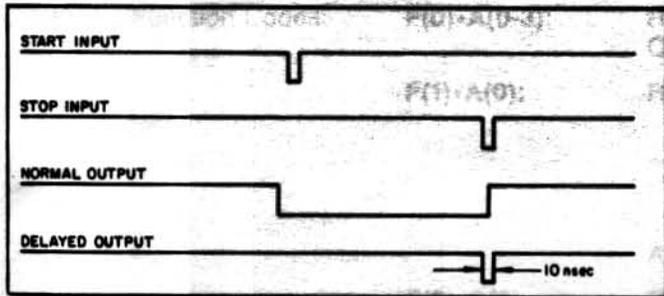
several external bins. In addition, an OR input for each channel permits the gate and delay interval to be extended by an external input.

The Model 222 provides a range switch and a screwdriver-adjustable potentiometer to permit continuous adjustment of gate durations from less than 100 nsec to greater than 11 seconds. A front-panel LED remains on when gate output is present, even if extended by the OR input. The approximate gate setting may be easily determined without an oscilloscope by means of the front-panel monitor point, which provides a DC voltage related to the gate duration. A conversion graph is enclosed with the unit. In addition to preset width ranges, the range switch has a "Latch" position to provide a continuous gate controllable by either the "Start" and "Stop" inputs or by the "Start" and "Stop" pushbuttons. Front-panel "Start" and "Stop" pushbuttons permit manual operation when full scale switch is set on "latch", and single-shot presettable operation when full scale switch is in any other position.

MODEL 222 DUAL GATE GENERATOR TIMING DIAGRAMS



PRESETTABLE WIDTH MODE



LATCH MODE

Each channel has one rear-panel Lemo connector that drives external bins using either normal or inverted logic (switch selectable). A rear-panel 3-position switch (A/B/OFF) determines which channel drives the bin in which the Model 222 is located.

CAMAC MODEL 2323A

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LeCroy's CAMAC Model 2323A is a fully programmable Gate and Delay Generator packaged with 2 channels in a double-width CAMAC module. Its Gate duration is programmable over the range 100 nsec to 10 seconds, covering a dynamic range of eight orders of magnitude. Moreover, outputs as short as 50 nsec can be selected at the expense of accuracy and stability. All settings may be programmed under CAMAC control or via front-panel controls. The settings of the instrument are battery backed-up, so the unit does not have to be reprogrammed after turning the crate off/on or after a power failure. The Model 2323A offers excellent stability and jitter properties with 0.2% of Full Scale accuracy in the gate setting.

The Model 2323A offers both Start and Stop inputs. This allows the output pulse width to be determined by the Start-Stop time difference in the latched mode or by the internal timer in the preset mode. A Blanking NIM input causes a notch to be taken out of the gate, equal in duration to the Blanking input. This is especially useful to gate off data acquisition during spurious periods. Conversely, a NIM OR input causes all outputs to be set to True for the duration of the OR inputs.

The unit offers NIM and NIM outputs equal in duration to the gate width selected. In addition, a DELAY output is produced at the trailing edge of the Gate pulse. The Model 2323A also provides a differential ECL output and a TTL output capable of driving a NIM Bin Gate. Both the ECL and TTL outputs may be driven from either the Gate or Delay circuit. These options are selected by board-mounted shorting plugs.

The Gate duration and the width of the Delayed output are both programmable under CAMAC control. Each of the two channels are programmed independently. All values which are loaded into the Model 2323A may also be read back via CAMAC. Programming the delay involves a 10-bit "mantissa" and a 3-bit "characteristic".

The Start input is normally configured to accept NIM signals. A bridged high impedance input is employed to allow the trigger of more than one channel of 2323A. The front end of the Start input consists of a comparator circuit, factory adjusted to trigger at -400 ± 50 mV. A front-panel accessed multiple turn potentiometer allows the user to adjust the threshold over the range -3 V to $+3$ V. This allows the unit to be triggered by NIM, ECL, TTL or other standard logic signals. A front-panel accessed switch selects either the positive-going or negative-going edge as the trigger. The stop input accepts NIM standard pulses.

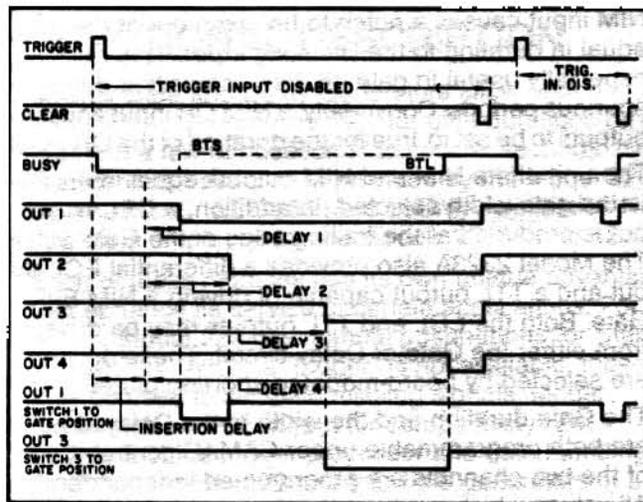
Timing diagrams for the Model 2323A are similar to those of the Model 222.

CAMAC MODEL 4222

The LeCroy Model 4222, Quad, Wide Range, Gate and Delay Generator, produces long, precise time delays and time intervals synchronously with a random Trigger input. All 4 channels of the Model 4222 are started by a common Trigger input. Each channel provides a programmable time delay of up to 16.7 msec in 1 nsec increments. All programming is under CAMAC control.

Three outputs are provided for each channel. One output provides NIM-level signals which go "True" after the programmed time delay and is reset by the Clear. Another output gives complementary NIM logic output. Each channel has a corresponding delayed pulse output that provides a 5 V fast risetime signal into 50 Ω occurring after the programmed time delay.

MODEL 4222 TRIGGER TIMING DIAGRAMS

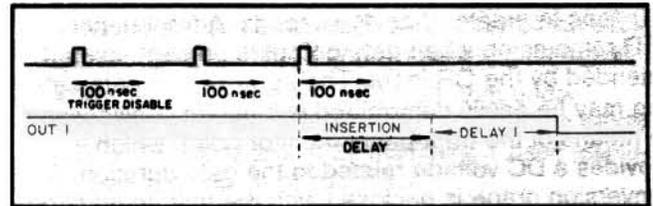


NON-RETRIGGER MODE

(RETRIGGER ACTION switch: SET TO RETRIGGER DISABLED)

The Model 4222 may be set to Retrigger Mode (side switch selectable) permitting the unit to retrigger without being reloaded. In Retrigger Mode, a second side switch permits two options:

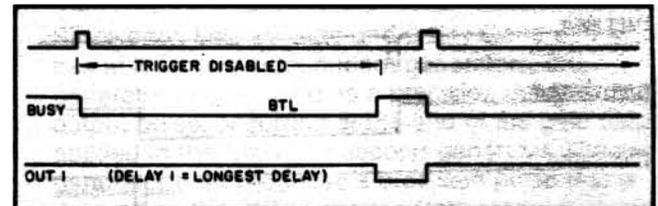
The unit may be retriggered any time 100 nsec after the last trigger, or any time after the longest delay has elapsed.



RETRIGGER BEFORE END OF DELAY

(RETRIGGER ACTION switches: SET TO RETRIGGER ENABLED
RETRIGGER BEFORE END)

Synchronization of many Model 4222 Gate and Delay Generators is possible. An external clock may be used to feed several Model 4222 modules with an identical time base. Stability and accuracy are then determined by the external clock.



RETRIGGER AFTER END OF DELAY

(RETRIGGER ACTION switches: SET TO RETRIGGER ENABLED
RETRIGGER AFTER END)

CAMAC COMMANDS AND FUNCTION CODES

Model 2323A Dual Programmable Gate and Delay Generator

CAMAC Commands:	C or Z:	Stops channels A and B gates.
	X:	X response is generated for each valid function.
	Q:	Q response is generated for each valid function unless otherwise specified.
CAMAC Function Codes:	F(1)•A(0):	Read channel A programming word.
	F(1)•A(1):	Read channel B programming word.
	F(9)•A(0):	Stop channel A gate.
	F(9)•(1):	Stop channel B gate.
	F(17)•A(0):	Write channel A programming word.
	F(17)•A(1):	Write channel B programming word.
	F(25)•A(0):	Start channel A gate.
	F(25)•A(1):	Start channel B gate.

Model 4222 Quad, Wide Range Gate and Delay Generator

CAMAC Commands:	Z:	Initializes module, resets all channels, disables trigger input and enables CAMAC access (does not reset data registers).
	C:	Resets all channels (does not reset data registers), equivalent to front-panel Clear input.
	I:	Disables trigger input when present.
	X:	X response is generated for each valid function.
	Q:	Q response is generated for each valid function unless otherwise specified.
CAMAC Function Codes:	F(0)•A(0-3):	Reads selected programmed delay for channels 1-4 in 24 bits; Q = 1 always; 24-bit unsigned integer convention.
	F(1)•A(0):	Reads status via Read Lines 1-4: R1 = 1 if shortest delay elapsed; R2 = 1 if longest delay elapsed; R3 = 1 if Model 4222 is ready for trigger; R4 = 1 if CAMAC access enabled.
		All states are strobed by the leading edge of the CAMAC N signal.
	F(9)•A(0):	Resets all channels (does not reset data registers) equivalent to external Clear input.
	F(16)•A(0-3):	If CAMAC access enabled, writes delay to selected channel 1-4 in 24 bits. Q = 1 if CAMAC access enabled; Q = 0 otherwise. 24-bit unsigned integer convention.
	F(24)•A(0):	Disables unit; enables CAMAC access.
	F(25)•A(0):	Triggers the unit (OR'd with the external front panel Trigger input): Q = 1 if unit was ready for Trigger; Q = 0 otherwise.
	F(26)•A(0):	Enables unit; disables CAMAC access.

TECHNICAL INFORMATION

MODEL	222	2323A	4222
General			
Packaging	Single-Width NIM	Double-Width CAMAC	Single-Width CAMAC
START Input:	NIM or TTL	-3 V to +3 V	-1.5 V to +1.5 V
STOP Input:	NIM	NIM	NIM (Clear input)
GATE WIDTH			
Range:	100 nsec to 11 seconds or Latch Mode	100 nsec to 10 seconds or Latch Mode	1 nsec to 16.777215 msec
Jitter:	0.05% of setting	<0.3% of setting	150 psec RMS max.
Accuracy:	-	±0.2% of full scale	±200 psec ±time base error
Resolution:	continuous	0.1% of full scale	1 nsec
Input to Output Delay:	14 nsec	24 nsec	170 nsec typical
DELAYED OUT			
Width:	10 nsec	10, 30, 100 or 300 nsec	100 nsec ±10%
Occurs:	Approximately at trailing edge of gate signal	Trailing edge of gate pulse	At end of delay
Risetime:	2.5 nsec max.	2 nsec max.	1 nsec
Signal:	NIM into 50 Ω	NIM (-16 mA)	5 V into 50 Ω
ADDITIONAL OUTPUTS			
TTL:	Quiescent 0 V; > +2.5 V into 50 Ω during pulse.	FET open drain output (+35 V Max, 250mV, 0.5W Max)	-
ECL:	-	Differential ECL (-0.8 V and -1.6 V)	-
TTL/ECL:	Selectable by internal jumpers to correspond to either the NIM or DELAYED outputs or their complements.		
GENERAL			
Power Consumption:			
24 V	+45 mA/-80 mA	+50 mA/-75 mA	+40 mA/-130 mA
12 V	+95 mA/-180 mA	-	-
6 V	+235 mA/-0 mA	+1.8 A/-1.3 A	+1.3 A/-2.5 A
	7.7 W	21.6 W	26.9 W

*Taken from +12 V if +6 V unavailable.

SECTION I
SPECIFICATIONS

1.2 Input Characteristics

1.2.1 START and STOP Inputs

The START and STOP inputs respond to either fast NIM* or TTL level inputs. Since the Model 222 input circuit automatically responds to either type of signal, no switch selection or internal change is necessary. A fast NIM input drives an impedance of 50 Ω , however the input is high impedance for TTL levels. A TTL input requires 5 mA at +2.5 V, increasing slightly as the input voltage is increased (i.e., 5.75 mA at +3.5 V). Protection is provided for currents of up to ± 5 A for 1 μ sec by a 47 Ω series-terminating resistor, clamping at 0 V for negative pulses and at +6 V for positive pulses.

It is important to note that the STOP input (or STOP pushbutton) is only intended for use with the FULL SCALE WIDTH switch in the LATCH mode. However, if a Stop is applied while an output is present with the FULL SCALE WIDTH switch set at a finite range, the output pulse will nevertheless be terminated, but only after a short delay.

1.2.2 BLANK Input

The BLANK input responds to fast NIM level* inputs. Input impedance is 50 Ω and input protection extends to at least ± 5 V. The blanking input suppresses only the portion of the Model 222 output pulse occurring during the blanking interval. The delayed output pulse is also suppressed on the standard unit.

1.2.3 OR Input

The OR input responds to fast NIM level* inputs, has a 50 Ω impedance, and is protected to at least ± 5 V. Its specific function is to enable the user to easily extend the preset output width on the basis of external criteria, (e.g., extending an input inhibit to scalars or other data acquisition modules while a computer readout is still in progress).

* Fast NIM Levels:
TTL Levels:

-12 mA	{	Logical 1	{	-36 mA
+2.0 V	{	Logical 1	{	+5.0 V

1.3 Output Characteristics

1.3.1 Gate Outputs

General

The Model 222 provides one standard fast NIM level output (quiescently 0 V, -750 mV during pulse) of approximately 2 nsec risetime, one complementary fast NIM level output (quiescently -750 mV, 0 V during pulse), and one TTL level output (quiescently 0 V, <+2.5 V into 50 Ω during pulse). The falltime of the fast NIM outputs is generally similar to the risetime, except at large output widths where the Model 222 timing stage causes a slight degradation of the falltime.

Gate Durations:

Preset output durations extend from <100 nsec to >11 sec and are determined by a combination of the FULL SCALE WIDTH selector switch and the screwdriver-adjustable vernier. On the BNC version (Model 222N), a lock-in potentiometer replaces the switch and vernier, giving direct visual indication of output width setting. On the LEMO Model 222, a DC level available at the front panel test point gives an indication of the output width setting as a percentage of the FULL SCALE WIDTH switch setting, from approximately 10% to 110%. The conversion chart representing this test point output is shown in Fig. 1.1.

When the output width range selector switch is set in the LATCH position, the output width of the Model 222 is determined by either the START and STOP pushbuttons, or the START and STOP inputs. Once "started", the Model 222 output will stay on indefinitely until "stopped" or until power is turned off.

1.3.2 Delayed Output

The delayed output (DEL) delivers a 10 nsec FWHM (Full Width Half Maximum) fast NIM level signal into 50 Ω . The leading edge of this output occurs shortly before the trailing edge of the normal gate output pulse. In other words, its leading edge occurs a few nsec before the normal gate output is fully completed.

The delayed output is normally suppressed by the BLANK input, but this feature may be disabled by factory option. This output is often useful for creating a "delay and gate generator" using two channels of the Model 222. In this case, either the delayed output or the complementary output of Channel 1 can be fed into the START input of Channel 2 of the Model 222 to create an output pulse of specified width occurring at a time determined by the output width setting of Channel 1. More standard applications involve using the delayed output to trigger a computer readout cycle, as a reset pulse, or as a "flag" pulse to indicate the completion of a data acquisition interval.

1.3.3 Bin Gate Driver Outputs

For Remote Bins:

The Model 222 provides a rear panel LEMO connector output which switch-selectably drives external bins in either the normal or inverted direction. For the normal direction, the Model 222 will clamp 200 mA for a Logical 1 (less than 1 volt). A Logical 0 is a high-impedance open-collector-type output. A 2 k Ω resistor provides pull up to +5.2 V.

NOTE: The NORMAL position disables the driven bin for the duration of the Model 222 output. The INVERTED position enables a normally disabled bin during the gate output interval.

For Driving the Local Bin:

Either Channel 1 or Channel 2 of the Model 222 can drive the bin from which the unit is powered. A rear panel 3-position switch selects which channel, with the third position (OFF) available to disassociate the local bin from the influence of the Model 222. The NORMAL position serves to disable the driven bin for the duration of the Model 222 gate output.

1.4 Recovery Time

With the Model 222, it is possible to get a second gate output immediately after the first gate output. In this respect, no delay period (deadtime) is required before the Model 222 can be retriggered. This feature is made possible by the OR'ing of two internal signals to create one output signal with a width corresponding to the front panel rotary switch setting and vernier.

1.5 BUSY Indicator

The Model 222 provides a front panel LED (light-emitting diode) indication when a gate output is present. This LED lights whenever an output is present, even if extended by an OR input. Because no mechanism is provided to slow down the turning on and off of the LED for each gate output, at short output widths or high rates, the LED will appear to the eye as a steady "on" condition.

1.6 Packaging

The Model 222 is packaged in a standard NIM module conforming to the standards outlined in AEC-NIM Report TID 20893, Rev. 3. The LEMO connector version has a #1 front panel width, while the BNC version utilizes a #2 width due to the size of the front panel lock-in potentiometer and the BNC connectors.

1.7 Current Requirements

The Model 222 dissipates 7.5 watts and requires the following NIM voltages and currents:

mA

mA
mA

d a mA h v d p l i ly d
 2 mA v h v p l i able
 wh y v y y p th Mod

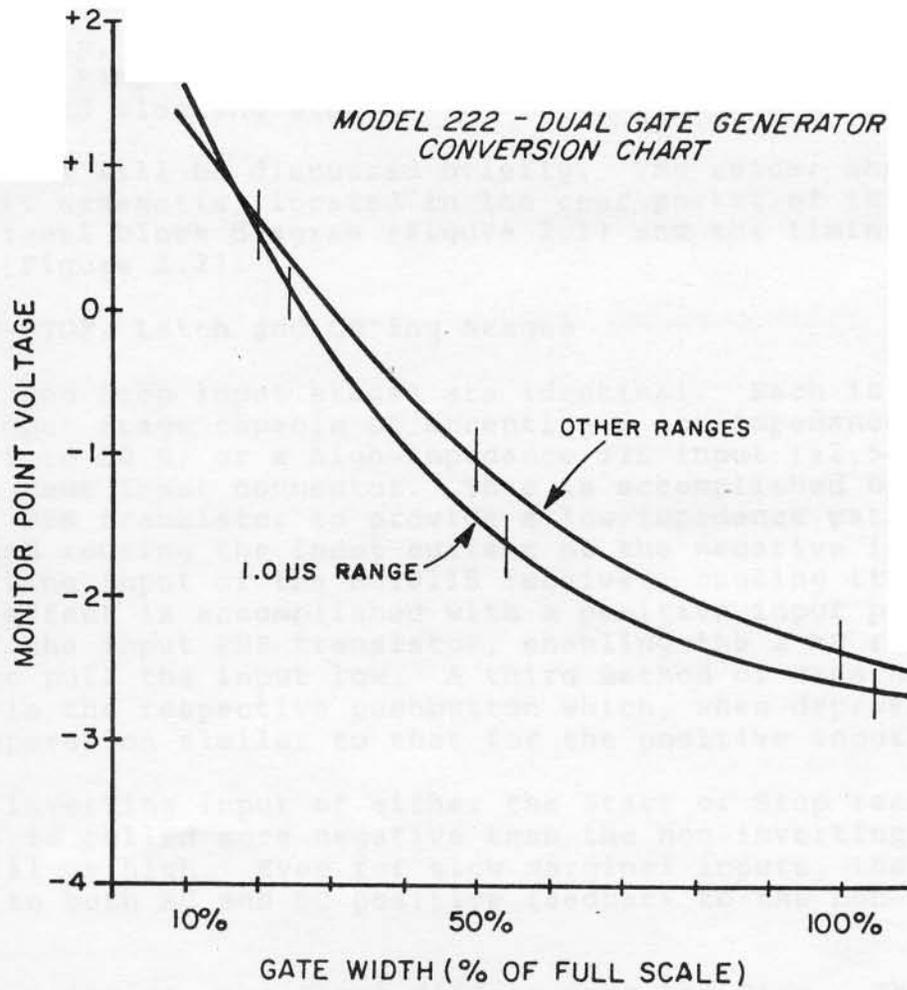


Figure 1.1

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 General

The Model 222 is a two-channel NIM module. It can be divided into three major sections:

The Start-Stop, Latch and OR'ing stages
 The Ramp and Ramp Level Detector stages
 The Output and Blanking stages

Each of these will be discussed briefly. The reader should refer to the circuit schematic (located in the rear pocket of this manual), the functional block diagram (Figure 2.1) and the timing waveform diagrams (Figure 2.2).

2.2 START-STOP, Latch and OR'ing Stages

The Start and Stop input stages are identical. Each is composed of a special input stage capable of accepting a low-impedance NIM input (-500 mV into 50 Ω) or a high-impedance TTL input (+2.5 V at 5 mA) using the same input connector. This is accomplished by requiring the input NPN transistor to provide a low-impedance path for negative signals and routing the input current of the negative input signal to the inverting input of the MC10115 receiver, causing it to go low. The same effect is accomplished with a positive input pulse, which turns off the input PNP transistor, enabling the 2 k Ω resistor on the MC10115 to pull the input low. A third method of causing a Start or Stop is via the respective pushbutton which, when depressed, causes circuit operation similar to that for the positive input.

When the inverting input of either the Start or Stop receivers (MC10115) is pulled more negative than the non-inverting input, the output will go high. Even for slow marginal inputs, the output is fast due to both AC and DC positive feedback to the non-inverting input.

From this point on, the Start differs from the Stop. The Start is first differentiated and the resulting "leading-edge" pulse is shaped by an emitter-coupled logic (ECL) receiver (which is inhibited if the Ramp section is already busy). The resulting pulse is then used to set the Latch, (composed of a heavily fed-back section of ECL receiver), by forcing the Latch output positive. (See "Pre-settable Width Mode" timing diagram in Figure 2.2). This pulse is present for the duration of the Latch and is fed to the Ramp section to start the ramp cycle as well as to provide a prompt input to the final OR stage which is used to drive the output stage.

Once a ramp is generated (see Section 2.3), the Ramp Detector output is fed to the OR along with the Latch output to hold the output stage "on" and inhibit the Start input for the entire ramp duration. At the maximum amplitude of the ramp, the Stop-level Detector (in the

Ramp section) will reset the Latch, but the output of the final OR will still be present until the ramp is totally recovered, at which point the Ramp Detector will return to its quiescent level, removing drive from the output stage.

The STOP input is intended primarily for use in the LATCH mode of operation. In this mode, the Ramp section is disabled, so the output stage follows the Latch output only. (See "Start-Stop Mode" timing diagram in Figure 2.2). A Stop input will reset the Latch previously set by the Start. Therefore, the output stage will be driven only for the time from Start to Stop. If a Stop input is generated when operating in any of the preset modes, it will reset the Latch before the end of the ramp, causing the ramp to be shortened, but because the output stage follows the total ramp duration, the output width will not be promptly terminated, but will be extended by the ramp recovery time (which depends on both the range setting and the amount of preset time which had already elapsed before the Stop was generated).

The input OR stage converts NIM levels to offset ECL levels required to drive directly the final OR stage, independent of the states of the Start-Stop stage, the Latch, the Ramp stage, etc. Thus it provides a final output width equal to the input OR width (or to the overlap of it and the Start-Stop Latch and/or the Ramp Detector).

2.3 Ramp and Ramp Detector Stages

The Ramp stage is composed of a capacitor, C_n ($n=1,2\dots 8$, as selected by the FULL SCALE WIDTH switch), resistor $R1^n$ (paralleled by $R2$ on the 1.0 μsec range), and a 10 mA current source (transistor Q15). The current source is quiescently on, causing the ramp to be clamped at about +3 V by the 1N702 zener diode and the base-emitter drop of Q2. When the Start-Stop Latch is set by a Start pulse, the Q15 current source is disabled and the ramp begins to discharge toward -3 V at a rate determined by $R1$ (15 k Ω , or 7.5 k Ω when paralleled by $R2$ on 1.0 μsec range) and C_n which is determined by the FULL SCALE WIDTH switch setting. (See "Presettable Width Mode" timing diagram in Figure 2.2).

As soon as the current source is turned off, the integrated circuit comparator used as the Ramp Detector is enabled because the collector of Q15 goes to zero. When the ramp reaches the voltage level set by the 2 k Ω front panel vernier width potentiometer, the Stop-level Detector comparator I.C. resets the Start-Stop Latch. This enables the current source and the ramp is returned to its quiescent level at a rate determined primarily by the 10 mA of the current source and the value of C_n . When the ramp reaches the clamp level determined by transistor Q2, the current is shunted to Q2 collector, the Ramp Detector turns off, the output drive to the ECL final OR and the inhibit to the Start stages are removed, and the unit can be retriggered.

2.4 Output and Blanking Stages

The NIM driver output stage is a 16 mA differential stage operating

from the output OR (with a 5 nsec stretcher stage) via a 1N706 zener diode to provide level shifting. Both the normal and complementary outputs are made available and they are individually clamped at -1 V if no output load is present.

The TTL and Bin Gate output stages and the BUSY LED driver are driven from a stage the same as above except that the collectors are referenced to positive voltages. The TTL stage uses a double emitter-follower to provide stiff drive for either logic level. The Bin Gate output uses one of two switch-selectable, stiff, clamp-to-ground inverting transistors. One provides a normal level to inhibit modules on the bin gate bus for the duration of the output. The other provides an inverted level to inhibit quiescently and to enable only during the output duration. The Busy driver holds the BUSY LED on for the duration of the output, stretching short pulses enough to provide a visual indication.

The Delayed Output stage is also similar to the NIM driver stage, except that only the normal output (quiescently zero, -16 mA during pulse) is available and the stage is driven from a trailing-edge differentiator-shaper stage to generate a 10 nsec wide pulse.

The Blanking input converts a NIM level input to a proper level to disable the three differential stages, and therefore all outputs and the BUSY LED, for the duration of the Blanking input.

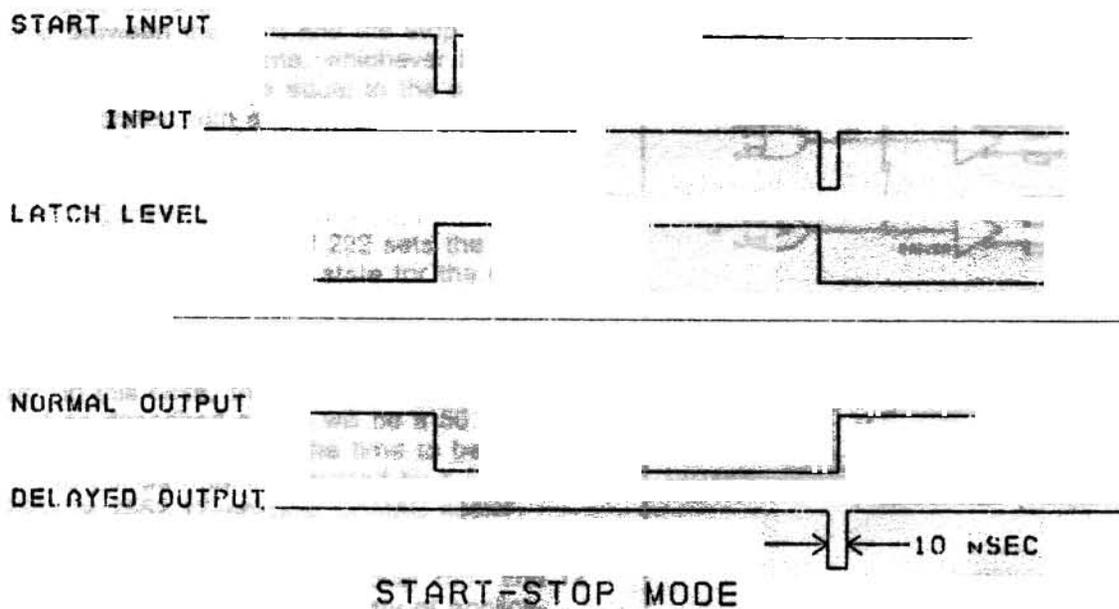
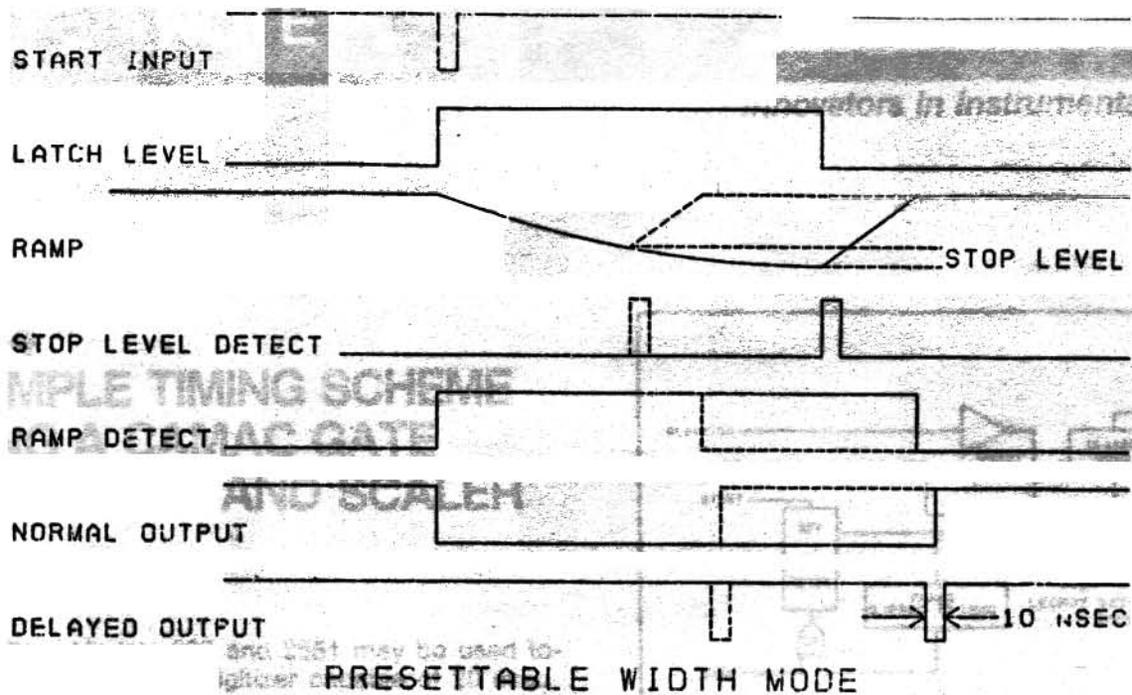
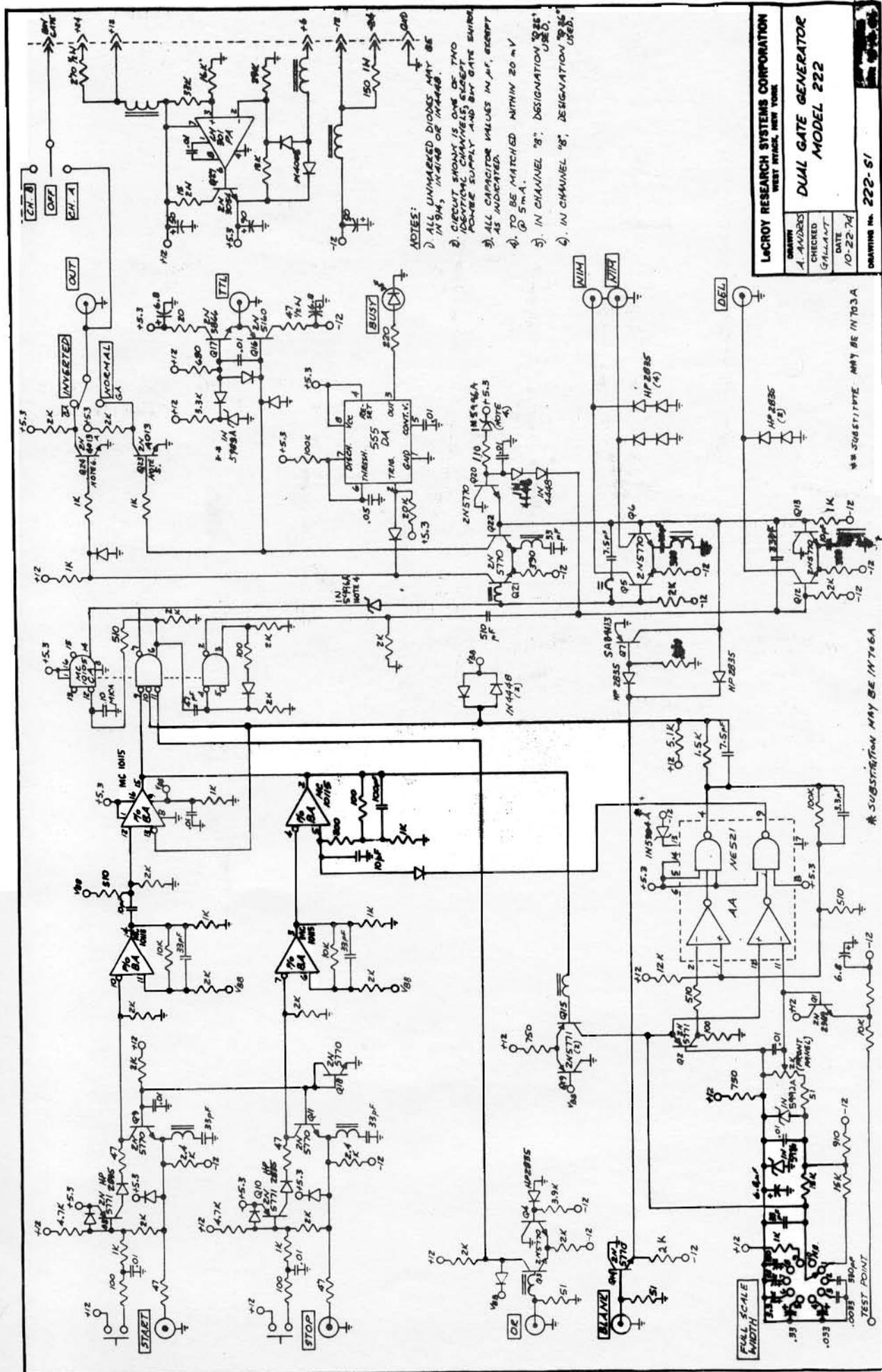


Figure 2.2



- NOTES:
1. ALL UNNUMBERED DIODES MAY BE IN 94, INSTEAD OF 104448.
 2. CIRCUIT SHOWS IS ONE OF TWO IDENTICAL CHANNELS, EXCEPT POWER SUPPLY AND BIT GATE SWRCH AS INDICATED.
 3. ALL CAPACITOR VALUES IN μ F, EXCEPT AS INDICATED.
 4. TO BE MATCHED WITHIN 20 mV.
 5. IN CHANNEL "B", DESIGNATION "285" USED.
 6. IN CHANNEL "B", DESIGNATION "286" USED.

LCRODY RESEARCH SYSTEMS CORPORATION
WESTY BRIDGE, NEW YORK

DUAL GATE GENERATOR
MODEL 222

DRAWN	A. AM/2005
CHECKED	GALLANT
DATE	10-22-74

DRAWING NO. 222-51

** SUBSTITUTION MAY BE IN 703A

* SUBSTITUTION MAY BE IN 706A

FULL SCALE WIDTH
TEST POINT