

TM-451A/E

SERVICE MANUAL

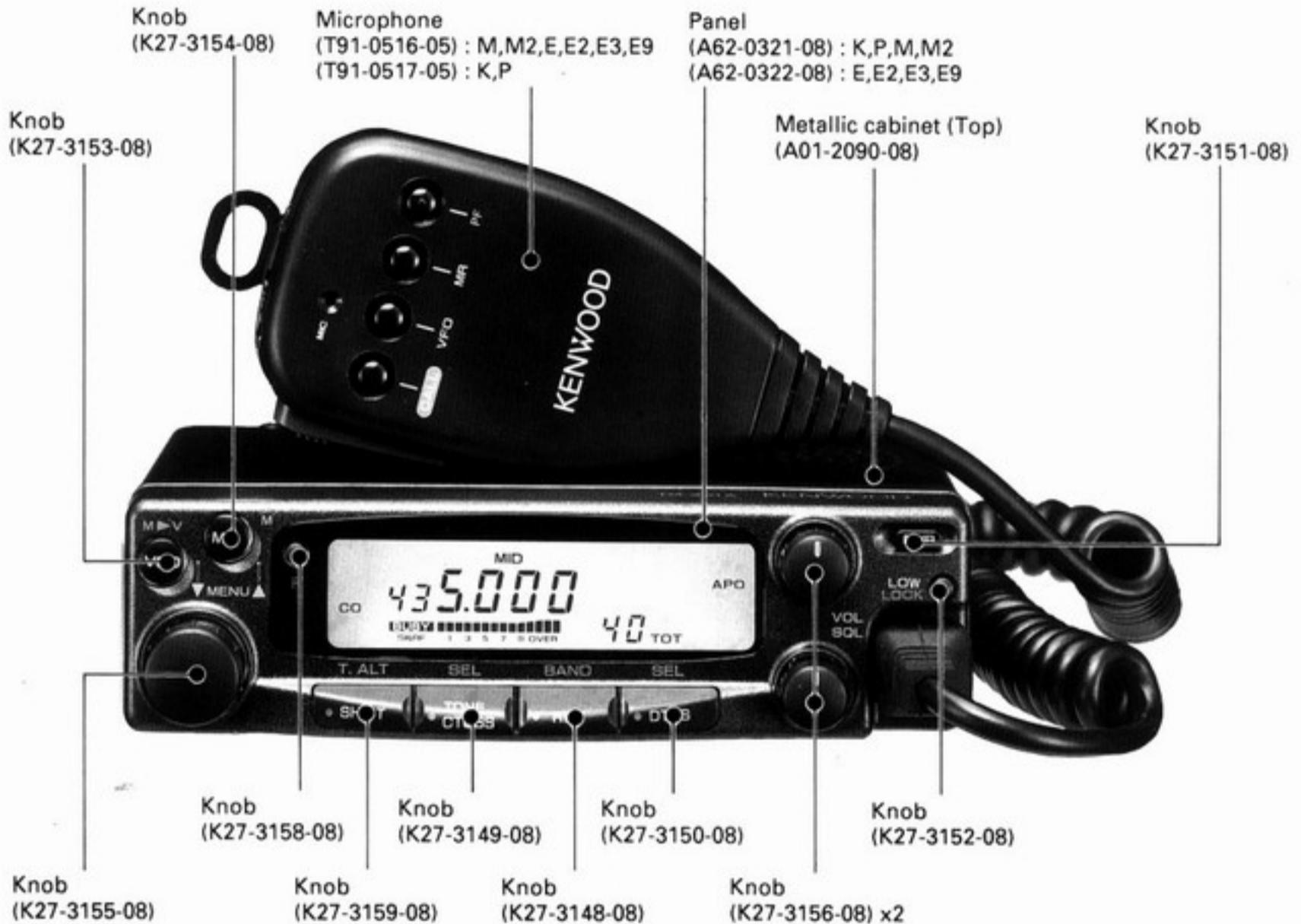


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CIRCUIT DESCRIPTION

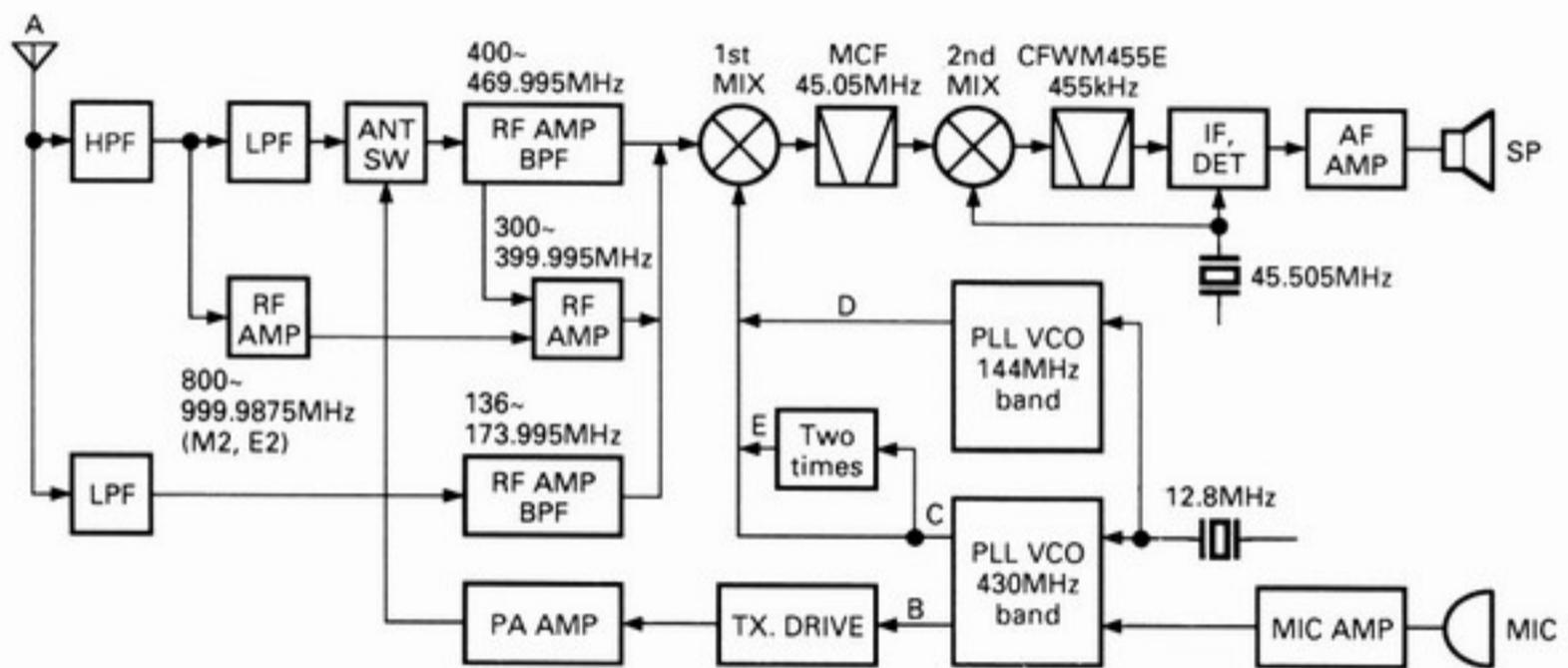
Frequency Configuration

The TM-451A/E transceiver incorporates a digital variable frequency oscillator (VFO), based on a phase-locked loop (PLL) synthesizer system, allowing a channel step of 5, 10, 12.5, 15, 20, or 25kHz.

The receiver is a dual-band type covering the 144 and 430MHz bands. Double conversion is used, in which the received signal is mixed with a first local oscillator frequency of 345.05 to 445.045MHz, 354.95 to 424.945MHz (K,P,M2,E2), and 384.95 to 394.945MHz (M,E,E3,E9) for 430MHz band reception, or 181.05 to

219.045MHz (K,P,M2,E2), 189.05 to 193.045MHz (M), and 189.05 to 191.045MHz (E,E3,E9) for 144MHz band reception, to produce the 45.05MHz first IF. The first IF signal is then mixed with the second local oscillator frequency of 45.505MHz to produce the 455kHz second IF.

The signal in the transmitter system is directly oscillated and frequency-divided by a PLL circuit, and amplified by a linear amplifier, then transmitted.



- | | |
|---|--|
| <p>A : TX 438~449.995MHz (K, P)
430~439.995MHz (M, E, E3, E9)
400~469.995MHz (M2)
410~469.995MHz (E2)</p> <p>RX 300~469.995MHz (K, P, M2, E2)
430~439.995MHz (M, E, E3, E9)
136~173.995MHz (K, P, M2, E2)
144~147.995MHz (M)
144~145.995MHz (E, E3, E9)
800~999.9875MHz (M2,E2)</p> | <p>B : 438~449.995MHz (K, P)
430~439.995MHz (M, E, E3, E9)
400~469.995MHz (M2)
410~469.995MHz (E2)</p> <p>C : 345.05~445.045MHz UPPER (K, P, M2, E2)
354.95~424.945MHz LOWER (K, P, M2, E2)

384.95~394.945MHz LOWER (M, E, E3, E9)</p> <p>D : 181.05~219.045MHz UPPER (K, P, M2, E2)
189.05~193.045MHz UPPER (M)
189.05~191.045MHz UPPER (E, E3, E9)</p> <p>E : 754.95~954.9375MHz LOWER (M2, E2)</p> |
|---|--|

Fig. 1 Frequency configuration

CIRCUIT DESCRIPTION

Receiver System

• Outline

The signal from the antenna passes through a high-pass filter and a low-pass filter in the final transmission stage and then goes through a transmission/reception selection diode switch to the receiving front end, where it is amplified by Q301 and unwanted components eliminated by a band-pass filter. The resulting signal is amplified by Q302 and unwanted components eliminated by another band-pass filter. The resulting signal goes to the first mixer, Q310.

The 144MHz sub-band signal from the antenna passes through a low-pass filter and is amplified by Q303 and Q304, and it goes to the first mixer, Q310.

When RX frequency is 400 to 469.995MHz, unwanted components are removed by a band-pass filter, the resulting signal is amplified by Q302, further unwanted signal components are removed by a band-pass filter, and it goes to the first mixer, Q310.

When RX frequency is 300 to 399.995MHz (K,P,M2,E2), the signal is amplified by Q313 and IC302, and it goes to the first mixer, Q310.

When RX frequency is 800 to 999.9875MHz (M2,E2), the signal is amplified by Q312, Q313 and IC302, and it goes to the first mixer, Q310.

The signal is mixed with the first local oscillator signal from the PLL circuit by the first mixer, Q310, to convert it to the first IF of 45.05MHz. Unwanted near-by signals are removed by a two-stage MCF. The first IF signal is amplified by Q311 and input to the second mixer Q4. This signal is then mixed with the second local oscillator signal to produce the second IF of 455kHz.

Unwanted near-by signal components are then eliminated by an FM ceramic filter and input to the FM IF HIC (IC1). The signal is amplified to the second IF signal level and FM-detected to produce an audio signal.

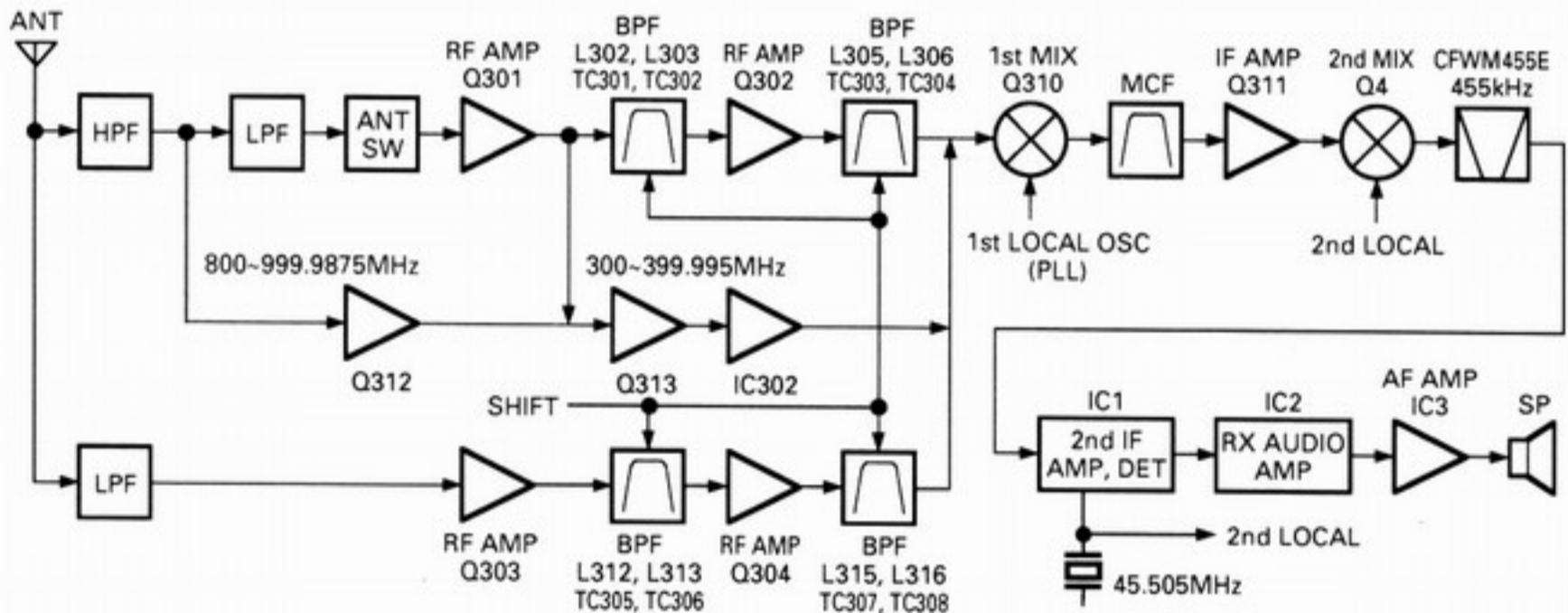


Fig. 2 Receiver system configuration

Item	Rating
Nominal center frequency	45.050MHz
Pass bandwidth	±7.5kHz or more at 3dB
Attenuation bandwidth	±22kHz or less at 25dB ±35kHz or less at 40dB
Guaranteed attenuation	80dB or more at ±890~930kHz Spurious: 40dB or more within ±1MHz
Insertion loss	1dB or less
Ripple	3.0dB or less
Terminating impedance	800Ω/2pF

Table 1 MCF characteristics

Item	Rating
Nominal center frequency	455kHz
6dB bandwidth	±7.5kHz or more
50dB bandwidth	±15kHz or less
Pass bandwidth ripple	3dB or less
Guaranteed attenuation	35dB or more at ±100kHz
Insertion loss	6dB or less
I/O impedance	1.5kΩ

Table 2 Ceramic filter characteristics

CIRCUIT DESCRIPTION

• S-meter circuit

The S-meter output voltage of the FM IF HIC IC1 (KCD04) is sent to the control unit and digitized by the CPU to operate the bar meter on the LCD.

• Shift register circuit

The SDT+, SCK+, and LER+ serial data from the control unit are sent to IC5 (BU4094BF) and IC4 (W02-1830-08) to control operations as outlined in the following table.

Pin No.	Name	Function
1	LER+	Enable input
2	SDT+	Serial data input
3	SCK+	Clock input
4	V5	+5V
5	GND	GND
6	SQL C	Squelch level control output *
7	SUB+	Sub reception ON. ON : High
8	360+	360MHz band ON. ON : High
9	800+	800MHz band ON. ON : High

* The SQL C (pin 6) is described in the section "Squelch circuit in the AF signal system".

Table 4 IC4 : W02-1830-08 function table

Pin No.	Name	Function
1	Strobe	Enable input
2	Serial IN	Serial data input
3	Clock	Clock input
4	Q1	Main VCO frequency selection
5	Q2	Sub VCO frequency selection
6	Q3	Packet 1200 bps ON. ON : High
7	Q4	Packet 9600 bps ON. ON : High
8	Vss	GND
9	Qs	Serial data output to IC4
10	Qs'	(Not used)
11	Q8	TX power selection LOW. LOW : High
12	Q7	TX power selection MID. MID : High
13	Q6	(Not used)
14	Q5	Sub PLL circuit ON. ON : High
15	OUTPUT	Output enable. Pulled up to +5V.
16	VDD	5V

Table 3 IC5 : BU4094BF function table

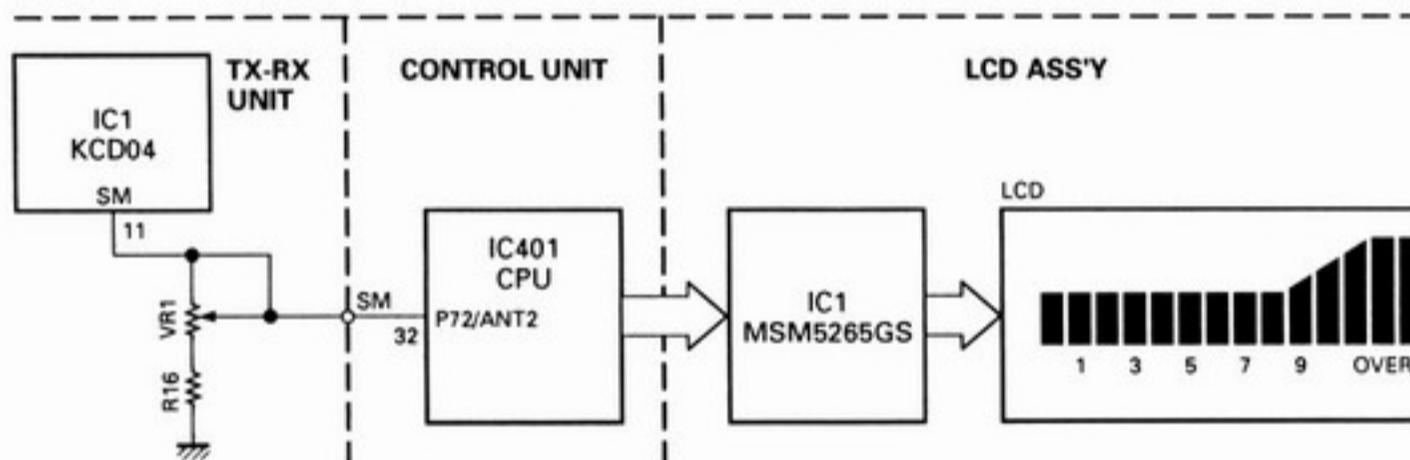


Fig. 3 S-meter circuit

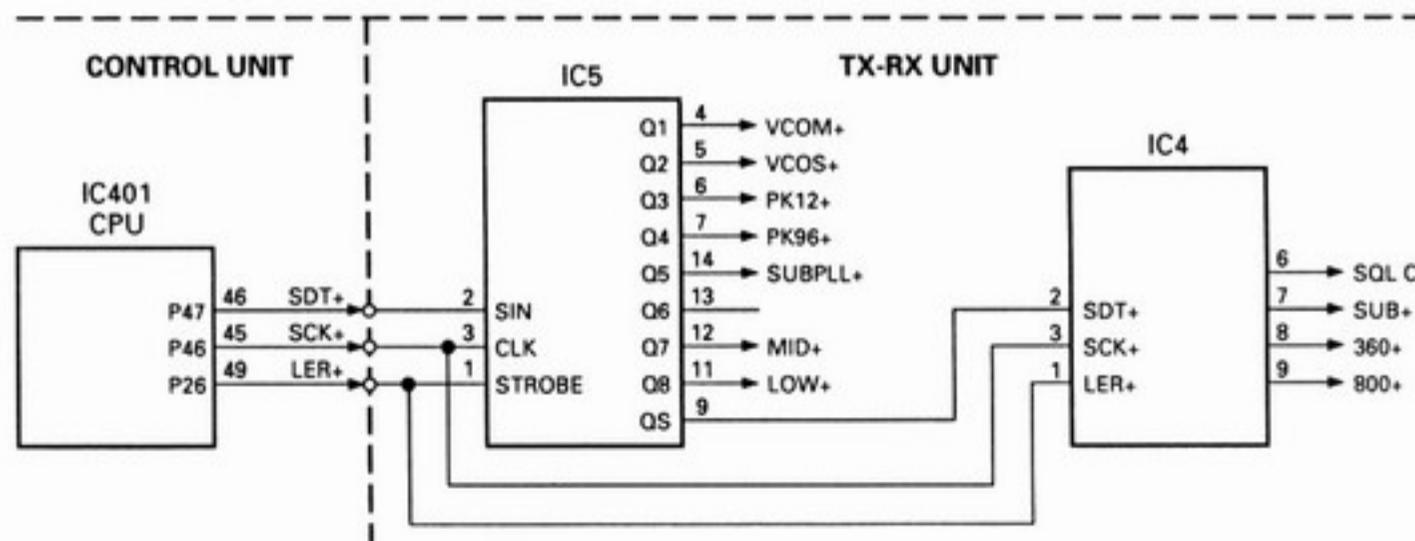


Fig. 4 Shift register circuit

CIRCUIT DESCRIPTION

Transmitter System

• Outline

The transmitter circuit directly produces and modulates the desired frequency by means of a vari-cap diode.

• Modulator circuit

The audio signal from the microphone is amplified by microphone amplifier IC408 in the control unit, and input to IC202 in the TX-RX unit. IC202 consists of a pre-emphasis circuit, amplifier, limiter, and splatter circuit that eliminates unwanted high-frequency components. (See the section "TX audio circuit.") The frequency modulation circuit directly modulates frequency by means of a varicap diode.

• Younger-stage circuit

The signal output from the VCO is buffer-amplified by Q201 and input to RF AMP HIC IC102. The amplifier provides a stable drive output without adjustment because of its wide bandwidth. The APC circuit con-

trols the collector voltage in the Younger final stage.

• Power amplifier circuit

The drive signal is input to power module IC101 and amplified to the specified level.

• APC circuit

The automatic transmission power control (APC) circuit detects part of the power module output with diodes D101 and D102, and generates the VDET detection voltage. The APC circuit compares VDET with reference voltage VREF by mean of transistor Q103, and controls the control voltage with DC amplifiers Q101 and Q102 so that VDET equals VREF, thus keeping the transmission output constant.

The transmission output is switched between low, medium, and high with reference voltage VREF by mean of transistor Q109. The switching signal is output from shift register IC5.

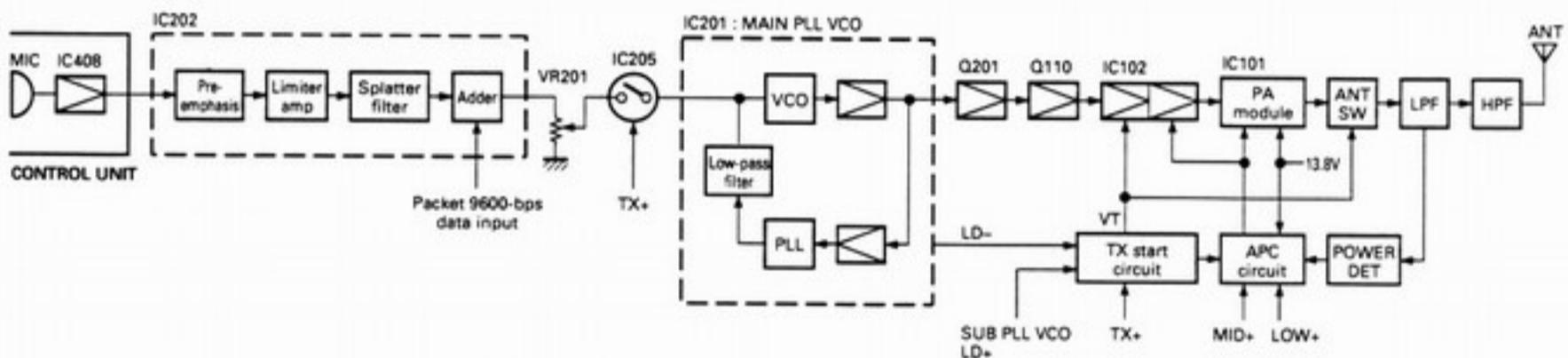


Fig. 5 Transmitter system block diagram

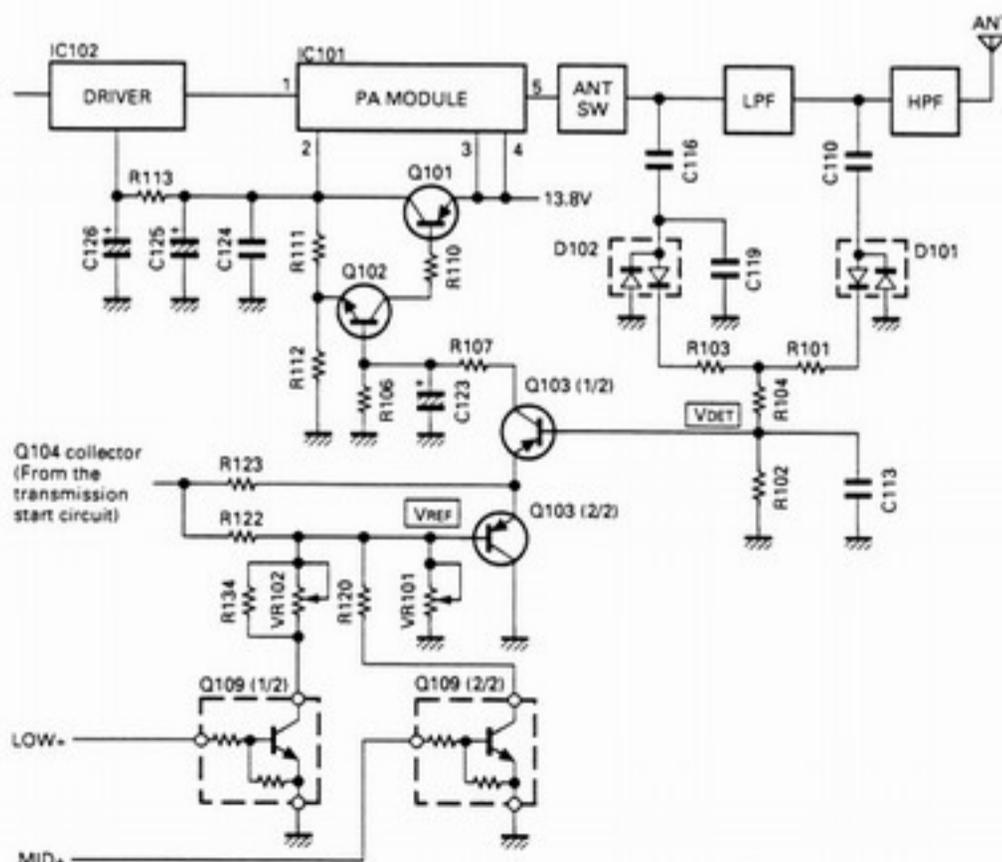


Fig. 6 APC circuit

CIRCUIT DESCRIPTION

• **TX audio circuit (IC202 : W02-1828-08)**

Figure 7 shows the TX audio circuit.

As explained in the description of the modulation circuit, C4 and R5 comprise a pre-emphasis circuit, IC2 (1/2) is a limiter amplifier, R9 and R10 comprise an attenuator, and IC2 (2/2) and its peripheral circuits comprise a splatter filter of 60dB log (f/3k). The output from the splatter filter is summed with the tone and the packet modulation data (9600bps) signal, PKD, that

passes through the IC1 analog switch by IC3 (2/2), and is output as the TX MOD signal.

The PKD packet modulation data signal can be switched to 1200bps or 9600bps by the IC1 analog switch. The switching control signal is output from the shift register circuit IC5 (BU4094BF) as the PK12+ or PK96+ signal. In addition, for the packet demodulation data (1200bps), the RXA signal is amplified by IC3 (1/2) and output as the PKRD signal.

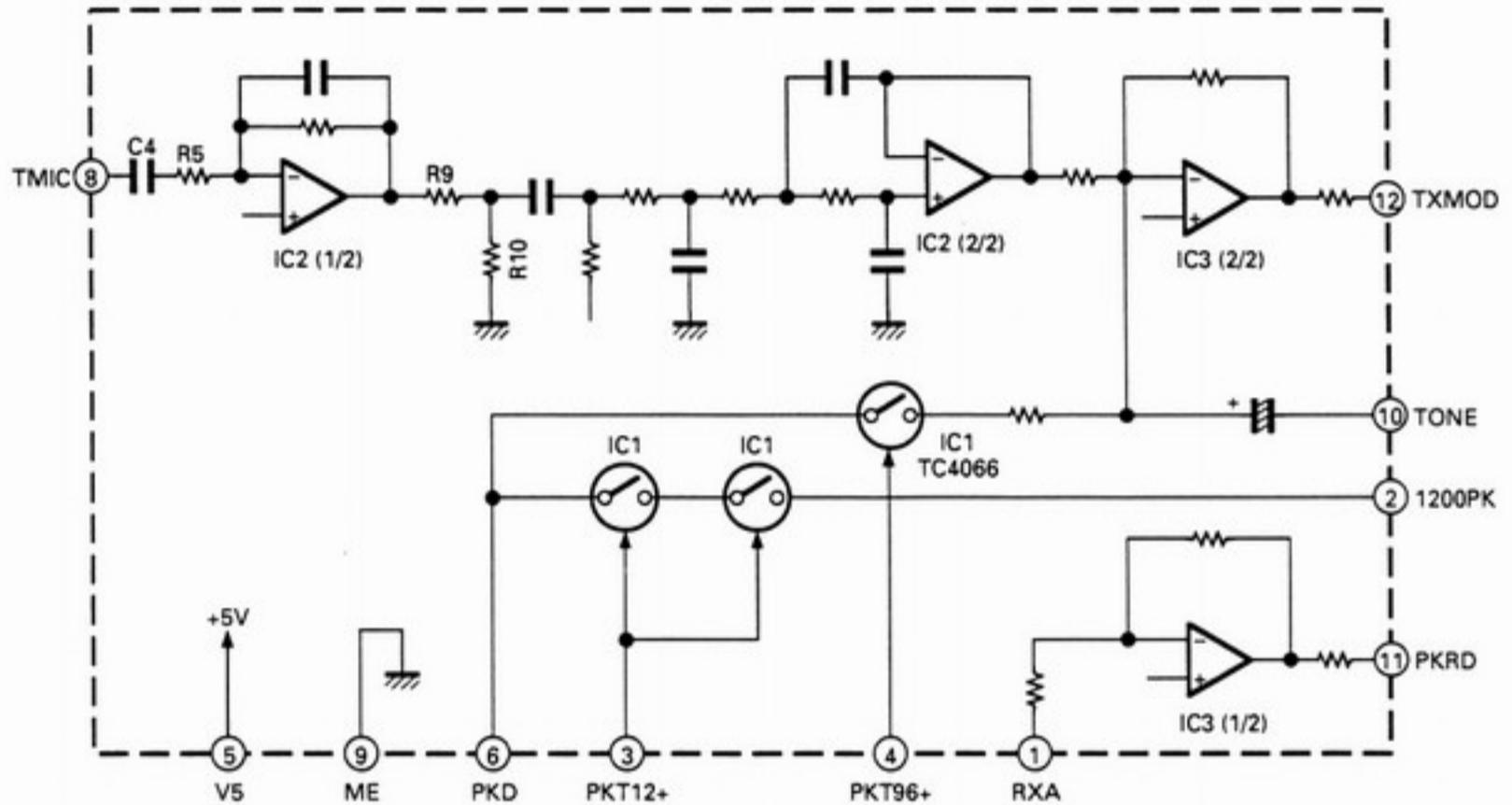


Fig. 7 TX audio circuit (IC202 : W02-1828-08)

CIRCUIT DESCRIPTION

PLL Synthesizer Section

The PLL and VCO circuits are housed in a solid shield case as a hybrid integrated circuit. IC201 (L78-0363-08) is for 430MHz band transmission and reception, and IC203 (L78-0351-08) is for 144MHz band reception. They share the 12.8MHz reference oscillator.

IC201 and IC203 consist of PLL and VCO circuits. The PLL circuit consists of the PLL control IC (IC1 : MB1504L), the operational amplifier (IC3 : NJM3404) that forms a loop filter, RF buffer amplifier Q4, and Q7, which forms an unlock detector.

The VCO circuit consists of the RX VCO (comprising vari-cap diode D3 and oscillation transistor Q1), TX VCO (comprising vari-cap diodes D101, D102 and transistor Q101) that varies the control voltage (VCONT) from the PLL circuit, buffer amplifier Q2, transistor Q3, Q101, which that is controlled via the SHIFT pin according to the oscillation frequency, and modulation vari-cap diode D103. The following paragraphs describe the oscillation frequency and the divide ratio of the PLL circuit.

Comparison frequencies of 5 and 6.25kHz are produced by dividing the 12.8MHz reference oscillator frequency by 2560 or 2048 to correspond to the 5, 10, 12.5, 15, 20 and 25kHz channel steps.

For 144MHz, the relationship between f_{VCO} (RX) and each frequency divide ratio is given by the following equation :

Where :

$$f_{VCO} = (144 + 45.05) = \{ (n \times 64) + A \} \times f_{OSC} + R \text{ [MHz]}$$

f_{VCO} : VCO output frequency

n : Binary 11-bit programmable counter setting value (divide ratio : 16 to 2047)

A : Binary 7-bit programmable counter setting value (divide ratio : 0 to 63)

f_{OSC} : Reference frequency 12.8MHz

R : Binary 14-bit programmable counter setting value (divide ratio : 8 to 16383)

5, 10, 15, 20kHz steps : 2560

12.5, 25kHz steps : 2048

In this case, n is 590 and A is 50.

$$\begin{aligned} \therefore f_{VCO} &= \{ (590 \times 64) + 50 \} \times 12800 + 2560 \\ &= \{ 37760 + 50 \} \times 5 \\ &= 189050\text{kHz} = 189.05\text{MHz} \end{aligned}$$

For 430MHz, the relationship between f_{VCO} (RX) and each frequency divide ratio is given by the following equation:

$$f_{VCO} = (430 - 45.05) = \{ (n \times 64) + A \} \times f_{OSC} + R \text{ [MHz]}$$

In this case, n is 1202 and A is 62.

$$\begin{aligned} \therefore f_{VCO} &= \{ (1202 \times 64) + 62 \} \times 12800 + 2560 \\ &= \{ 76928 + 62 \} \times 5 \\ &= 384950\text{kHz} = 384.95\text{MHz} \end{aligned}$$

The following table lists the pin functions of the PLL VCO circuit :

No.	Name	Function
1	LE	Enable input
2	DT	Data input
3	CK	Clock input
4	V5	5V
5, 6	OSC	12.8MHz crystal oscillator connection
7	LD	Lock signal (Low : Lock)
8	V10	10V
9	OUT	VCO output
10	MOD	Modulation signal input
11	VS8	8V (Ripple filter)
12	VCONT	Lock voltage output
13	GND	Ground
14	SHIFT	Frequency band select signal input

Table 5 Main PLL VCO pin functions (IC201 : L78-0363-08)

No.	Name	Function
1	LE	Enable input
2	DT	Data input
3	CK	Clock input
4	V5	5V
5	Xin, Xout	12.8MHz crystal oscillator connection
6, 10	Xout, MOD	Not used
7	LD	Lock signal (Low : Lock)
8	V10	10V
9	OUT	VCO output
11	VS8	8V (Ripple filter)
12	VCONT	Lock voltage output
13	GND	Ground
14	SHIFT	Frequency band select signal input

Table 6 Sub PLL VCO pin functions (IC203 : L78-0351-08)

CIRCUIT DESCRIPTION

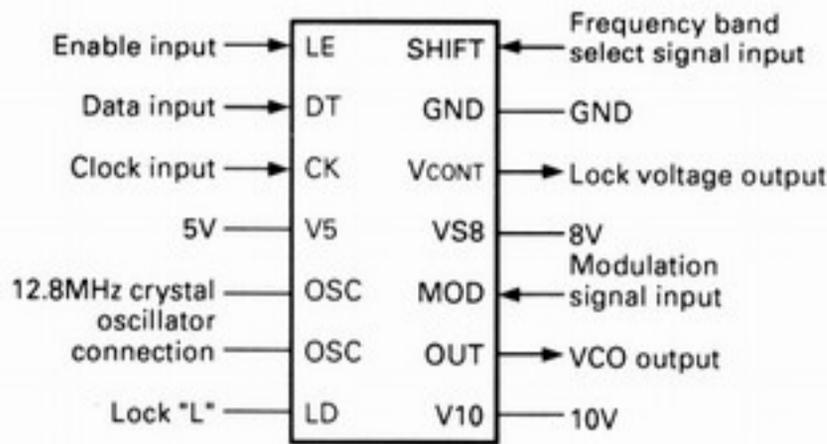


Fig. 8 Main PLL VCO pin description (IC201 : L78-0363-08)

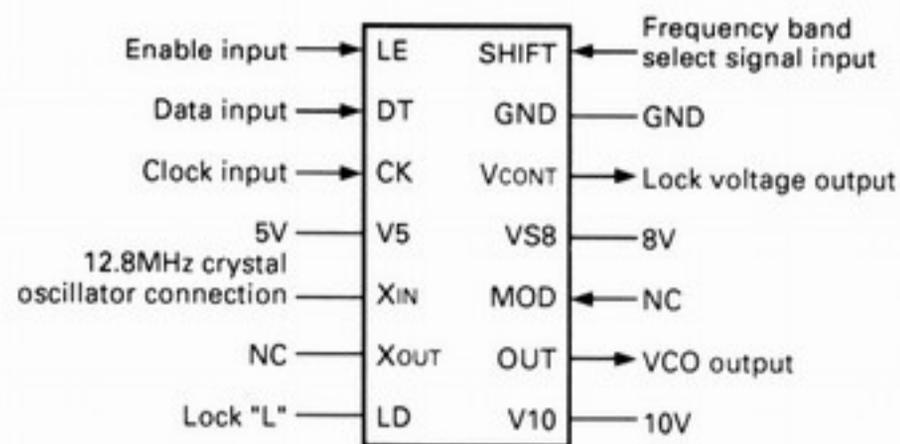


Fig. 9 Sub PLL VCO pin description (IC203 : L78-0351-08)

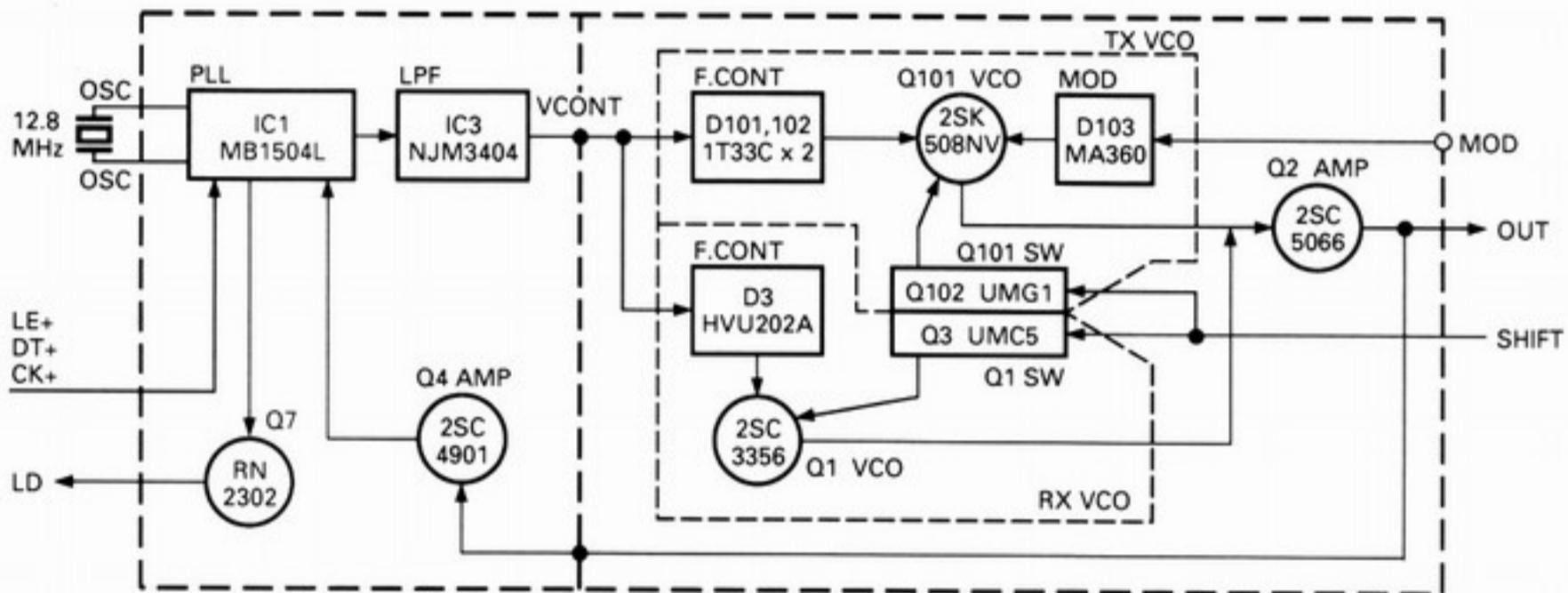


Fig. 10 Main PLL VCO block diagram (IC201 : L78-0363-08)

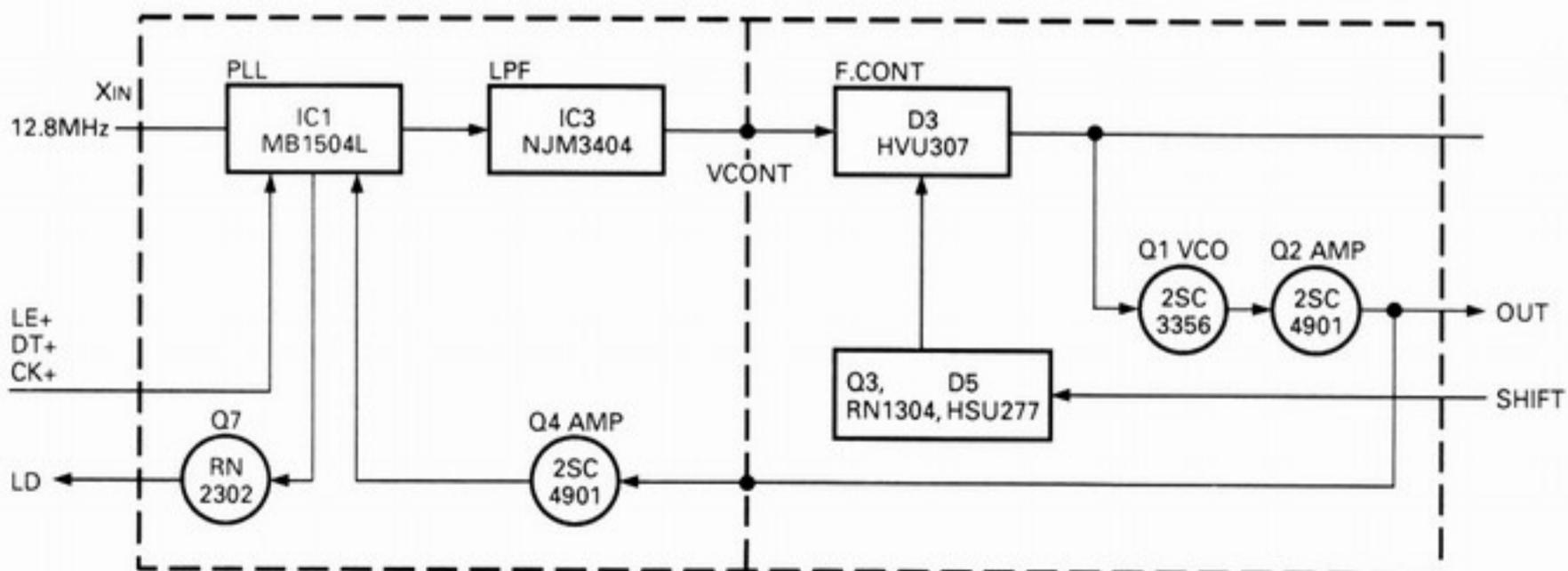


Fig. 11 Sub PLL VCO block diagram (IC203 : L78-0351-08)

CIRCUIT DESCRIPTION

• VT (8 V during transmission) and unlock signal

The base of Q106 (1/2) has 0V applied to it during reception (TX+ : Low level), and Q106 (1/2) and Q105 are turned off. No voltage is applied to the collector (VT) of Q105.

The base of Q106 (1/2) has 2.5 to 5V applied to it during transmission (TX+ : High level), Q106 (1/2) and

Q105 are turned on, and 8V is applied to the collector (VT) of Q105. When the main or sub PLL VCO is unlocked, Q209 is turned on and Q106 (2/2) and Q104 are turned off, the 8V applied to the APC circuit is cut off, and the transmit signal is not output.

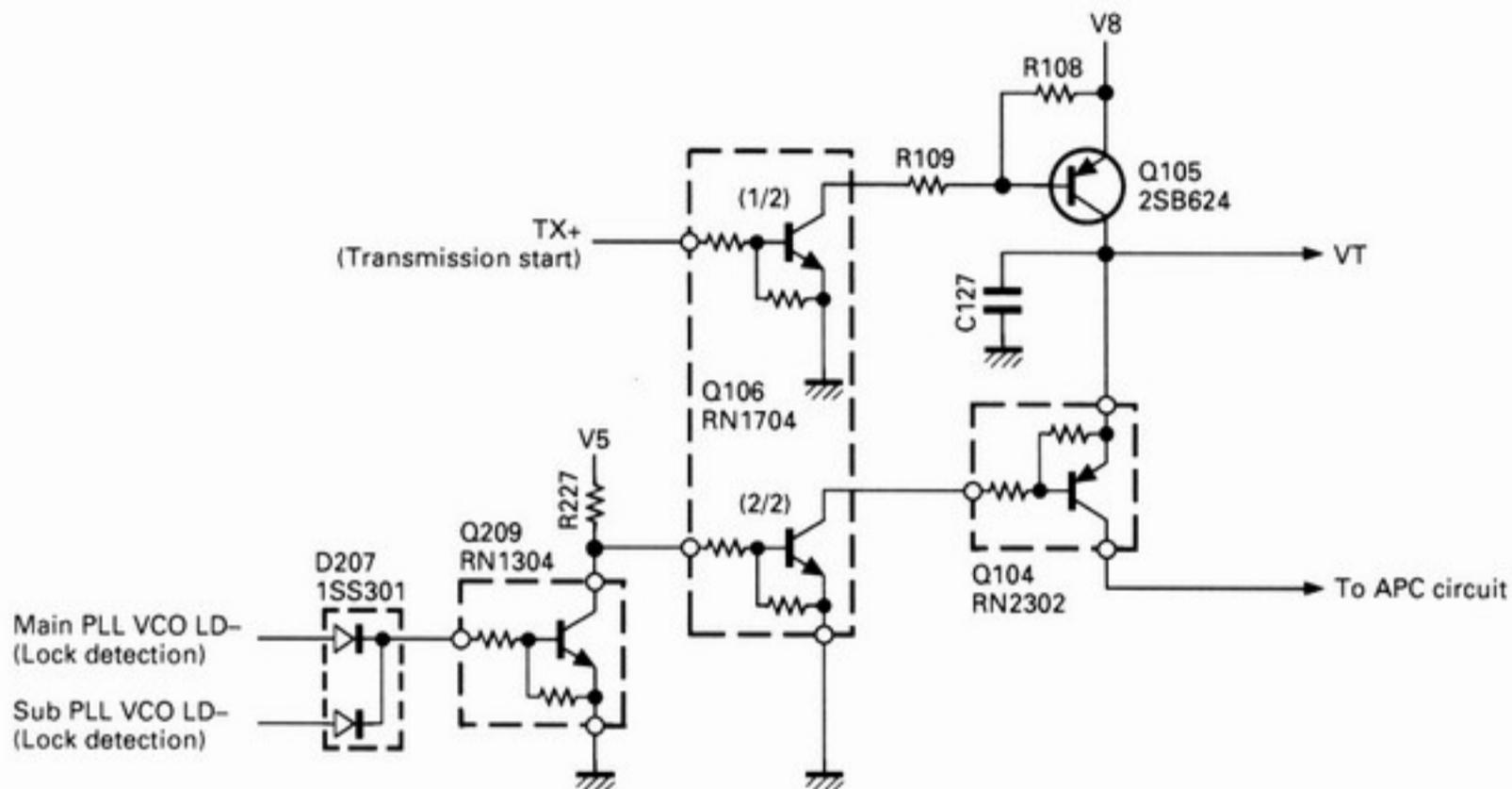


Fig. 12 Transmission start circuit

AF Signal System

• Outline

The audio signal (RXA) from the FM IF HIC (IC1) is input to the RX audio HIC (IC2). The signal passes through the mute circuit in IC2, is summed with the digital recording playback tone, passes through the VR in the control unit, and goes to IC2 again. The signal is then summed with a BUZZER signal (beep and DTMF tones), power-amplified by AF amplifier IC3, and output to the speaker.

When the remote controller is connected, the volume is controlled by the electronic VR in IC2 instead of the VR in the control unit.

• RX audio circuit

Figure 13 shows the circuit of the RX audio (IC2). The path of the audio signal through the VR in the control unit is indicated by the bold line. If the electronic VR is selected (\overline{CS} low), the analog switch IC2 (3/4) is turned off, and the VR in the control unit is isolated. At the same time, IC2 (1/4) is turned off, IC2 (4/4) is turned on, and the volume is controlled by the electronic VR.

The electronic VR consists of 31 resistor elements. The signal can be output from both ends of each element. The element from which the signal is output is specified using CPU P45 (CS-), P43 (U/D-), and P42 (INC-) signals.

CIRCUIT DESCRIPTION

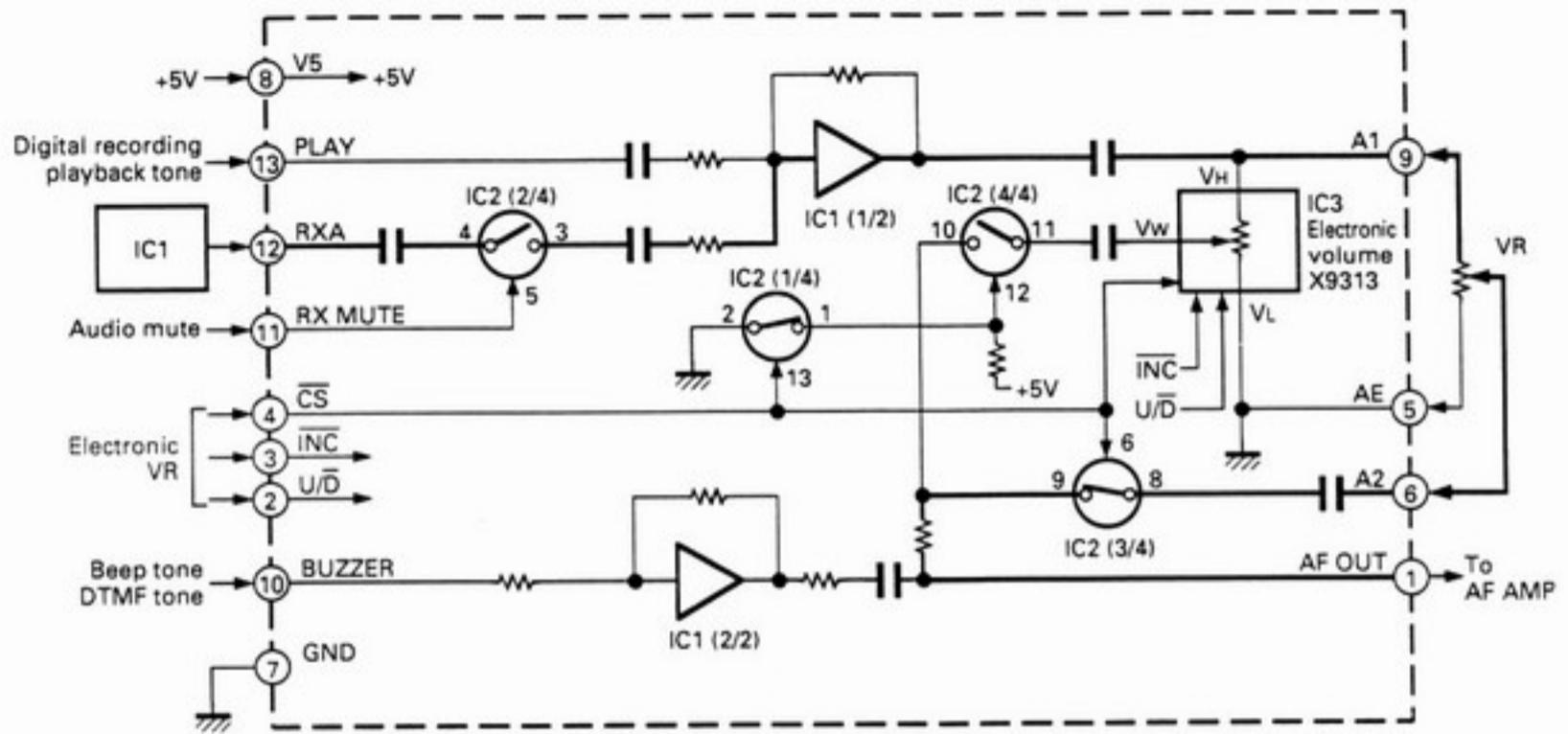


Fig. 13 RX audio circuit (IC2 : W02-1829-08)

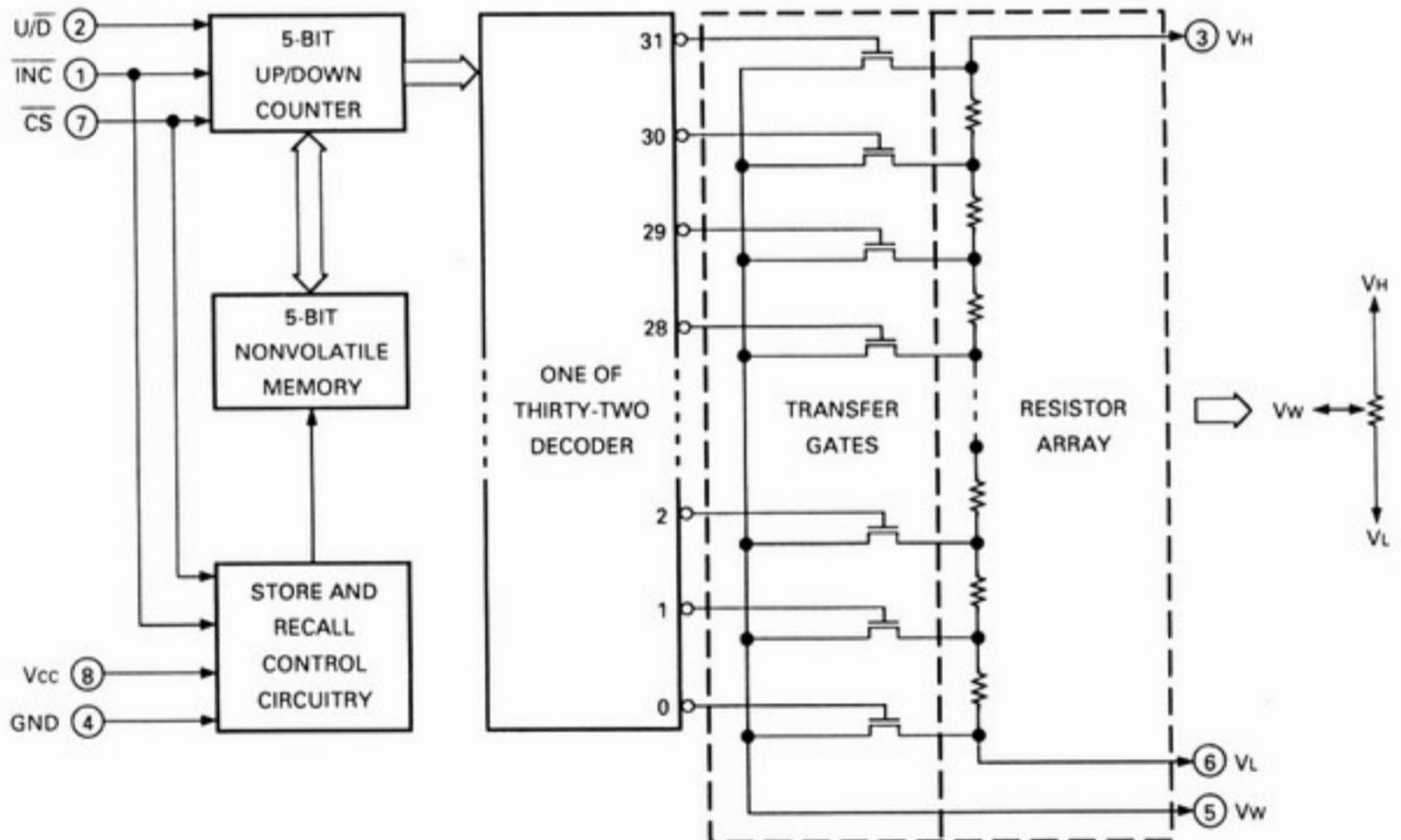


Fig. 14 Electronic VR (X9313) block diagram

CIRCUIT DESCRIPTION

• Squelch circuit

The squelch can be set with the squelch VR in the control unit. The CPU in the control unit converts the squelch VR level to 5-bit digital data and transfers it to the shift register circuit (IC4). (See the description of the shift register circuit.)

The shift register circuit converts the digital data to analog using the shift register and analog switch, gen-

erates the control voltage for IC1 (KCD04) at the SQLC pin, and inputs it to the IC1 SQ pin.

The BUSY signal output from the IC1 SC pin is sent to the CPU as the SC+ signal, and at the same time is output to the hysteresis circuit by Q1, logically reversed by Q6, and output as the SQC signal for packet transmission.

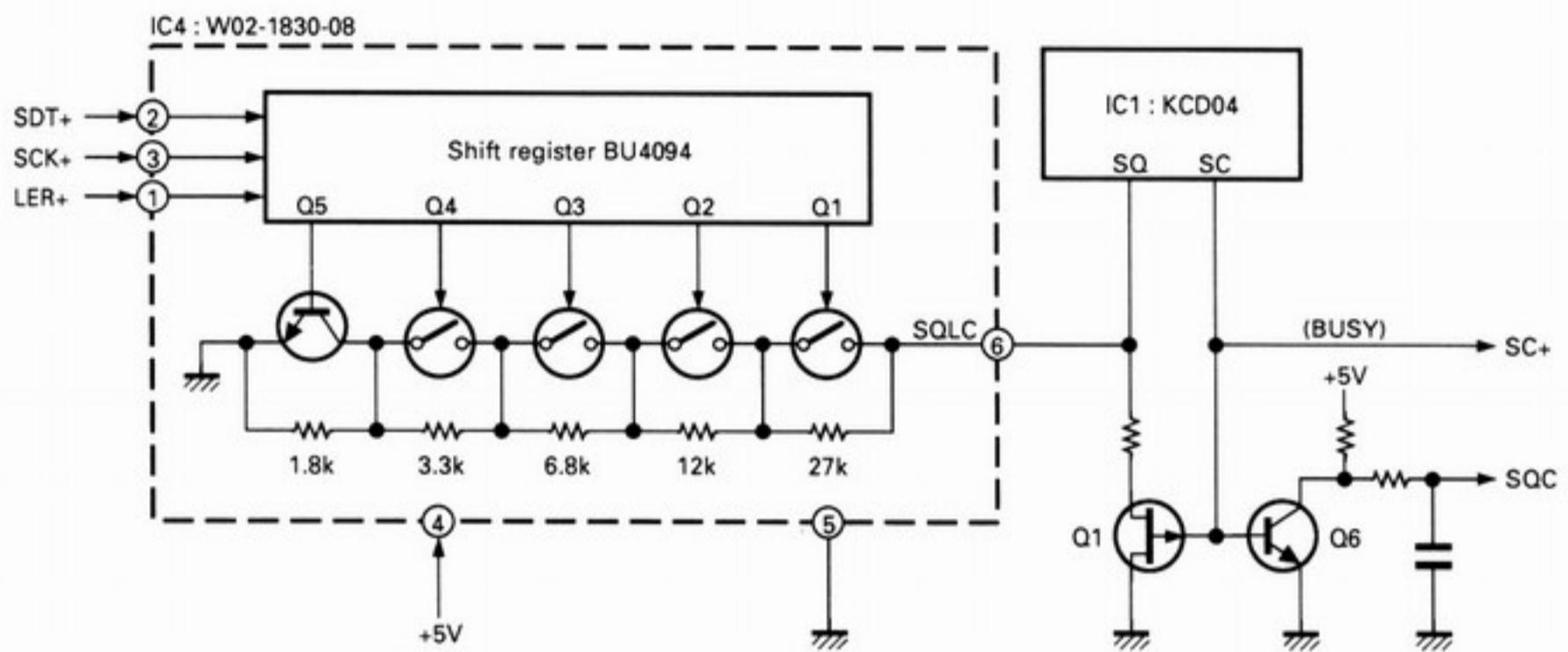


Fig. 15 Squelch circuit

Digital Control Section

• Outline

The digital control section controls each function with the microcomputer (CPU). It consists of the key rotary encoder input circuit, display circuit, reset and backup circuits, DTMF circuit, tone output circuit, digital recording circuit, microphone key input circuit, and SQL input circuit.

• Key and rotary encoder input circuit

The keys on the panel are arranged in a matrix, and signals are input to the CPU by key scanning. The rotary encoder is directly connected to the CPU.

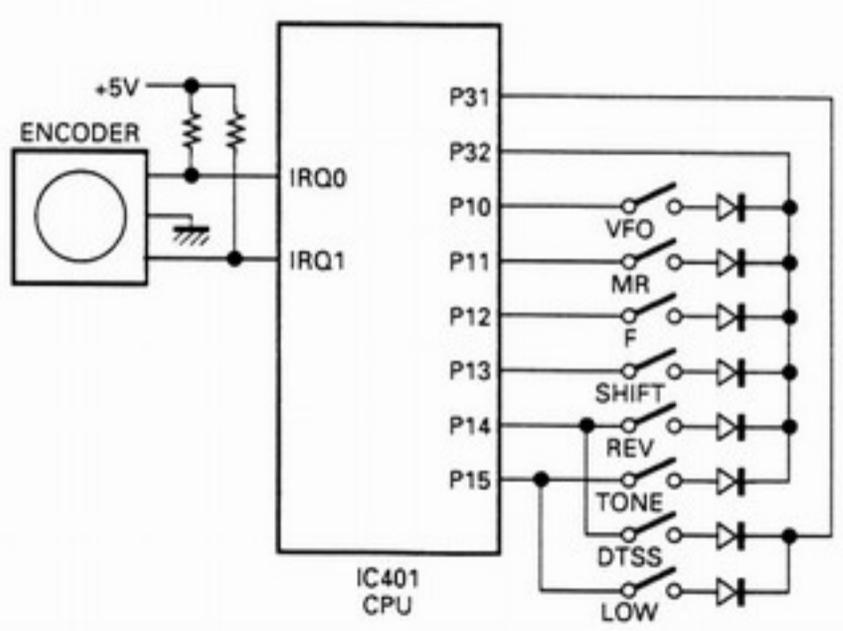


Fig. 16 Key and rotary encoder input circuits

CIRCUIT DESCRIPTION

• Microphone key input circuit

The microphone UP, DOWN, and function keys are connected to the analog input of the CPU. The appropriate function is activated according to the voltage generated when a key is pressed.

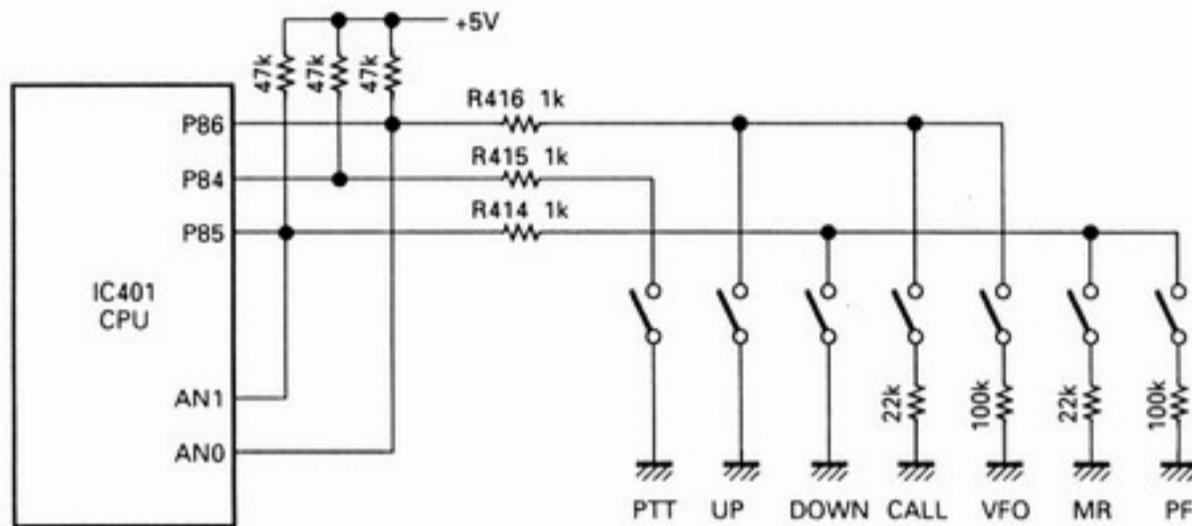


Fig. 17 Microphone key input circuit

• Reset and backup circuits

When the power is turned on, a roughly 20ms low-level pulse is output by the reset circuit according to the time constant, and input to the RESET pin of the CPU. This pulse power-on resets the CPU. When the power is turned off, the +13.8V line voltage drop is detected by the backup circuit, the NMI pin of the CPU

goes high, and the CPU enters backup mode.

The signal is input to the NMI pin and the P97 input port at the same time because P97 is used to check whether the operating voltage for the backup circuit is correct after the power is turned on.

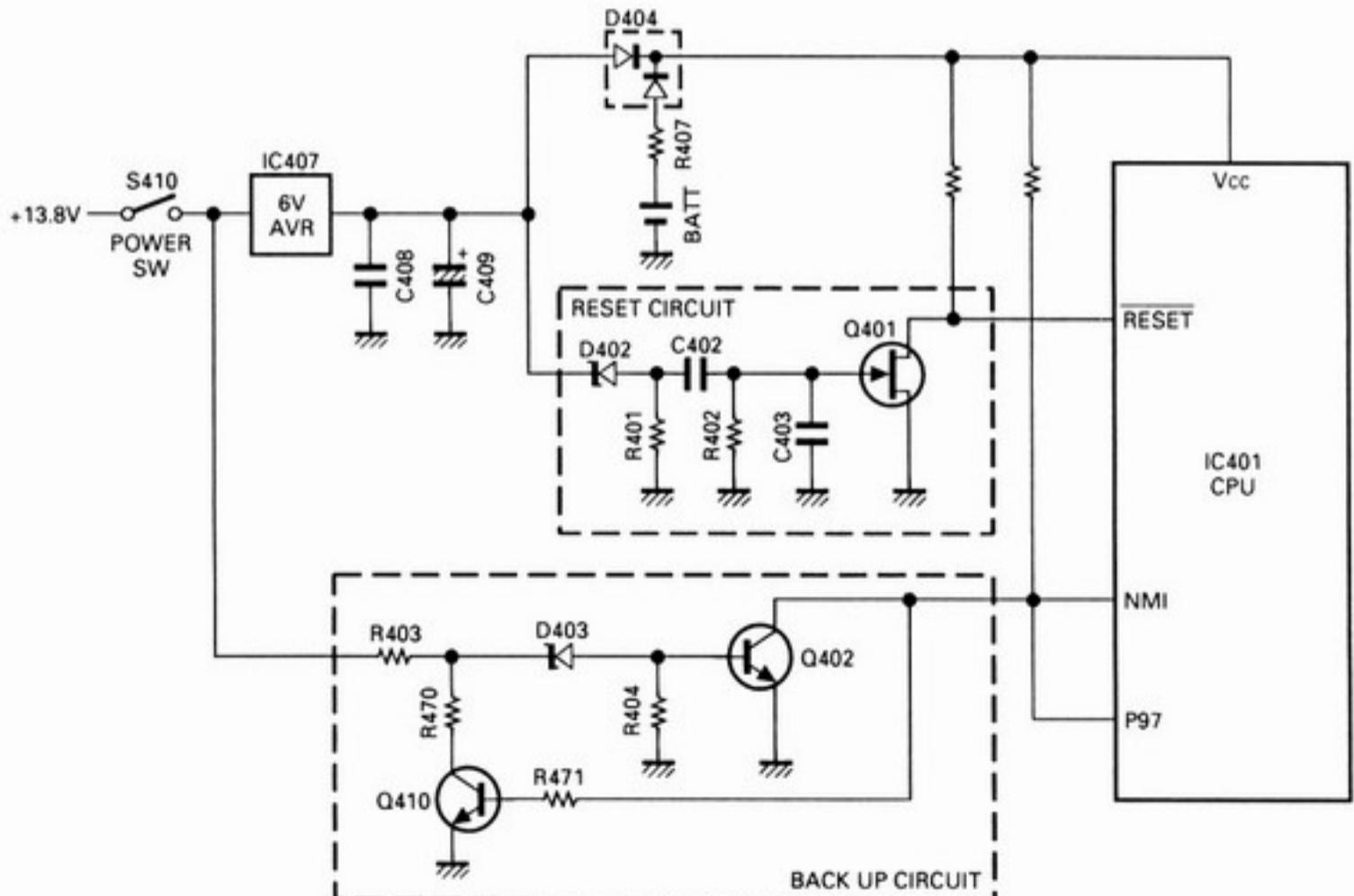


Fig. 18 Reset and backup circuits

CIRCUIT DESCRIPTION

• Display circuit

The display circuit in the LCD assembly consists of an LCD driver, its peripheral circuits, a dimmer circuit, and an LCD. The LCD is dynamically lit with half duty. Serial data is transferred from P50, P51, and P52 of the CPU to the LCD driver.

• Dimmer circuit

The dimmer circuit changes the brightness of the lamp in four steps or turns it off. Q3 amplifies the error of the stabilized power supply using the 5V reference voltage. P35 and P36 of the CPU are made high or low to turn Q5 and Q6 on or off. The output voltage can be controlled in four steps by combining these ports.

If P37 of the CPU is made low, Q4 is turned off, and the lamp voltage is not output, making the lamp go off.

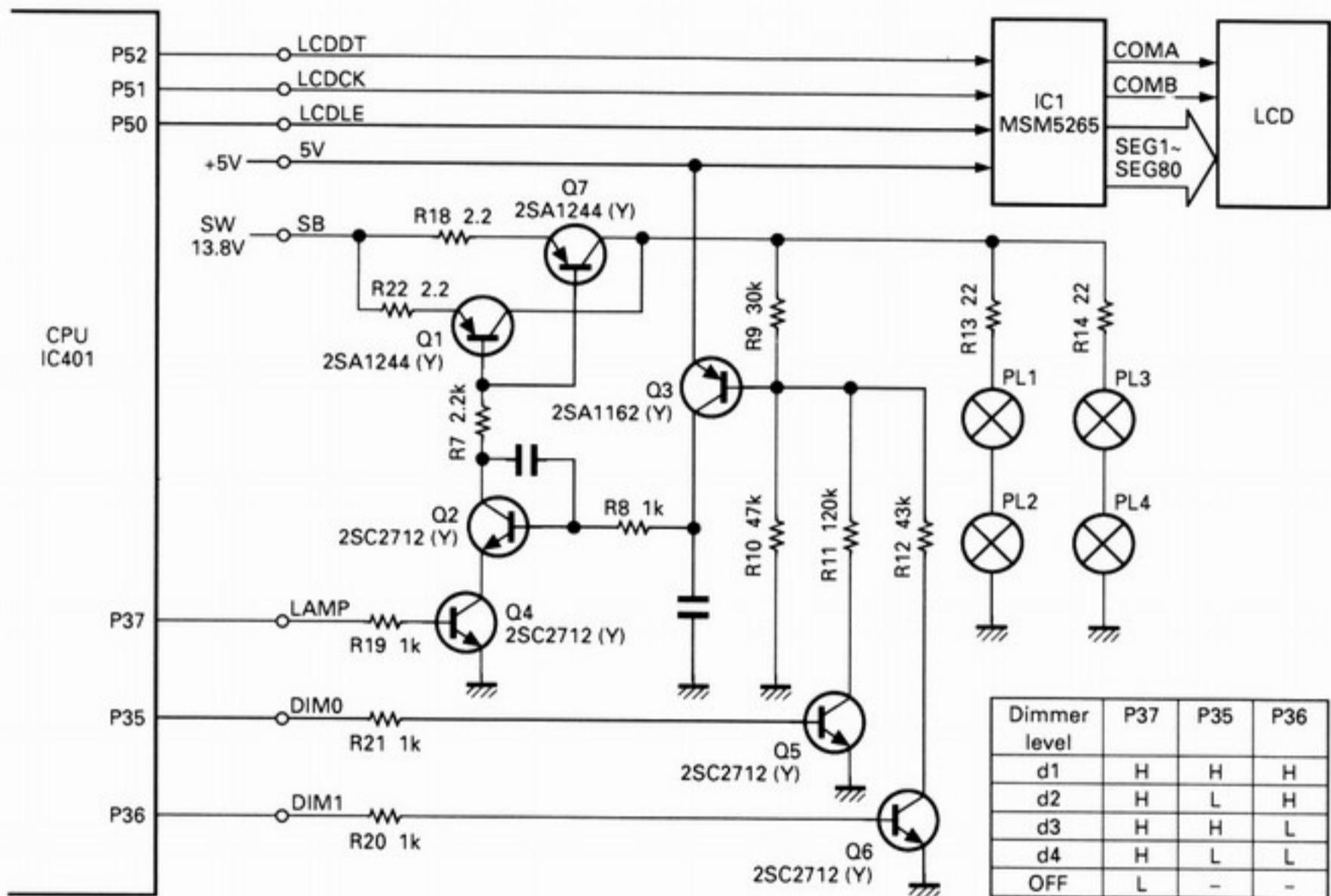


Fig. 19 Display and dimmer circuits

CIRCUIT DESCRIPTION

• PLL data output

PLL data is output from CPU P47 (SDT+), P46 (SCK+), P22 (LEM+), and P23 (LES+). P22 (LEM+) is a main band PLL enable signal, and P23 (LES+) is a sub-band PLL enable signal.

The data transfer format and data configuration are illustrated below.

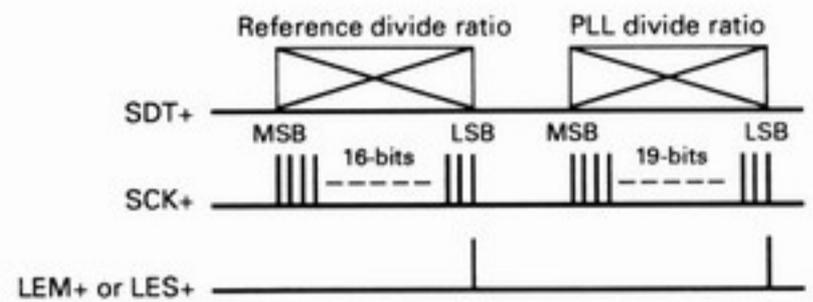


Fig. 20 Data transfer format

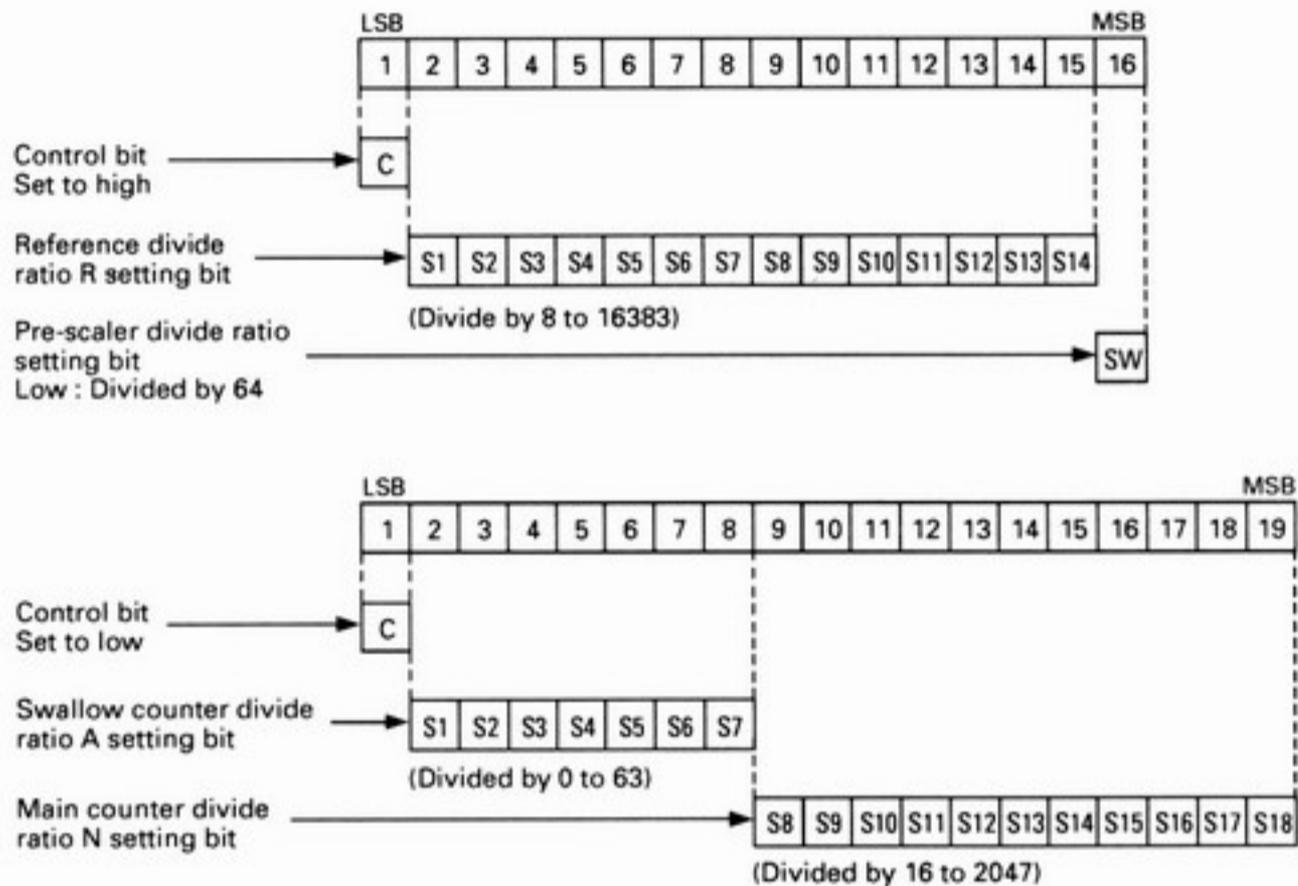


Fig. 21 Data configuration

• Squelch VR input

The CPU digitizes the voltage output by dividing the 5V applied to variable resistor VR401 through the analog port to read the rotation angle of the squelch VR.

• Tone output circuit

The staircase waveform corresponding to the set tone frequency is output from the D/A converter in the CPU, filtered and output via buffer amplifier Q405.

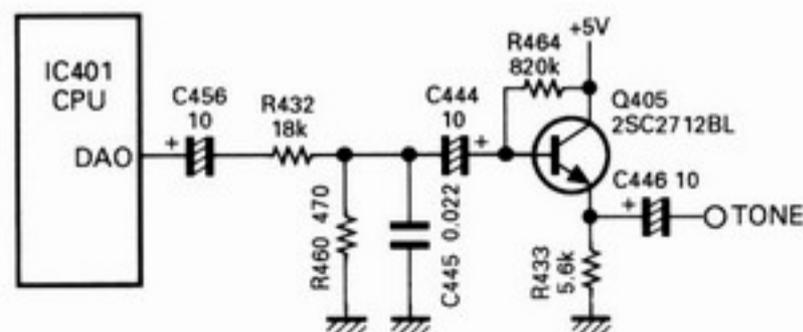


Fig. 22 Tone output circuit

CIRCUIT DESCRIPTION

• DTMF input/output

The DTMF encode IC404 (TC35219F) and DTMF decode IC405 (LC7385M) share CPU P80 to P83 to control input and output operations.

For the encoder, when data arrives at P80 to P83 and P16 (TE+) is high, the tone corresponding to each item of data is output from the IC404 TONE pin. The output DTMF tone passes through buffer amplifier Q406 and analog switch IC409, and is output as the DTMF modulation signal. The DTMF tone is output to the AF signal system as a beeper signal together with the beep tone output from CPU P44.

For the decoder, the detection signal RXD from TX-RX unit IC1 passes through analog switch IC406 and is input to IC405.

When a valid tone is detected, the STD pin goes high and CPU P33 is enabled. When the CPU makes P34 high, data is input to P80 to P83, and the CPU confirms that it matches the preset DTSS code. The input from the DTMF microphone can be read when the CPU switches the analog switch IC406.

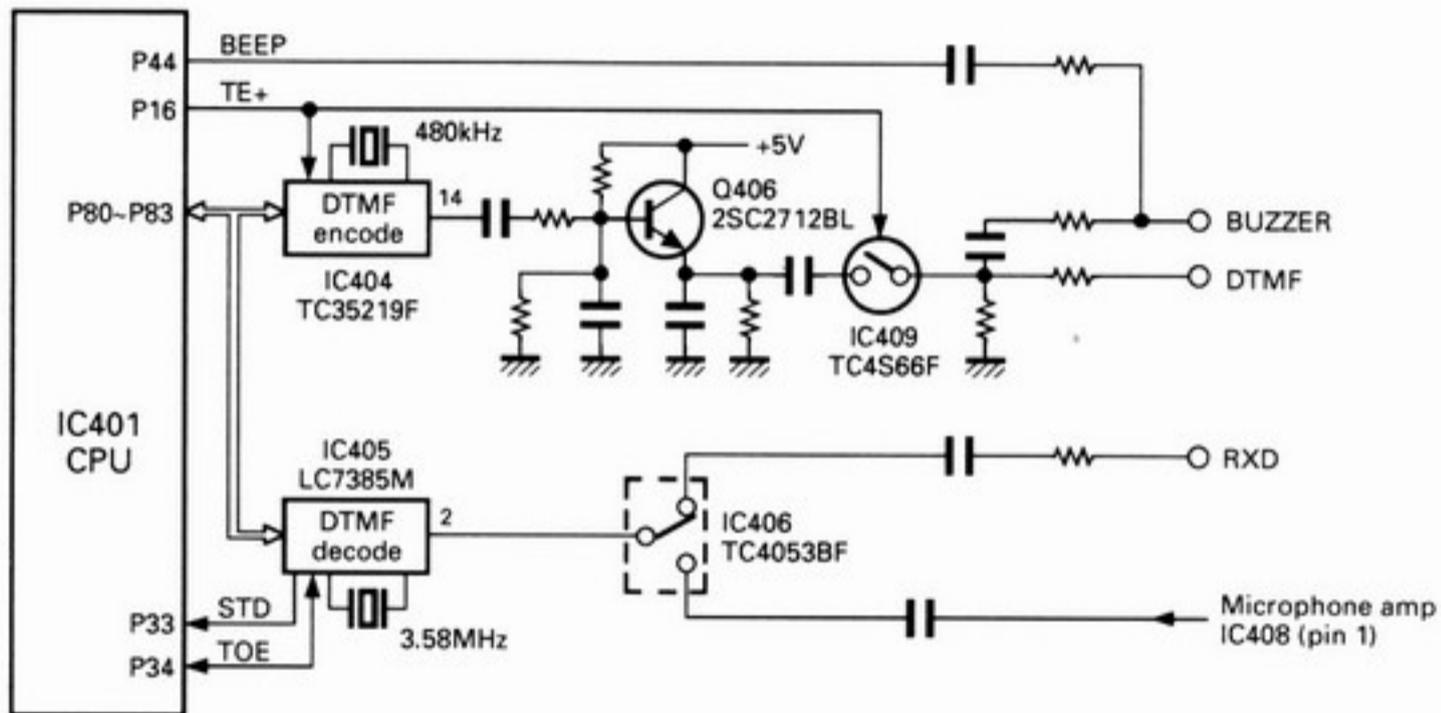


Fig. 23 DTMF input/output

CIRCUIT DESCRIPTION

• Digital recording circuit

The digital recording circuit consists of recording LSI IC402 (MSM6588) based on the ADPCM system and 256-Kbit serial register IC403 (MSM6586). IC402 is controlled by P80 to P83 (shared by DTMF encode/decode control), and P60 to P63.

Recording is performed by applying the receive audio RXA signal to the IC402 MIN pin with CPU control. The playback tone output from the IC402 Fout pin is amplified by IC408 (2/2), passes through analog switches IC410 and IC406, is output as the PLAY signal, and is output from the speaker.

The playback tone can be input to the microphone amplifier IC408 (1/2) and transmitted by controlling the IC406 analog switch with the CPU. (Same band repeater function) In addition, the playback tone is also output to the microphone RD pin.

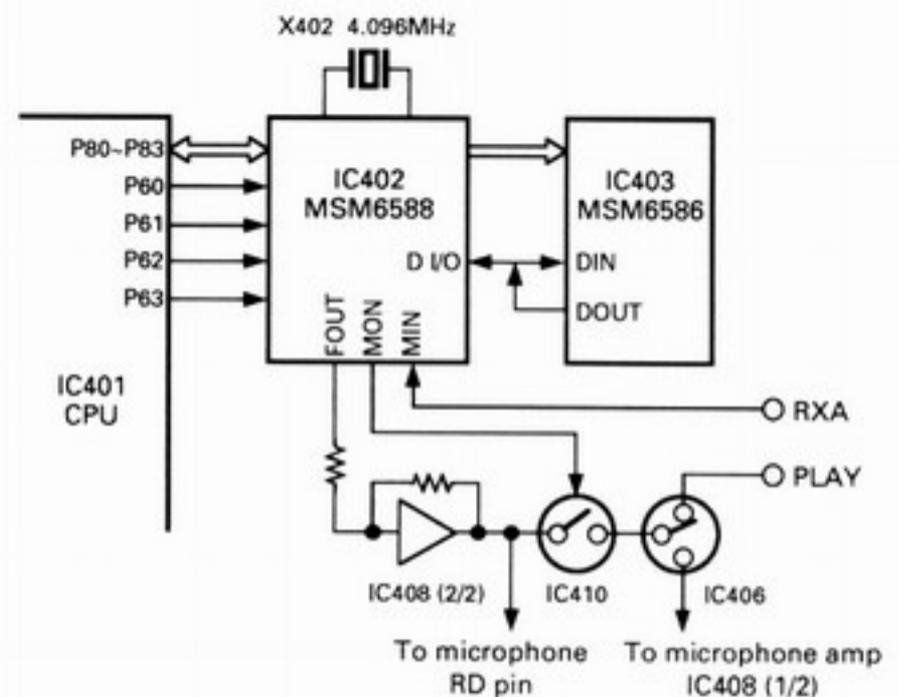


Fig. 24 Digital recording circuit

• CTCSS input/output (option TSU-8)

The CTCSS unit is controlled by using CPU P47 (SDT+), P46 (SCK+), P65 (CTE+), and P96 (SDO-). Figure 25 shows the data transfer format and Figure 26 shows the data configuration. When a tone from the CTCSS unit is detected, the SDO- pin goes low, and the signal is input to CPU P96 to open the squelch.

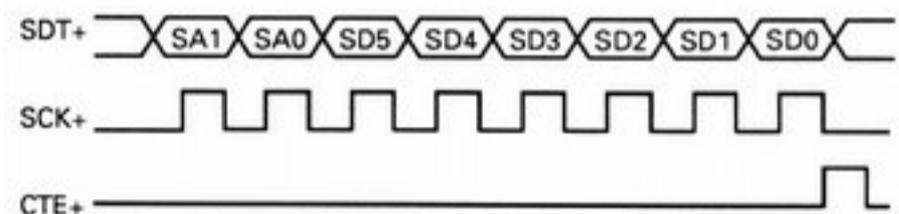


Fig. 25 Data transfer format

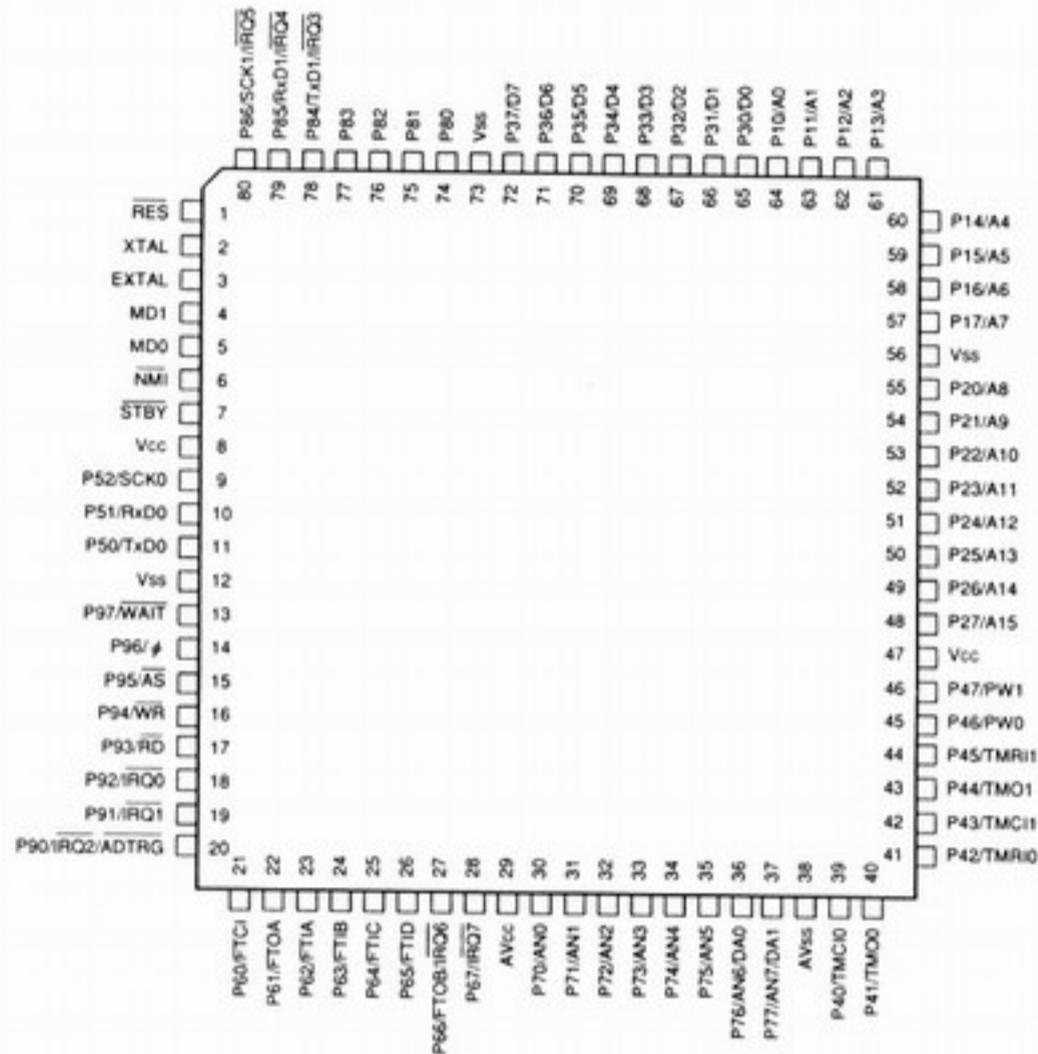
SA1	SA0	SD5	SD4	SD3	SD2	SD1	SD0	Tone frequency
H	H	L	L	L	H	L	H	88.5Hz

Fig. 26 CTCSS data configuration

SEMICONDUCTOR DATA

CPU : HD6473388F-XXX (Control Unit IC401) -K04 · K,P -W04 : M,M2,E,E2,E3,E9

• Terminal connection diagram



• Terminal function (○ : Pullup by soft, ● : Pullup by hard, ■ : Pulldown by hard)

No.	CPU name	Port name	I/O	Pullup	Backup	Function
1	RES		I	●		Reset pin. Normally : High, Reset : Low
2	XTAL		-			Crystal input pin. 4.194304MHz
3	EXTAL		-			Crystal input
4, 5	MD1, MD0		I	●		Operation mode (mode 3) setting. Set to high
6	NMI		I	●		Power supply check. Backup processing on rising edge and power recovery on falling edge.
7	STBY		I	●		Set to high
8	Vcc		-			Power supply voltage
9	P52/SCK0	LCD DT+	O		I	LCD driver data output
10	P51/RXD0	LCD CK+	O		I	LCD driver clock output
11	P50/TXD0	LCD LE+	O		I	LCD driver enable output
12	Vss		-			GND
13	P97/WAIT		I		I	Power supply check. 1 : Backup, 0 : Power supply voltage normal
14	P96/ø	SDO-	I	■	I	CTCSS tone detection. 1 : Mismatch, 0 : Match
15	P95/AS	RM+	O		I	DTMF decoder input signal switching. 1 : Receive RXD, 0 : Microphone input
16	P94/WR	REP+	O		I	Cross-band repeater demodulation signal output switching. 1 : Microphone amplifier
17	P93/RD	RD MUTE+	O		I	Microphone connector RD signal output control. 1 : Mute, 0 : Mute cancel
18	P92/IRQ0	ENC CK-	I	●	I	Encoder clock input
19	P91/IRQ1	ENC DT-	I	●	I	Encoder data input
20	P90/IRQ2/ADTRG	T MUTE+	O		I	Not used.
21	P60/FTCI	DRS WR-	O		I	DRS write output. 0 : Write
22	P61/FTOA	DRS RD-	O		I	DRS read output. 0 : Read
23	P62/FTIA	DRS CE-	O		I	DRS chip enable output. 0 : Chip enable

SEMICONDUCTOR DATA

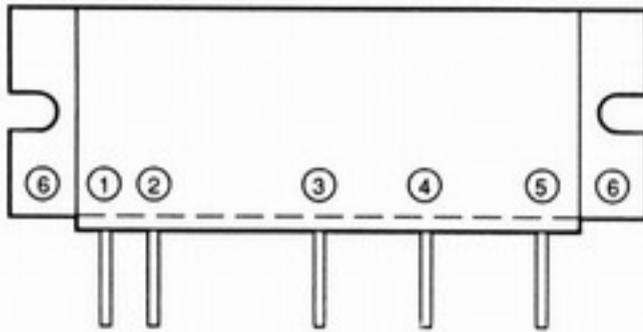
No.	CPU name	Port name	I/O	Pullup	Backup	Function				
24	P63/FTIB	DRS RST-	O	■	I	DRS reset output. 0 : Reset				
25	P64/FTIC	M MUTE-	O		I	Microphone mute output. 1 : Mute cancel, 0 : Mute				
26	P65/FTID	CTE-	O	●	I	CTCSS load enable output				
27	P66/FTOB/IRQ6	PKTS-	I	●	I	Packet PTT input. 1 : Space, 0 : Mark				
28	P67/IRQ7	PSW+	O		I	SW 13.8V power switch. 1 : ON, 0 : OFF				
29	AVcc		-			Analog power supply. Reference power supply for A/D and D/A conversion				
30	P70/AN0	UP	I		I	Microphone switch input (UP, CALL, VFO)				
31	P71/AN1	DWN	I		I	Microphone switch input (DOWN, MR, PF)				
32	P72/AN2	SM	I		I	S-meter level input				
33	P73/AN3	ALD	I		I	Not used				
34	P74/AN4	SQL	I		I	Squelch volume position detection				
35	P75/AN5	RD+	I		I	Controller connection detection. 1 : Connected, 0 : Not connected				
36	P76/AN6/DA0	TONE	O		I	38-wave CTCSS tone output				
37	P77/AN7/DA1	BPFC	O		I	BPF control voltage control output				
38	AVss		-			Analog ground. Ground for A/D and D/A conversion				
39	P40/TMCIO	RX MUTE-	O		I	Demodulation audio mute. 1 : Mute cancel, 0 : Mute				
40	P41/TMO0	1750	O		I	1750Hz tone output (for destination E only)				
41	P42/TMRI0	INC-	O		I	Electronic volume incremental output				
42	P43/TMCI1	U/D-	O		I	Electronic volume UP/DOWN selection. 1 : UP, 0 : DOWN				
43	P44/TMO1	BEEP	O		I	Beep, effect sound output				
44	P45/TMRI1	CS-	O		I	Electronic volume chip select output. 1 : Non-select, 0 : Select				
45	P46/PW0	SCK+	O		I	Common serial clock output				
46	P47/PW1	SDT+	O		I	Common serial data output				
47	Vcc		-			Power supply voltage				
48	P27/A15	TX+	O		I	Transmit/Receive select output. 1 : Transmit, 0 : Receive				
49	P26/A14	LER+	O		I	Shift register load enable				
50	P25/A13	SC+	I	●	I	SC signal input. 1 : No signal, 0 : Signal				
51	P24/A12	MUTE+	O		I	Speaker output mute output. 1 : Speaker mute, 0 : Mute cancel				
52	P23/A11	LES+	O		I	Sub-PLL load enable output				
53	P22/A10	LEM+	O		I	Main PLL load enable output				
54	P21/A9	MDT+	I/O	○	I	EEPROM data input/output (ME-1)				
55	P20/A8	MCK+	O		I	EEPROM clock output (ME-1)				
56	Vss		-			GND				
57	P17/A7	STE-	O		I	DTMF encoder tone selection. 1 : Dual tone, 0 : Single tone				
58	P16/A6	TE+	O	■	I	DTMF encoder tone enable. 1 : ON, 0 : OFF				
59	P15/A5	KIN5-	I	○	I	Key input. TONE, LOW				
60	P14/A4	KIN4-	I	○	I	Key input. REV, DTSS				
61	P13/A3	KIN3-	I	○	I	Key input. SHIFT				
62	P12/A2	KIN2-	I	○	I	Key input. F				
63	P11/A1	KIN1-	I	○	I	Key input. MR				
64	P10/A0	KIN0-	I	○	I	Key input. VFO				
65	P30/D0	KOUT0-	O		I	Key output				
66, 67	P31/D1, P32/D2	KOUT1-, 2-	O		I	Key output				
68	P33/D3	DET+	I		I	DTMF decoder detection input. 1 : Signal detection, 0 : No signal				
69	P34/D4	OE+	O		I	DTMF decoder output enable output. 1 : Enable, 0 : High impedance				
70	P35/D5	DIM0+	O		I	LCD dimmer switching				
71	P36/D6	DIM1+	O		I		D1	D2	D3	D4
DIM0							1	0	1	0
72	P37/D7	LAMP+	O		I	LCD lamp switching. 1 : ON, 0 : OFF				
73	Vss		-			GND				
74-77	P80-P83	D0+~D3+	I/O		I	DRS/DTMF data line D0-D3				
78	P84/TXD1/IRQ3	PTT-	I/O	●	I	PTT input, K bus SO output. 1 : Space, 0 : Mark				
79	P85/RXD1/IRQ4	DWN	I	●	I	K bus SI input				
80	P86/SCK1/IRQ5	UP	I/O	●	I	K bus clock output				

SEMICONDUCTOR DATA

Power Module : M57788M-27-K2 (TX-RX Unit IC101)

• Terminal connection diagram

- 1 : Input
- 2 : Vcc1
- 3 : Vcc2
- 4 : Vcc
- 5 : Output
- 6 : GND (Flange)



• Maximum rating (Tc = 25°C)

Item	Code	Condition	Rating	Unit
Power supply voltage	Vcc		17	V
Current consumption	Icc		12	A
Input power	Pi	Vcc1 ≤ 12.5V, ZG = ZL = 50Ω	800	mW
Output power	Po		50	W
Operating case temperature	Tc(opr)		-30 to +100	°C
Storage temperature	Tstg		-40 to +110	°C

DESCRIPTION OF COMPONENTS

TX-RX UNIT (W02-18XX-08) 1849 : K,P 1850 : M,M2,E,E2,E3,E9

Ref No.	Use and function	Operation/Condition/Compatibility
IC1	2nd local oscillator, IF amplifier, FM detection, Low-frequency amplifier, Noise amplifier, Noise detection, Squelch switching	3, 4 : 2nd local oscillator 45.505MHz 7 : 2nd IF input 455kHz 9 : Scan control BUSY signal (Busy : 0V) 10 : Noise detection voltage output (DC) 11 : S-meter output 12 : FM detection output 14 : RD output 15 : RA output
IC2	AF mute, Adder, Electronic VR	See circuit description.
IC3	AF amplifier	1 : AF input 4 : AF output
IC4	Shift register, Analog switch (squelch)	See circuit description.
IC5	Shift register	See circuit description.
IC101	Final power amplifier	
IC102	Transmit driver amplifier	
IC103	8V AVR	
IC104	5V AVR	
IC201	430MHz-band PLL VCO	See circuit description.
IC202	Pre-emphasis, Limiter amplifier, Splatter filter, Packet modulation data switching, Packet demodulation buffer amplifier	See circuit description.
IC203	144MHz-band PLL VCO	See circuit description.
IC204	10V AVR	
IC205	Analog switch (modulation input on/off)	
IC208	144MHz-band PLL VCO output amplifier	
IC302	360MHz, 800MHz-band RF amplifier	K, P type : 360MHz-band only.
IC303	RF band-pass filter control, DC amplifier, RD buffer amplifier	
Q1	Squelch hysteresis	Squelch on : ON
Q2	Speaker output mute switch	
Q3	Inverter	SC logic inversion.
Q4	Second mixer	
Q101	DC amplifier	
Q102	DC amplifier	
Q103	Differential amplifier (APC circuit)	
Q109	Mid/low power change switch	
Q104-106	Switching	See circuit description.
Q107, 108	Switching	13.8V on/off
Q110	430MHz-band RF amplifier	
Q201	430MHz-band PLL VCO output amplifier	
Q202	PLL VCO 8V ripple filter	
Q203, 205	144MHz-band PLL VCO power switch	Q205 : 5V, Q203 : 8V
Q204	Q203 and Q205 control	
Q206	Multiplier (Double)	K, P type are not used.
Q208	12.8MHz buffer	

DESCRIPTION OF COMPONENTS

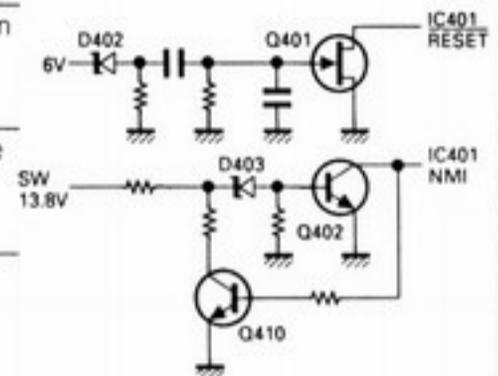
Ref No.	Use and function	Operation/Condition/Compatibility
Q209	Inverter (PLL lock signal)	OFF : Lock
Q210	Packet modulation, Excessive input detection	
Q211	Inverter (Packet PTT)	
Q212	10V ripple filter	
Q301, 302	High-frequency amplifier (430MHz-band reception)	
Q303, 304	High-frequency amplifier (144MHz-band reception)	
Q305	360MHz, 800MHz-band receive circuit power switch	1/2 : 360MHz-band, 2/2 : 800MHz-band (Except K, P type)
Q306	Q305 control	
Q307	430MHz, 144MHz-band receive circuit power switch	1/2 : 430MHz-band, 2/2 : 144MHz-band
Q308	Q307 (1/2) control	
Q309	Q307 (2/2) control	
Q310	First mixer	
Q311	First IF amplifier	
Q312	High-frequency amplifier (800MHz-band reception)	Except K, P type
Q313	High-frequency amplifier (360MHz, 800MHz-band reception)	K, P type : 360MHz-band reception only
D1	Limiter (First IF)	
D101, 102	Power detection	
D103, 104	Antenna switch	
D105	Power reverse-connection prevention	
D106, 107	Antenna switch	
D108	VCO output switch	
D201	VCO output switch (transmission/reception switching)	
D203	First local change-over switch (800MHz-band ON/OFF)	Except K, P type
D204	First local change-over switch (430MHz/800MHz)	K, P type : 430MHz-band only
D205, 209	First local change-over switch (430MHz, 360MHz/144MHz)	
D206	Circuit protection	
D207	Unlock signal OR (logic sum)	
D208	Packet modulation input signal detection	
D301	OR (logic sum)	
D302	RF switch	430MHz/360MHz
D303-306	Vari-cap tuning	430MHz-band band-pass filter
D309	RF switch	360MHz/800MHz (K, P type : 360MHz-band only)
D311, 312	RF amplifier protection	
D313-316	Vari-cap tuning	
D317, 318	RF switch	
D319-321	OR (logic sum)	
D322	RF switch	800MHz-band (Except K, P type)

CONTROL UNIT (W02-18XX-08) 1852 : K,P 1853 : M 1854 : M2 1855 : E,E3,E9 1856 : E2

Ref No.	Use and function	Operation/Condition/Compatibility
IC401	Microprocessor	See circuit description.
IC402	Digital recording control	See circuit description.
IC403	256-kbit serial register	See circuit description.
IC404	DTMF encoder	See circuit description.
IC405	DTMF decoder	See circuit description.
IC406	Analog switch (multiplexer)	1 : Audio playback modulation output 2 : Audio playback speaker output 3 : Receive audio output (repeater) 4 : Receive audio input 12 : DTMF microphone input 13 : DTMF receive input 14 : Output to DTMF decoder 15 : Audio playback tone input

DESCRIPTION OF COMPONENTS

Ref No.	Use and function	Operation/Condition/Compatibility
IC407	6V AVR	
IC408	Low-frequency amplifier, Adder	1 : Output 4 : GND 8 : 5V 2 : Microphone input, 1200-bps AFSK data input, 1750Hz tone input, Receive audio input (repeater) 6 : Audio playback tone input 7 : Audio playback tone output
IC409	Analog switch	DTMF signal on/off
IC410	Analog switch	Audio playback tone on/off
Q401	Reset switch	ON for about 20ms when the power is turned on. Normally OFF.
Q402	Backup switch	OFF when the 13.8V line is below 8.3 V. Normally ON.
Q410	Hysteresis switch	ON when Q402 is OFF. Normally OFF.
Q403	Microphone muting	ON : During reception, OFF : Microphone remote, ON : Repeater
Q404	RD muting	ON : Digital recording playback Interlocked with SQL when the RD mute function is on.
Q405	Buffer amplifier	For tone
Q406	Buffer amplifier	For DTMF
Q409	Switch	DTMF decoder IC405 power save
D401	Reverse-flow prevention	
D402	Reset detection voltage	
D403	Backup detection voltage	
D404	Reverse-flow prevention	Lithium battery ON when the power is off.
D405	Microprocessor protection	
D407-410	Reverse-flow prevention	
D411, 412	Channel display mode setting	D411 is not installed.
D413-418	Destination setting	
D419, 420	Reverse-flow prevention	



SUB PLL VCO (IC203 : L78-0351-08)

Ref No.	Use and function	Operation/Condition/Compatibility
IC1	PLL controller	7 : Unlock : Pulse output 8 : VCO input
IC3	LPF	
Q1	VCO	
Q2	VCO output buffer	
Q3	VCO frequency band switching	
Q4	VCO output buffer	
Q7	Lock detector	
D3	VCO voltage control	
D5	High-frequency switch	

DESCRIPTION OF COMPONENTS

MAIN PLL VCO (IC201 : L78-0363-08)

Ref No.	Use and function	Operation/Condition/Compatibility
IC1	PLL controller	7 : Unlock : Pulse output 8 : VCO input
IC2	Analog switch	Normally OFF.
IC3	LPF	
Q1	VCO	Receiver VCO.
Q2	VCO output buffer	
Q3	VCO frequency band switching	
Q4	VCO output buffer	
Q7	Lock detector	
Q101	VCO	Transmitter VCO.
Q102	Switching	
D3	VCO voltage control	
D101, 102	VCO voltage control	
D103	Transmit modulation	

TX AUDIO (IC202 : W02-1828-08)

Ref No.	Use and function	Operation/Condition/Compatibility
IC1	Analog switch	See circuit description.
IC2 (1/2)	Limit amplifier	Preemphasis, limiter
IC2 (2/2)	LPF	Splatter filter
IC3 (1/2)	Receive data output buffer	
IC3 (2/2)	Adder	

RX AUDIO (IC2 : W02-1829-08)

Ref No.	Use and function	Operation/Condition/Compatibility
IC1 (1/2)	Adder amplifier	
IC1 (2/2)	Output buffer	
IC2	Analog switch	See circuit description.
IC3	Audio electronic VR	1 : INC input (Operate on rising edge.) 2 : Up/down control input 3 : Audio input 4 : GND 5 : Audio output 6 : GND 7 : Chip select input 8 : +5V

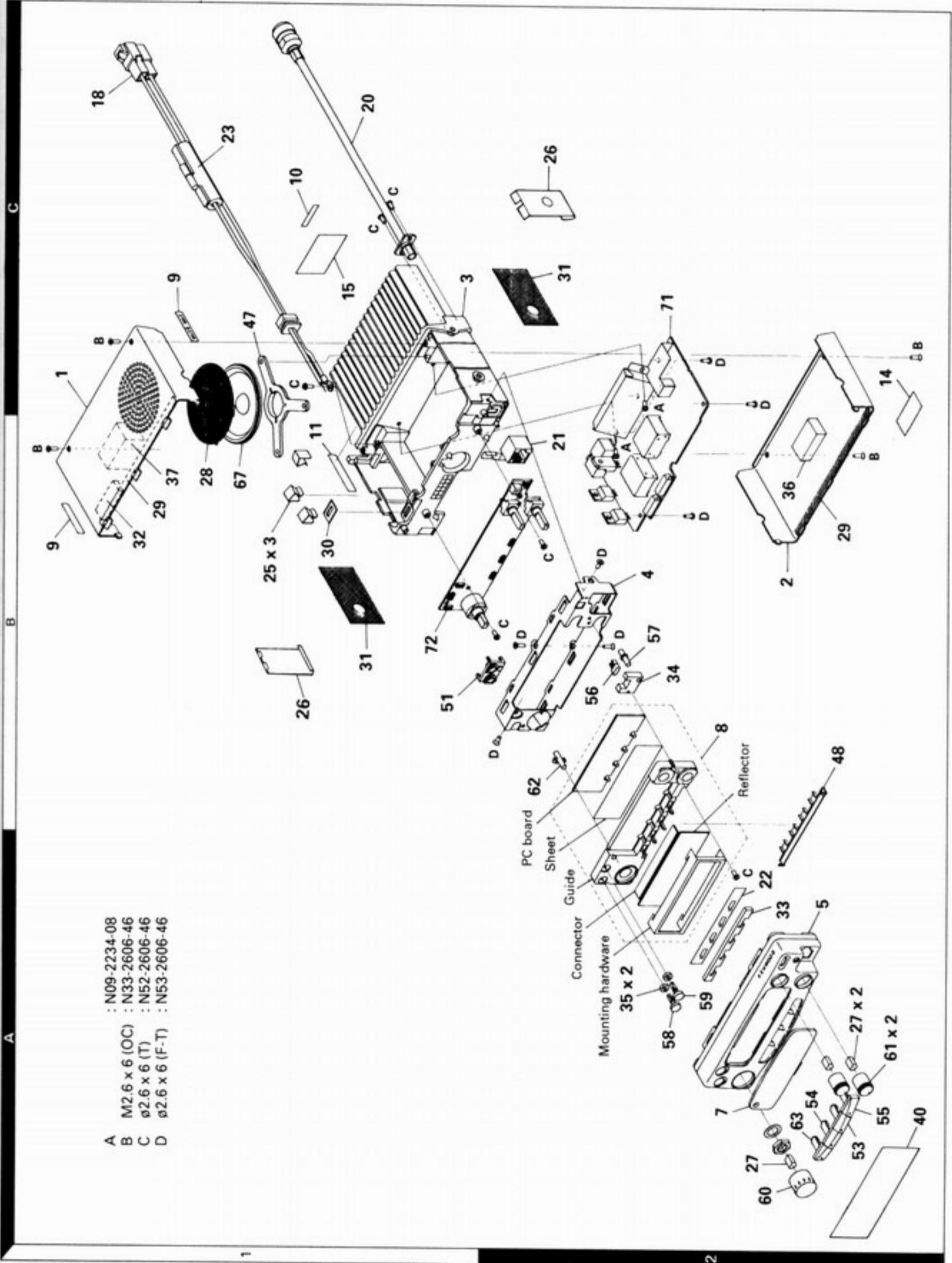
PROG SQL (IC4 : W02-1830-08)

Ref No.	Use and function	Operation/Condition/Compatibility
IC1	Shift register	1 : Enable input 2 : Serial data input 3 : Clock input 4 : SQL0 output 5 : SQL1 output 6 : SQL2 output 7 : SQL3 output 8 : GND 11 : Sub-band reception ON 12 : 360MHz-band reception ON 14 : SQL4 output 15 : Output enable input (normally high) 16 : +5V
IC2	Analog switch	See circuit description.
Q1	Inverter	

RF AMP (IC102 : W02-1831-08)

Ref No.	Use and function	Operation/Condition/Compatibility
Q1, 2	High-frequency amplifier	

EXPLODED VIEW



- A : N09-2234-08
- B : M2.6 x 6 (OC) : N33-2606-46
- C : ø2.6 x 6 (T) : N52-2606-46
- D : ø2.6 x 6 (F-T) : N53-2606-46

ADJUSTMENT

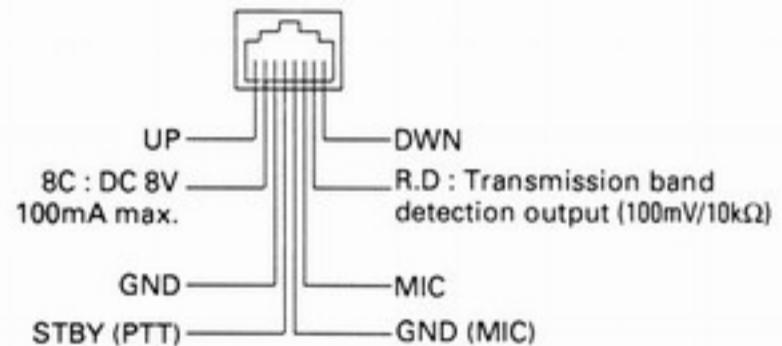
Measuring Equipment for Adjustment

1. Tester
Input impedance: High
2. RF valve voltmeter (RF V.M)
Input impedance: $1M\Omega$ or more, 2 pF or less
Voltage range: Full scale = 10mV to 300V
Measurable frequency range: up to 500MHz
3. Frequency counter (f. counter)
Input sensitivity: About 50mV
Measurable frequency: 500MHz or more
4. DC power supply
Voltage: Variable in the range 10 to 17V
Current: 13A or more
5. Power meter
Measurement power: 50W, 25W, 3W
Impedance: 50Ω
Measurable frequency: 500MHz
6. AF valve voltmeter (AF V.M)
Input impedance: $1M\Omega$ or more
Voltage range: Full scale = 1mV to 30V
Measurable frequency range: 50Hz to 10kHz
7. AF generator (AG)
Output frequency: 100Hz to 10kHz
Output voltage: 0.5mV to 1V
8. Line detector
Measurable frequency: 500MHz
9. Spectrum analyzer
Measurable frequency: 500MHz
10. Directional coupler
11. Oscilloscope
High sensitivity with horizontal input terminal
12. Standard signal generator (SSG)
The standard signal generator must be able to generate the 144 and 430MHz band frequencies and vary the amplitude and frequency.
Output: $0.1\mu V$ to greater than 1mV
13. Dummy load
 8Ω , about 5W
14. Noise generator
The noise generator must be able to generate noise similar to ignition noise containing high-frequency components of 500MHz or more.
15. Sweep generator
The sweep generator must be able to sweep the 144 and 430MHz bands.
16. Tracking generator
17. Adjustment jig
Extension flat cable.

Preparation

- Set the controls and switches to the positions listed below unless otherwise specified.

VOL control	Fully counterclockwise
SQL control	Fully counterclockwise
POWER switch	OFF
(For fixed stations) DC power supply POWER switch	OFF



Microphone socket
 (as viewed from the front of the set)

- Use an insulated rod, such as a plastic rod, for adjustment (especially for trimmers, coils, etc.).
- To protect the signal generator, never connect the microphone to the microphone socket when the receiver section is adjusted.
- Before the power cord is connected, make sure the power switch is off.
- See the instruction manual for transmit and receive operations.

ADJUSTMENT

Common Section Adjustment

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
1. Setting	1) Power supply voltage : 13.8V DC POWER SW : OFF VOL VR, SQL VR : Fully counterclockwise							
2. Reset	1) Hold down the MR key, and turn the power switch on. Confirm that all LCD segments turn on, then release the MR key.						Check	All LCD segments on
3. PLL lock voltage	1) 430MHz band FREQ. : 435.000MHz M,M2,E,E2,E3,E9 FREQ. : 445.000MHz K,P Receive and transmit	DVM	TX-RX	TP201			Check	M,M2,E,E2,E3,E9 RX : 4.7V±1V TX : 3.7V±1V K,P RX : 5.4V±1V TX : 4.3V±1V
	2) 144MHz band FREQ. : 144.980MHz Receive			TP202				
4. Transmit frequency	1) FREQ. : 435.000MHz M,M2,E,E2,E3,E9 FREQ. : 445.000MHz K,P Transmit	f. counter Dummy load	Rear panel	ANT	TX-RX	TC201	435.00070MHz M,M2,E,E2,E3,E9 445.00070MHz K,P	±100Hz

Receiver Section Adjustment

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
1. BPF (430MHz band)	1) FREQ. : 435.040MHz M,M2,E,E2,E3,E9 FREQ. : 445.040MHz K,P AF VOL : 9 o'clock position Connect the distortion meter to the EXT. SP socket. (Dummy load : 8Ω) Connect the SSG to the ANT.	SSG Distortion meter Oscilloscope AF VTVM	Rear panel	EXT. SP	TX-RX			
	2) SSG output : 0.28μV/-118dBm MOD : 1kHz DEV : ±3kHz					TC303 TC304	Adjust TC304, TC303, and TC304 in the order listed so that SINAD is the best.	
	3) SSG output : 0.18μV/-122dBm MOD : 1kHz DEV : ±3kHz					TC301 TC302	Adjust TC302, TC301, and TC302 in the order listed so that SINAD is the best.	SINAD 12dB or more.
2. Crystal filter coil	1) SSG output : 500μV/-53dBm MOD : 1kHz DEV : ±3kHz					L317	Best distortion rate.	SINAD 35dB or more.
3. BPF (144MHz band)	1) FREQ. : 145.980MHz AF VOL : 9 o'clock position Connect the distortion meter to the EXT. SP socket. (Dummy load : 8Ω) Connect the SSG to the ANT.							
	2) SSG output : 0.28μV/-118dBm MOD : 1kHz DEV : ±3kHz					TC307 TC308	Adjust TC308, TC307, and TC308 in the order listed so that SINAD is the best.	
	3) SSG output : 0.18μV/-122dBm MOD : 1kHz DEV : ±3kHz					TC305 TC306	Adjust TC306, TC305, and TC306 in the order listed so that SINAD is the best.	SINAD 12dB or more.

ADJUSTMENT

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
4. Sensitivity	1) 430MHz band M,M2,E,E2,E3,E9 FREQ. : 430.040MHz FREQ. : 435.040MHz FREQ. : 439.980MHz K,P FREQ. : 438.040MHz FREQ. : 445.040MHz FREQ. : 449.980MHz SSG output : 0.18 μ V/-122dBm	SSG Distortion meter Oscilloscope AF VTVM	Rear panel	EXT. SP			Check	SINAD 12dB or more.
	2) 144MHz band E,E2,E3,E9 FREQ. : 144.040MHz FREQ. : 145.040MHz FREQ. : 145.980MHz K,P,M,M2 FREQ. : 144.040MHz FREQ. : 145.980MHz FREQ. : 147.980MHz SSG output : 0.18 μ V/-122dBm							Check
5. Major input S/N ratio	1) 430MHz band FREQ. : 435.040MHz M,M2,E,E2,E3,E9 FREQ. : 445.040MHz K,P SSG output : 500 μ V/-53dBm AF output : 2.83V/8 Ω	SSG Oscilloscope AF VTVM	Rear panel	EXT. SP			Check	S/N 46dB or more.
	2) 144MHz band FREQ. : 145.040MHz E,E2,E3,E9 FREQ. : 145.980MHz K,P,M,M2 SSG output : 500 μ V/-53dBm AF output : 2.83V/8 Ω							
6. Distortion ratio	1) 430MHz band FREQ. : 435.040MHz M,M2,E,E2,E3,E9 FREQ. : 445.040MHz K,P SSG output : 50 μ V/-73dBm AF output : 4V/8 Ω	SSG Distortion meter Oscilloscope AF VTVM	Rear panel	EXT. SP			Check	5% or less.
	2) 144MHz band FREQ. : 145.040MHz E,E2,E3,E9 FREQ. : 145.980MHz K,P,M,M2 SSG output : 50 μ V/-73dBm AF output : 4V/8 Ω							
7. S-meter	1) 430MHz band FREQ. : 435.040MHz M,M2,E,E2,E3,E9 FREQ. : 445.040MHz K,P SSG output : 3.5 μ V/-96dBm	SSG	Rear panel	ANT	TX-RX	VR1	Turn clockwise gradually until all the S-meter segments turn on.	All S-meter segments on.
	2) SSG output : OFF							
	3) 144MHz band FREQ. : 145.040MHz E,E2,E3,E9 FREQ. : 145.980MHz K,P,M,M2 SSG output : 8.0 μ V/-89dBm						All S-meter segments on.	
	4) SSG output : OFF						All S-meter segments off.	

ADJUSTMENT

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
8. Squelch	1) 430MHz band FREQ. : 435.040MHz M,M2,E,E2,E3,E9 FREQ. : 445.040MHz K,P SSG output : OFF Turn the SQL VR until noise disappears.	SSG Oscilloscope	Rear panel	EXT. SP			Check	Control position : 8~11 o'clock BUSY off.
	2) SSG output : 0.1μV/-127dBm							Squelch is open. BUSY on.
	3) SQL VR : Fully clockwise							AF output off. BUSY off.
	4) SSG output : 0.35μV/-116dBm							Squelch is open.
	5) 144MHz band FREQ. : 145.040MHz E,E2,E3,E9 FREQ. : 145.980MHz K,P,M,M2 SSG output : OFF Turn the SQL VR until noise disappears.							Control position : 8~11 o'clock BUSY off.
	6) SSG output : 0.1μV/-127dBm							Squelch is open. BUSY on.
	7) SQL VR : Fully clockwise							AF output off. BUSY off.
	8) SSG output : 0.35μV/-116dBm							Squelch is open.

Transmitter Section Adjustment

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
1. Power	1) FREQ. : 435.000MHz M,M2,E,E2,E3,E9 FREQ. : 445.000MHz K,P	Power meter Ammeter	Rear panel	ANT	TX-RX	VR101	Fully clockwise	37W or more.
	2) Power : High Transmit						36W	35~42W 10A or less.
	3) Power : Low Transmit						5W	±1W
	4) Power : Mid					Check	10~14W	
	5) M,M2,E,E2,E3,E9 FREQ. : 430.000MHz FREQ. : 435.000MHz FREQ. : 439.940MHz K,P FREQ. : 438.000MHz FREQ. : 445.000MHz FREQ. : 449.940MHz Power : High Transmit						35~42W 10A or less.	
	6) Power : Mid Transmit						10~14W	
	7) Power : Low Transmit						3~8W	
	8) FREQ. : 400.000MHz M2 FREQ. : 410.000MHz E2 FREQ. : 469.940MHz M2,E2 Power : High Transmit						3.5W or more.	

ADJUSTMENT

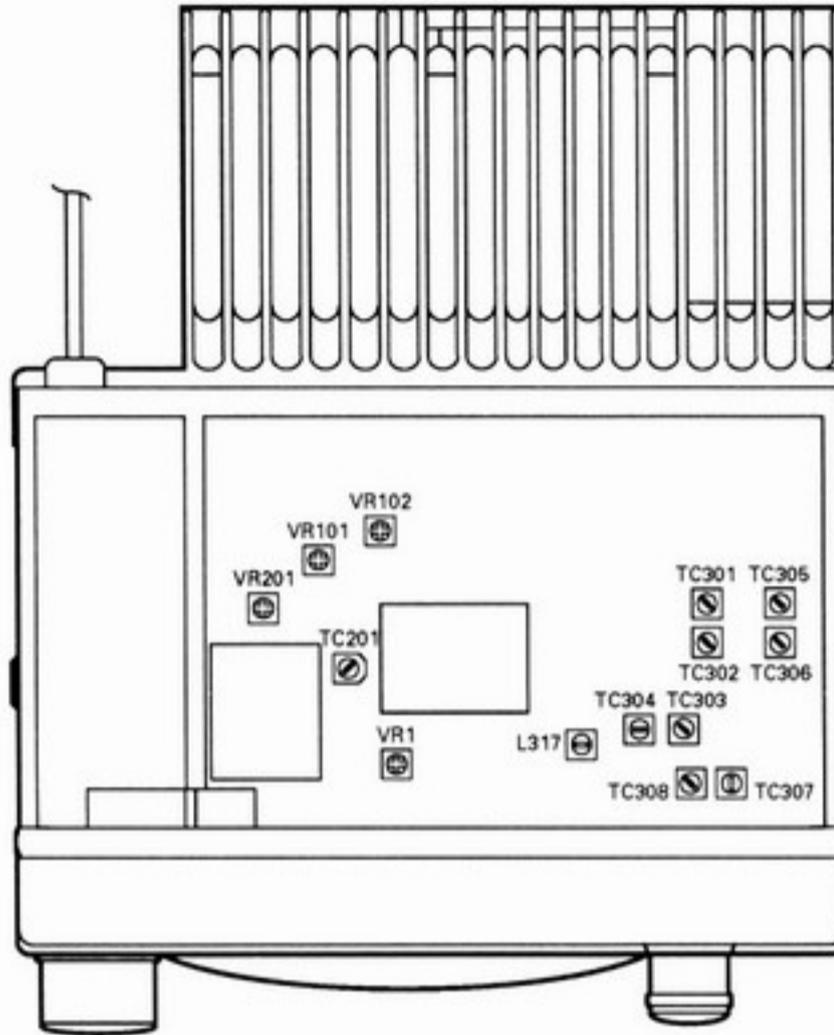
Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
2. DEV.	1) FREQ. : 435.000MHz M,M2,E,E2,E3,E9 FREQ. : 445.000MHz K,P AG : 1kHz/25mV E,E2,E3,E9 AG : 1kHz/50mV K,P,M,M2	Line detector Oscilloscope AG	Rear panel	ANT	TX-RX	VR201	±4.3kHz (larger one)	±200Hz
	2) AG : 1kHz/2.5mV E,E2,E3,E9 AG : 1kHz/5.0mV K,P,M,M2						Check	
3. TONE	1) FREQ. : 435.000MHz M,M2,E,E2,E3,E9 FREQ. : 445.000MHz K,P TONE key : ON Transmit After check TONE key : OFF	Line detector Oscilloscope	Rear panel	ANT			Check	±0.5~1.5kHz
4. DTSS	1) POWER SW : OFF Hold down the F, VFO, DTSS, and LOW keys, and turn the power switch on. Transmit Confirm, reset, and put the frequency in memory again.						Check the 1633Hz single tone.	±2.5kHz or more.
5. Abnormal spurious oscillation	1) M,M2,E,E3,E9 FREQ. : 430.000MHz FREQ. : 435.000MHz FREQ. : 439.940MHz K,P FREQ. : 438.000MHz FREQ. : 445.000MHz FREQ. : 449.940MHz Power : High/Mid/Low Power supply voltage : 11.5 to 16.0V	Spectrum analyzer					Check	Spurious : -60dB or less There must be no abnormal spurious oscillation.
6. CTCSS	1) FREQ. : 435.000MHz M,M2,E,E2,E3,E9 FREQ. : 445.000MHz K,P For only units containing TSU-8 Set the tones of the main unit and monitor unit to the same frequency. (Press the F key, then the TONE key.) Turn SQL VR until noise disappears. Adjust mutually.	Monitor unit					Check	Mutual adjustment must be possible.
	2) Change the tone frequency and transmit it from the monitor unit.							The squelch must not be open.
7. Protection	1) FREQ. : 439.940MHz M,M2,E,E2,E3,E9 FREQ. : 449.940MHz K,P ANT : Open ANT : Short Transmit	Ammeter					Check	10.0A or less.

ADJUSTMENT

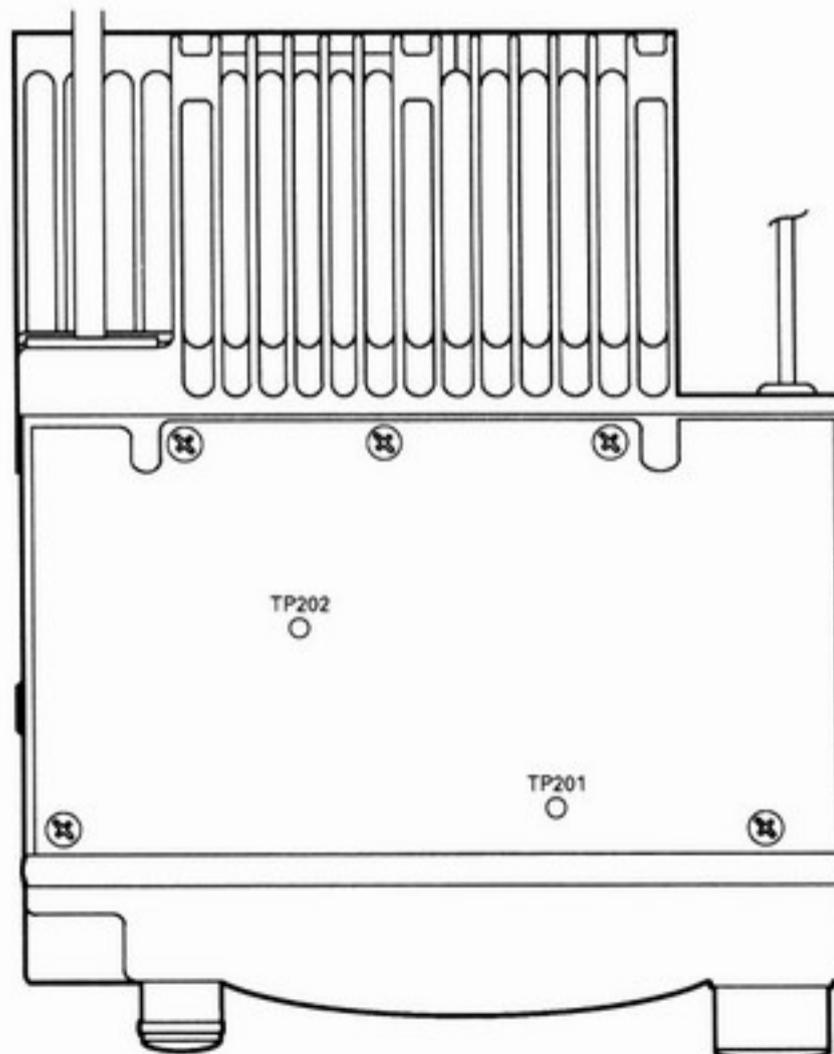
Adjustment Points

· Top view

- TC201 : Transmit frequency
- TC301~304 : 430MHz BPF
- TC305~308 : 144MHz BPF
- L317 : Crystal filter coil
- VR1 : S-meter (430MHz)
- VR101 : High power
- VR102 : Low power
- VR201 : DEV.



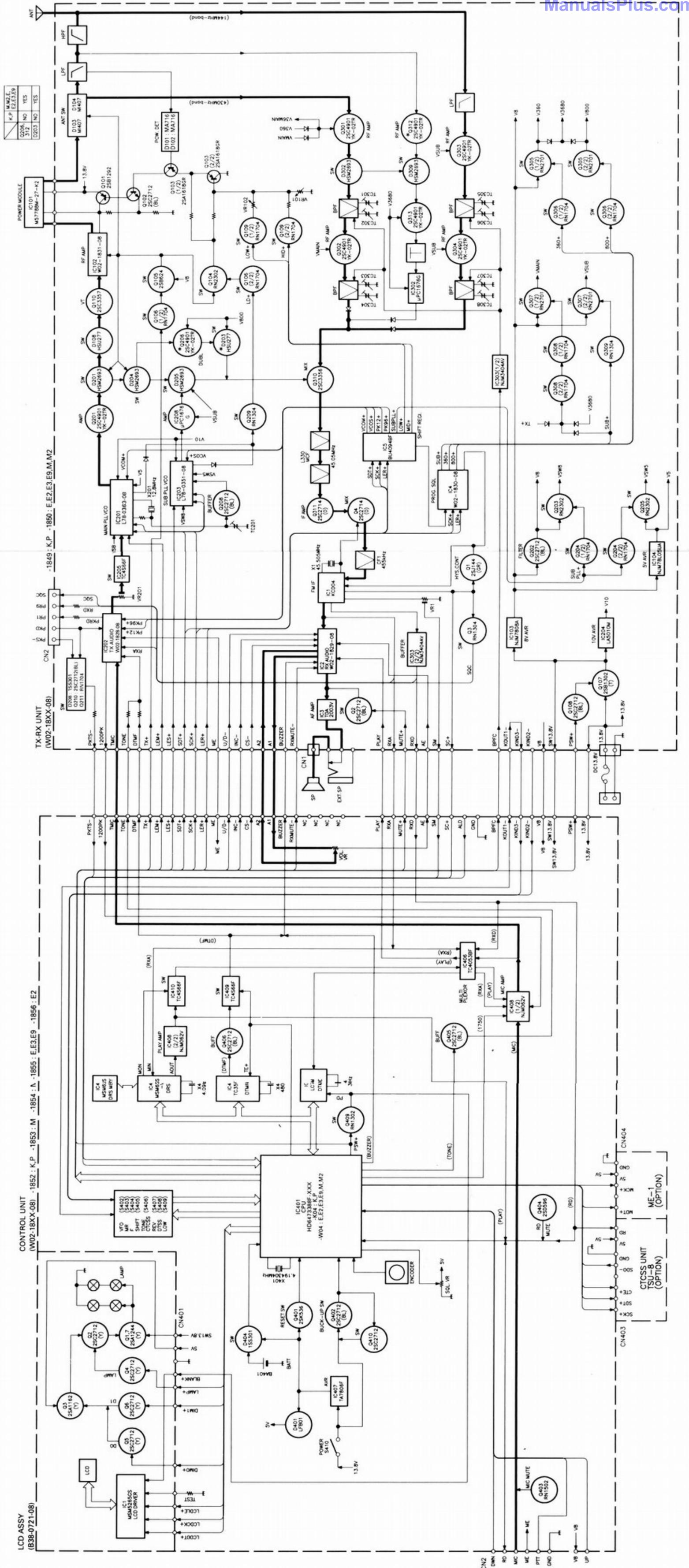
· Bottom view



TERMINAL FUNCTION

CN No.	Pin No.	Name	Function	CN No.	Pin No.	Name	Function
TX-RX UNIT							
CN1	1	GND	GND	CN402 MODULAR FPC MC-45	1	DWN	MIC SW DOWN, MR, PF input : (K bus serial input)
	2	SP	Speaker output		2	RD	Demodulation signal, DRS playback tone output : (Controller connection detection input)
CN2	1	PKD	Packet data modulation input		3	MIC	Microphone audio input : (Controller audio input)
	2	DE	GND		4	ME	Microphone ground (GND)
	3	PKS-	Packet PTT signal input		5	PTT	Microphone PTT input : (K bus serial output)
	4	PR9	Packet 9600-bps data demodulation output		6	GND	GND
PG-5A (Option)	5	PR1	Packet 1200-bps data demodulation output		7	V8	+8V
	6	SQC	Squelch control output		8	UP	MIC SW UP, CALL, VFO input : (K bus serial output)
CN201	1	GND	GND	CN403 TSU-8 (Option)	1	SCK+	CTCSS serial clock output
	2	KOUT1-	Frequency band identification data input		2	SDT+	CTCSS serial data output
	3	ALD	Connected to GND		3	CTE+	CTCSS serial data strobe output
	4	KIND2-	Frequency band identification data output		4	NC	
	5	BPFC	Receive RF band-pass filter control input		5	SDO-	CTCSS tone detection input
	6	KIND3-	Frequency band identification data output		6	GND	GND
	7	MUTE+	Audio mute control input		7	5V	+5V
	8	SDT+	PLL data, shift register serial data input		8	RD	Demodulation signal output
	9	SCK+	PLL data, shift register serial clock input	CN404 ME-1 (Option)	1	GND	GND
	10	LEM+	430MHz-band PLL enable input (main PLL)		2	5V	+5V
	11	LES+	144MHz-band PLL enable input (sub PLL)	3	MCK+	ME-1 serial clock output	
	12	LER+	Shift register enable input	4	NC		
	13	TX+	Transmission start signal input	5	MDT+	ME-1 serial data input/output	
	14	NC		CN405 TX-RX UNIT CN201	1	GND	GND
	15	NC			2	KOUT1-	Frequency band identification data output
	16	NC			3	ALD	Not used
	17	SC+	Squelch busy control output		4	KIND2-	Frequency band identification data input
	18	SM	S-meter output		5	BPFC	Receive RF band-pass filter control output
	19	RXA	Audio signal output		6	KIND3-	Frequency band identification data input
	20	RXD	Demodulation signal output		7	MUTE+	Audio mute control output
CN202	1	NC			8	SDT+	PLL data, shift register serial data output
	2	U/D-	Audio electronic VR up/down control input		9	SCK+	PLL data, shift register serial clock output
	3	INC-	Audio electronic VR increment control input		10	LEM+	430MHz-band PLL enable output (main PLL)
	4	CS-	Audio electronic VR chip select input		11	LES+	144MHz-band PLL enable output (sub PLL)
	5	AE	GND		12	LER+	Shift register enable output
	6	A2	Audio input (from AF VOL of control unit)	13	TX+	Transmission start signal output	
	7	A1	Audio output (to AF VOL of control unit)	14	NC		
	8	BUZZER	Beeper input (Beep and DTMF tone)	15	NC		
	9	RX MUTE-	Receive audio mute control input	16	NC		
	10	PLAY	Digital recording playback tone input	17	SC+	Squelch busy control input (To CPU)	
	11	ME	MIC GND	18	SM	S-meter input (To CPU)	
	12	DTMF	DTMF modulation input	19	RXA	Audio signal input	
	13	TONE	Sub-tone modulation input	20	RXD	Demodulation signal input	
	14	TMIC	Audio input (from the mic amp circuit of control unit)	CN406 TX-RX UNIT CN202	1	NC	
	15	1200PK	Packet modulation data 1200-bps output		2	U/D-	Audio electronic VR up/down control output
	16	PKTS-	Packet PTT output		3	INC-	Audio electronic VR increment control output
	17	PSW+	Power switch control input		4	CS-	Audio electronic VR chip select output
	18	V8	+8V		5	AE	GND
	19	SW13.8V	Switched 13.8V		6	A2	Audio output (from AF VOL)
	20	13.8V	+13.8V		7	A1	Audio input (to AF VOL)
CONTROL UNIT					8	BUZZER	Beeper output (Beep and DTMF tone)
CN401 LCD ASSY	1	LCDDT+	LCD driver data output		9	RX MUTE-	Receive audio mute control output
	2	LCDCk+	LCD driver clock output		10	PLAY	Digital recording playback tone output
	3	LCDLE+	LCD driver enable output		11	ME	MIC GND
	4	TEST+	Not used		12	DTMF	DTMF modulation output
	5	DIM0+	Dimmer control output	13	TONE	Sub-tone modulation output	
	6	DIM1+	Dimmer control output	14	TMIC	Audio output (from the mic amp circuit)	
	7	LAMP+	Lamp drive output	15	1200PK	Packet modulation data 1200-bps input	
	8	BLANK+	LCD blank display control output.	16	PKTS-	Packet PTT input	
	9	GND	GND	17	PSW+	Power switch control output	
	10	5V	+5V	18	V8	+8V	
	11	SW13.8V	Switched 13.8V	19	SW13.8V	Switched 13.8V	
			20	13.8V	+13.8V		

BLOCK DIAGRAM



IC1: M5778M-27-42

IC201: L78-0351-08

IC202: L78-0351-08

IC301: M5778M-27-42

IC302: M5778M-27-42

IC401: HD64738BF-XXX

IC402: M5778M-27-42

IC403: M5778M-27-42

IC404: M5778M-27-42

IC405: M5778M-27-42

IC406: M5778M-27-42

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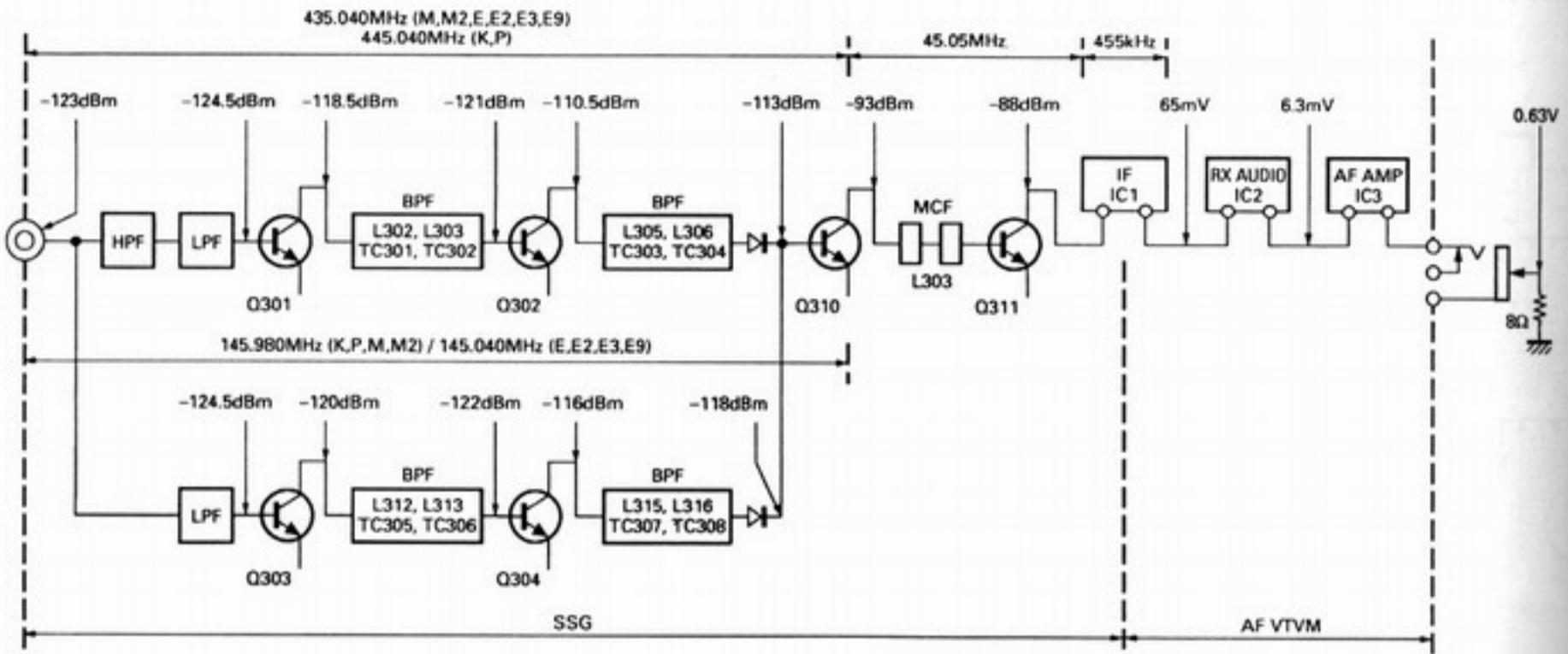
IC610: M5778M-27-42

IC611: M5778M-27-42

IC612: M5778M-27-42

LEVEL DIAGRAM

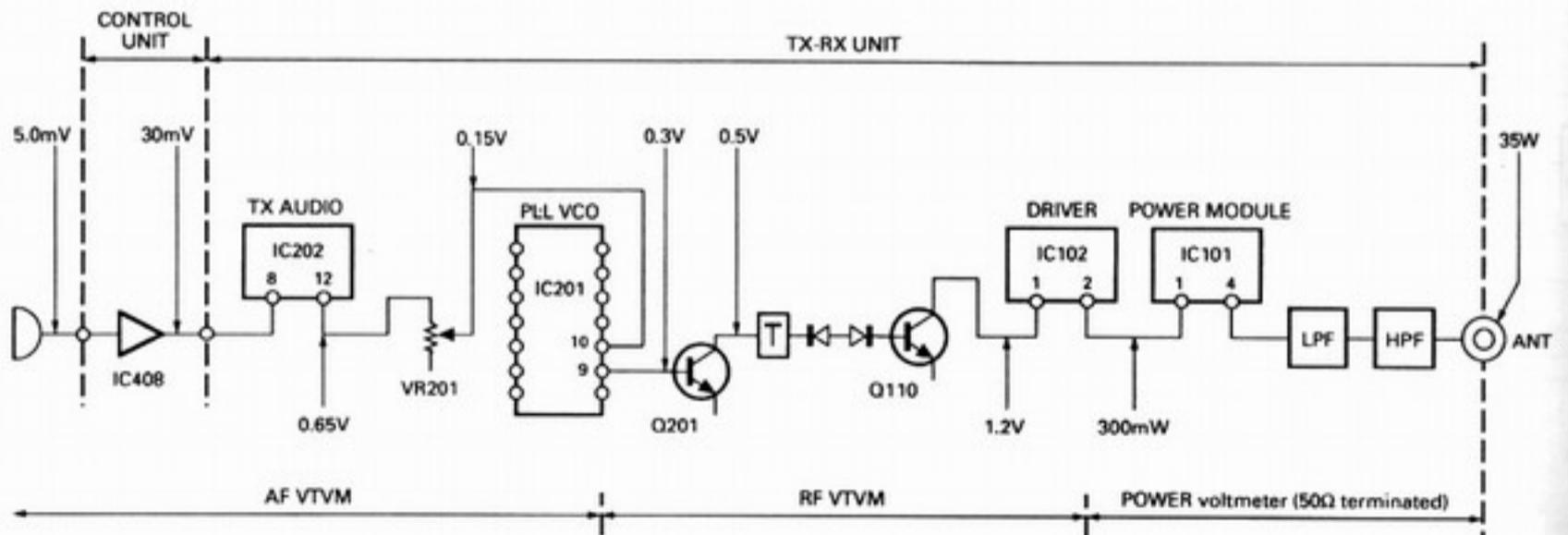
Receiver Section



Note 1: 12dB SINAD is obtained at this signal generator level when the signal is input from the signal generator via the 0.01μF coupling at each point the first IF.

Note 2: The AF level is measured with the AF valve voltmeter when the 40dBμ (-73dBm) signal generator signal that is modulated by a modulation signal of 1kHz with a deviation of 3kHz is received and the AF output is adjusted with AF VOL to 0.63V/8Ω.

Transmitter Section



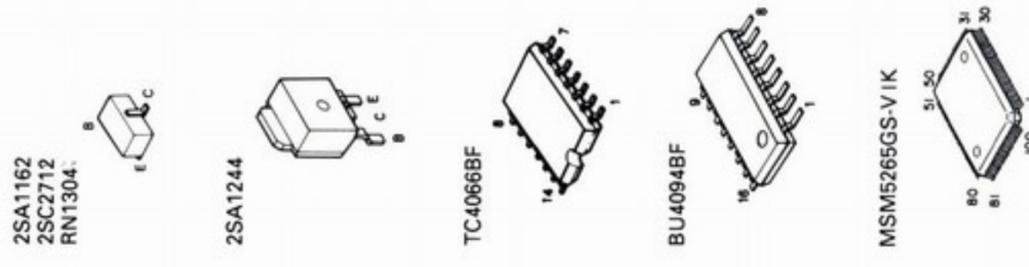
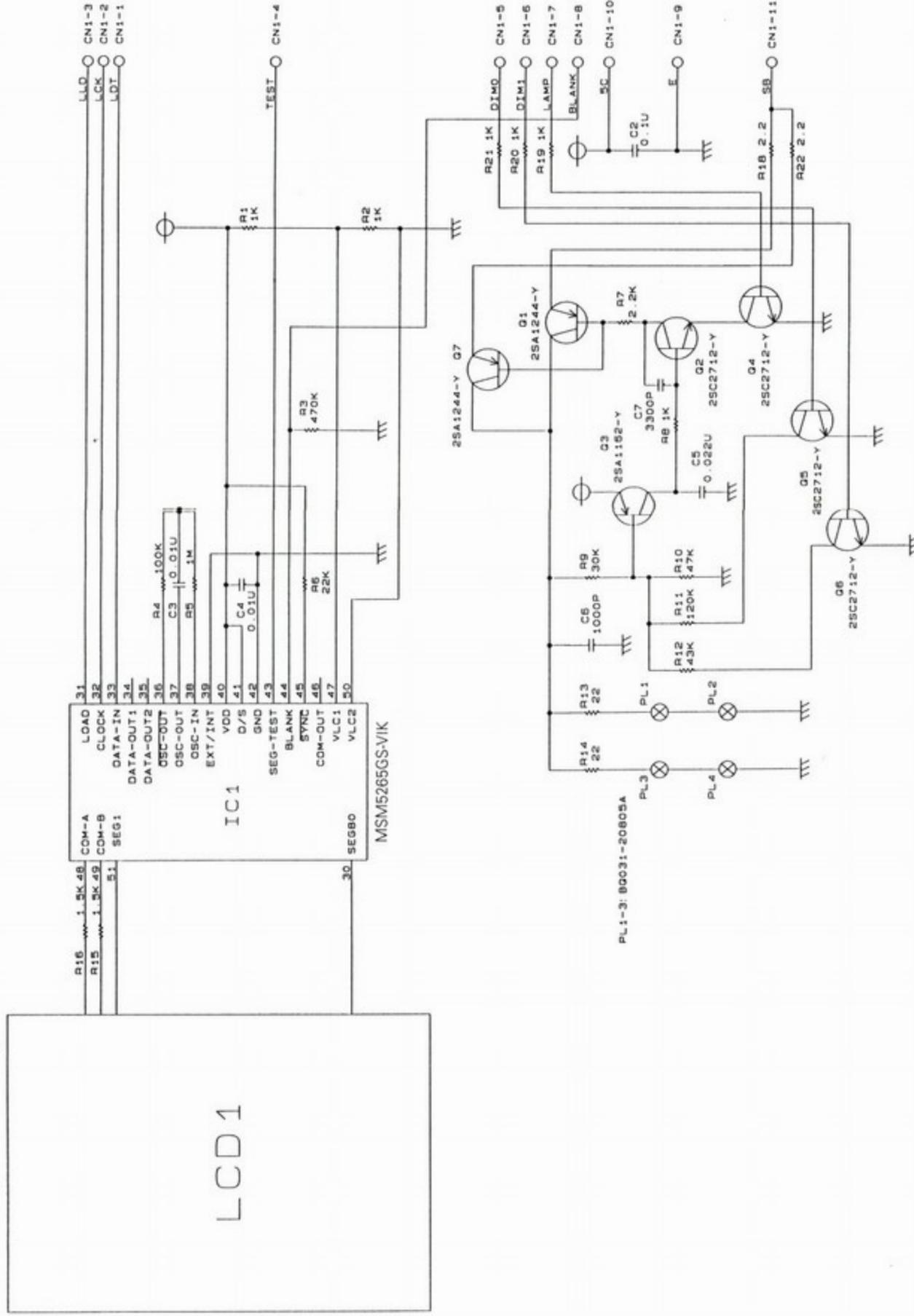
Note 1: Set the AF generator so that the MIC socket input is 3kHz DEV at 1kHz MOD.

Note 2: The transmit frequency is 435.000MHz (M, M2, E, E2, E3, E9), 445.000MHz (K, P).

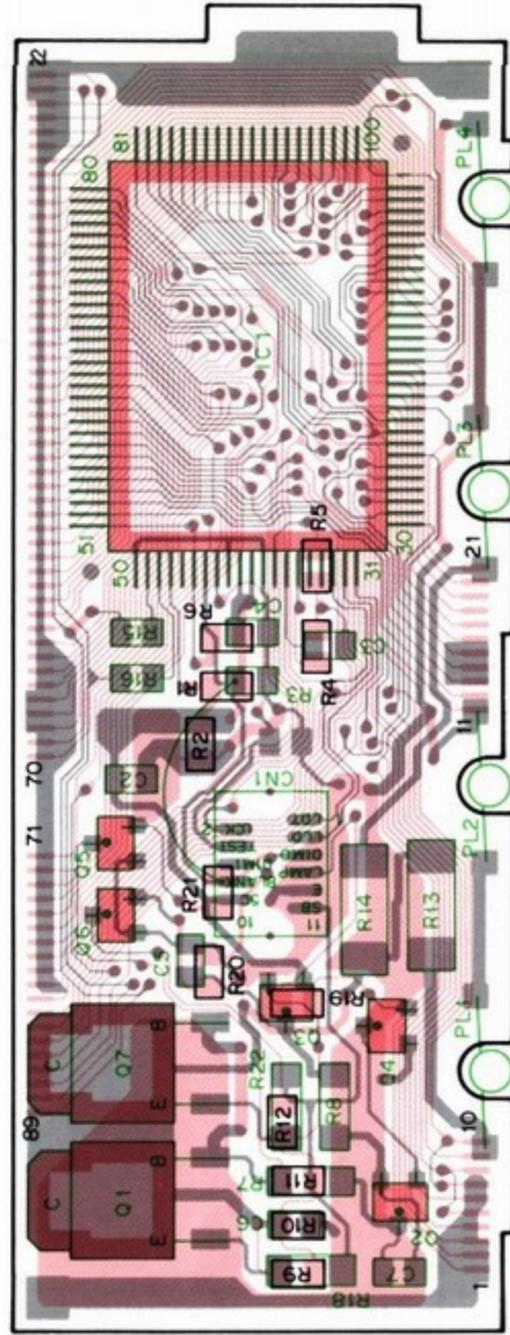
Note 3: The High/Low switch is High.

TM-451A/E CIRCUIT DIAGRAM / PC BOARD VIEWS

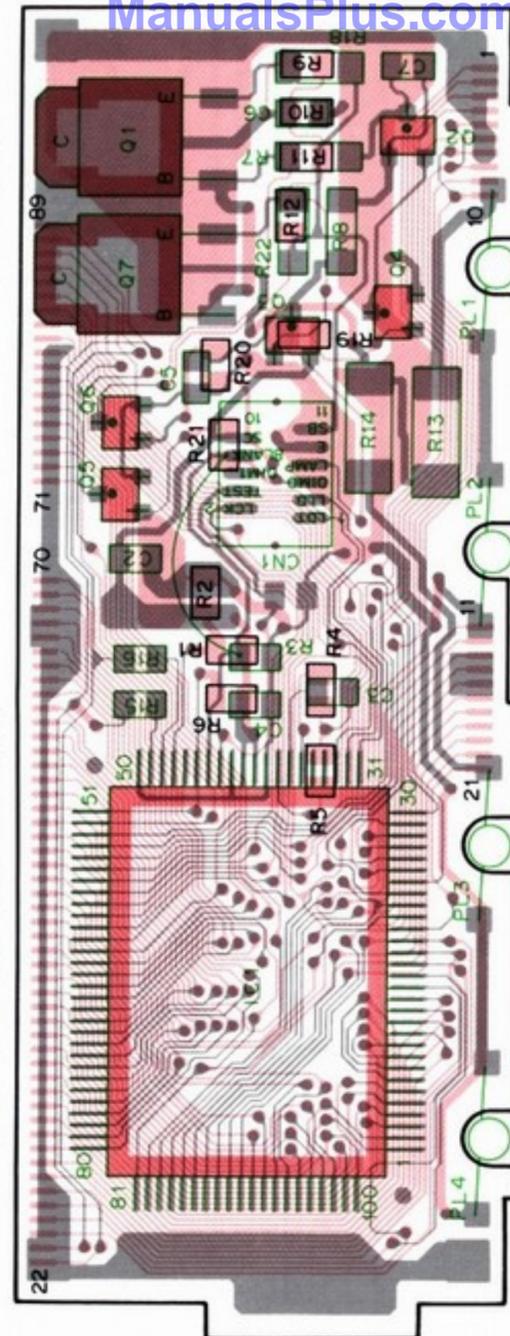
LCD ASSY (B38-0721-08)



LCD ASSY (B38-0721-08) Component side view



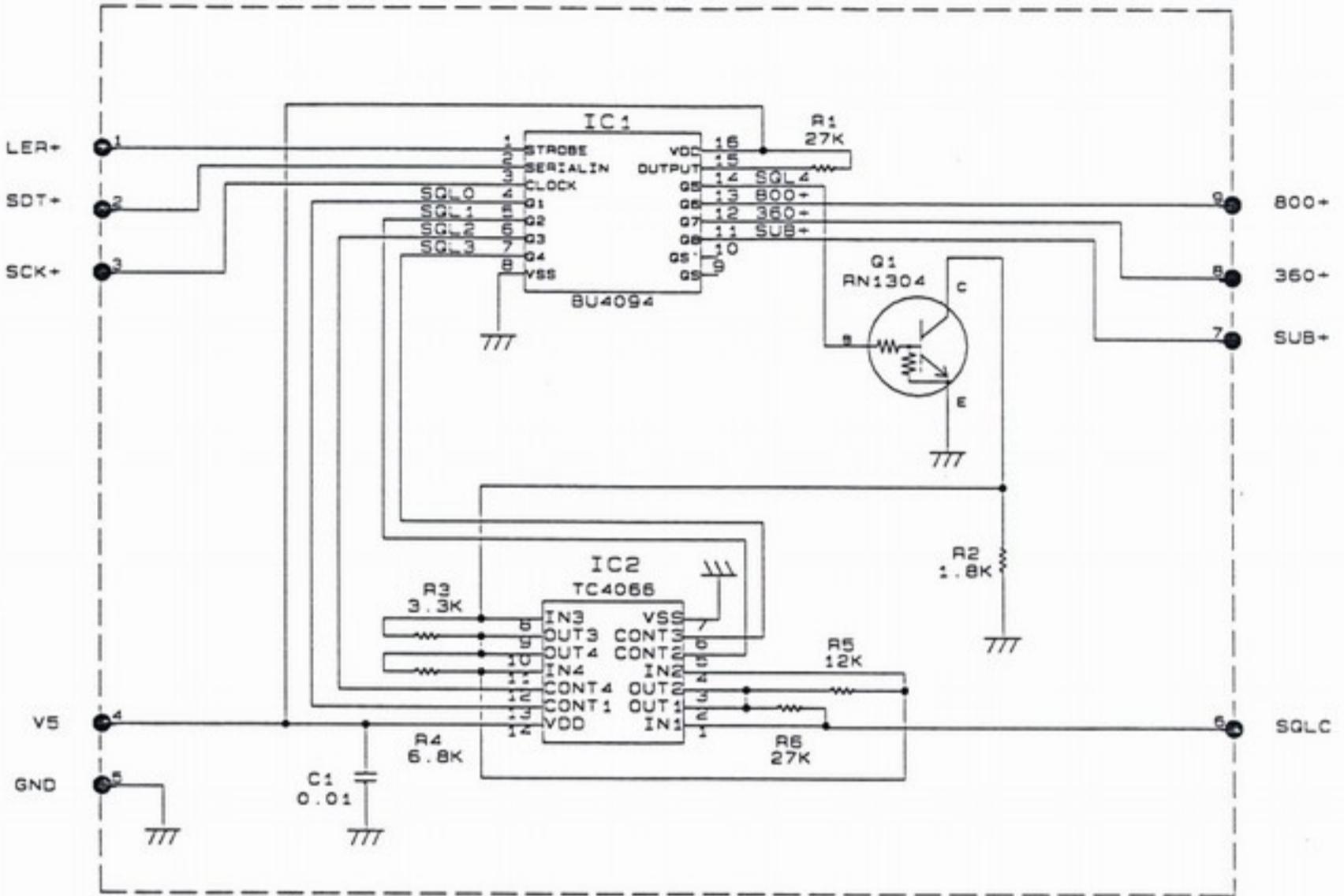
LCD ASSY (B38-0721-08) Foil side view



Component side
Foil side

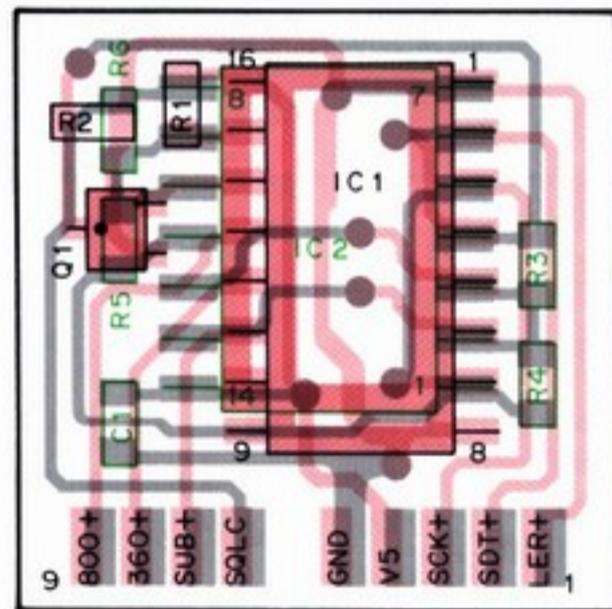
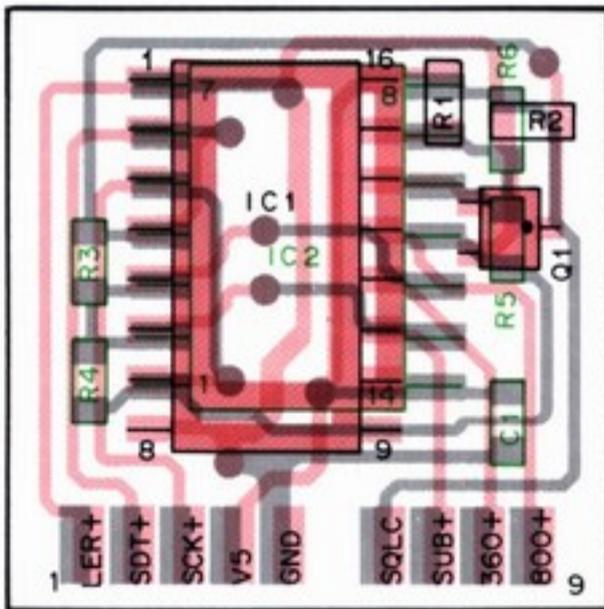
CIRCUIT DIAGRAM / PC BOARD VIEWS ManualsPlus.com

IC4 : PROG. SQL (W02-1830-08)



IC4 : PROG SQL (W02-1830-08)
Component side view

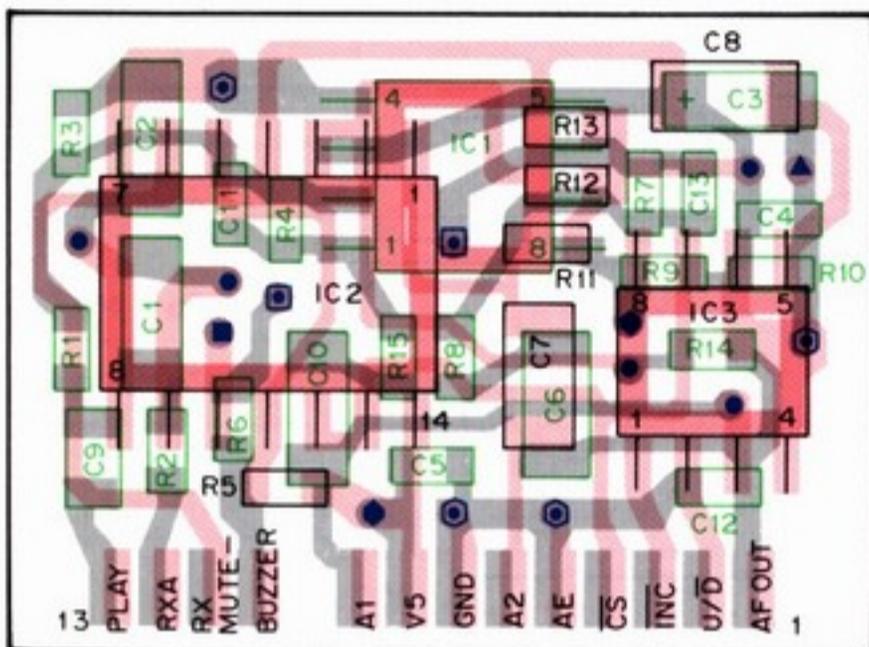
IC4 : PROG SQL (W02-1830-08)
Foil side view



Component side
Foil side

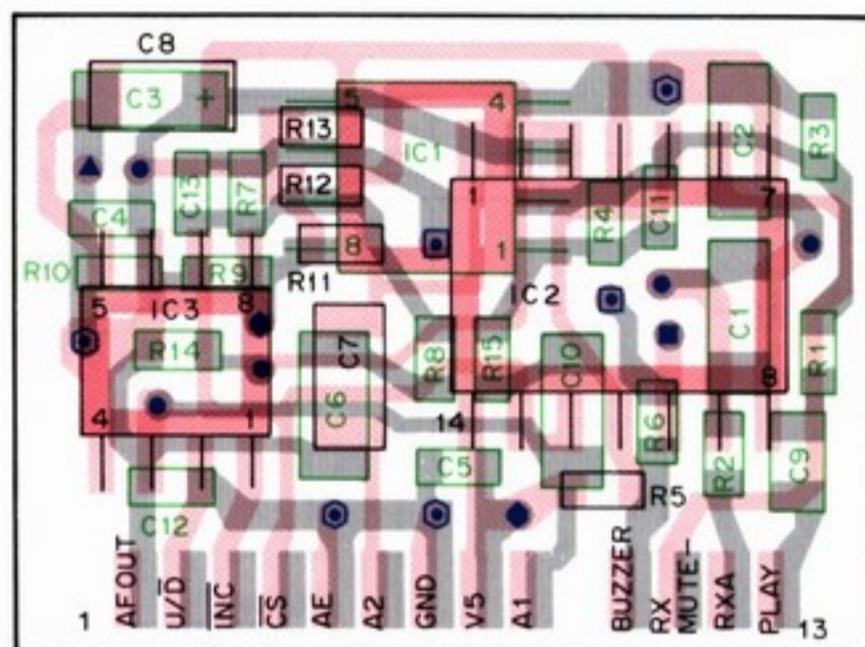
TM-451A/E PC BOARD VIEWS

IC2 : RX AUDIO (W02-1829-08)
Component side view

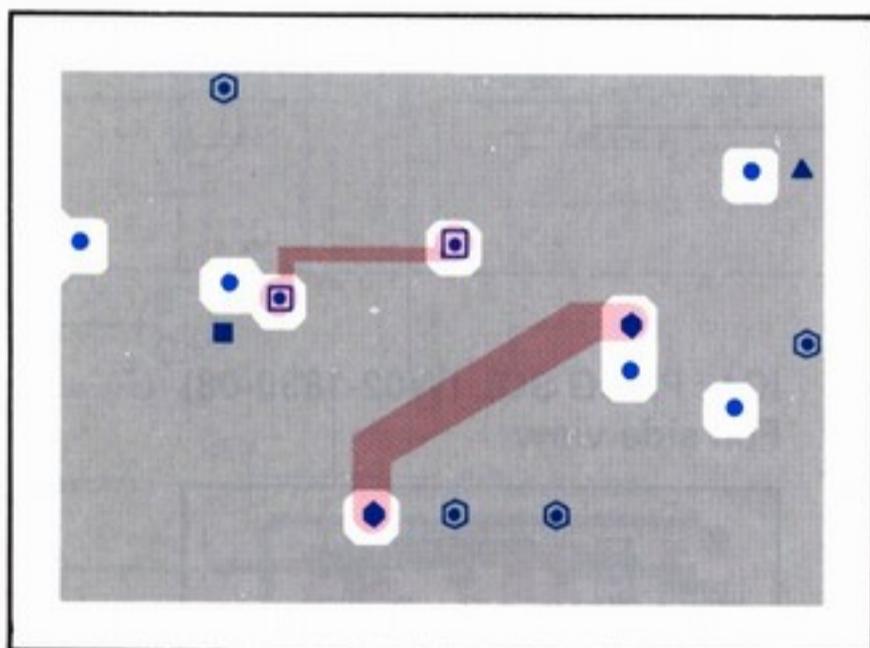


A pattern
B pattern

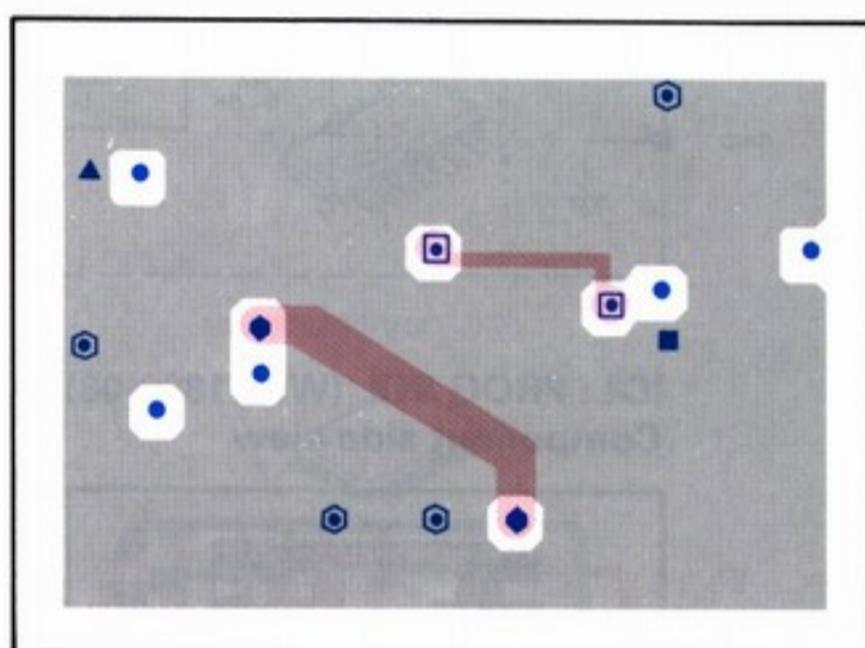
IC2 : RX AUDIO (W02-1829-08)
Foil side view



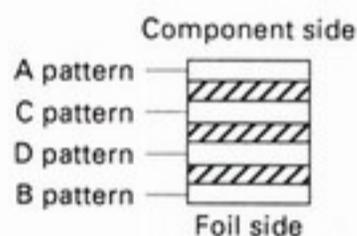
A pattern
B pattern



C pattern
D pattern

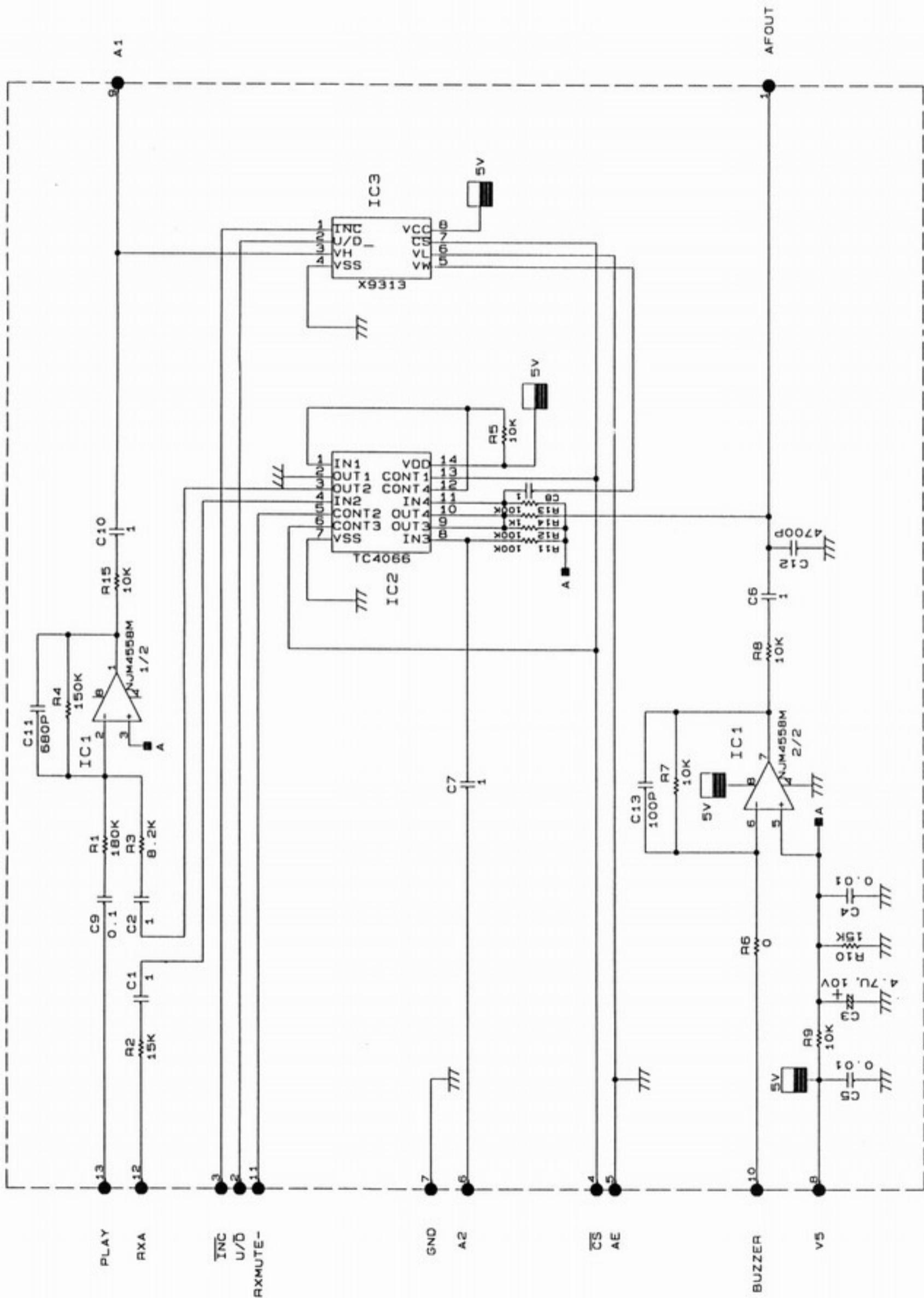


C pattern
D pattern

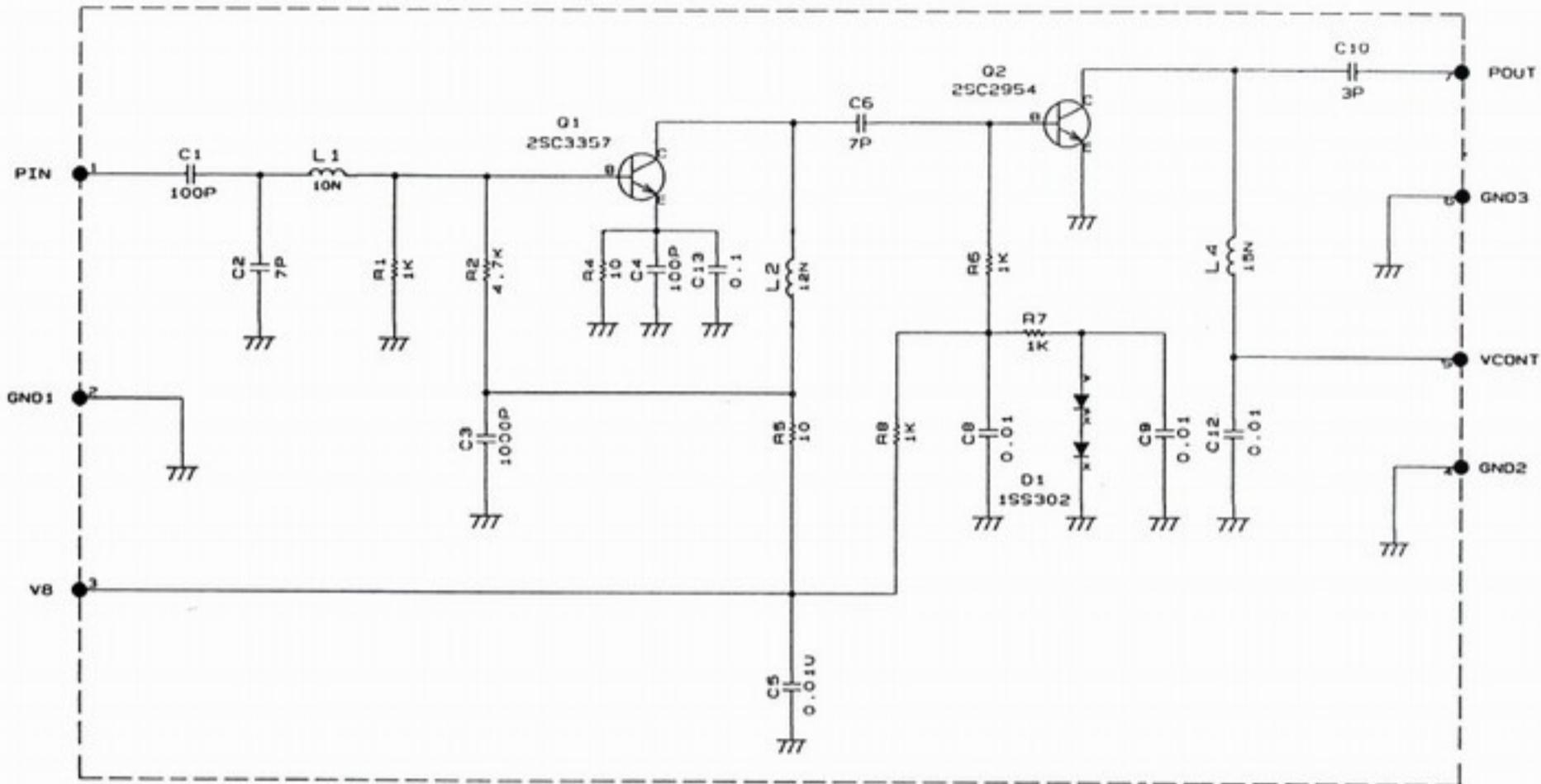


- A and B connected
- ⊙ A and C connected
- A and D connected
- ◻ B and C connected
- ▲ B and D connected
- △ C and D connected
- A, B and C connected
- ⊙ A, B and D connected
- ⊙ A, C and D connected
- ◻ B, C and D connected
- ▲ A, B, C and D connected
- A only
- ◻ B only
- △ C only
- D only
- No mark is not connected

IC2 : RX AUDIO (W02-1829-08)

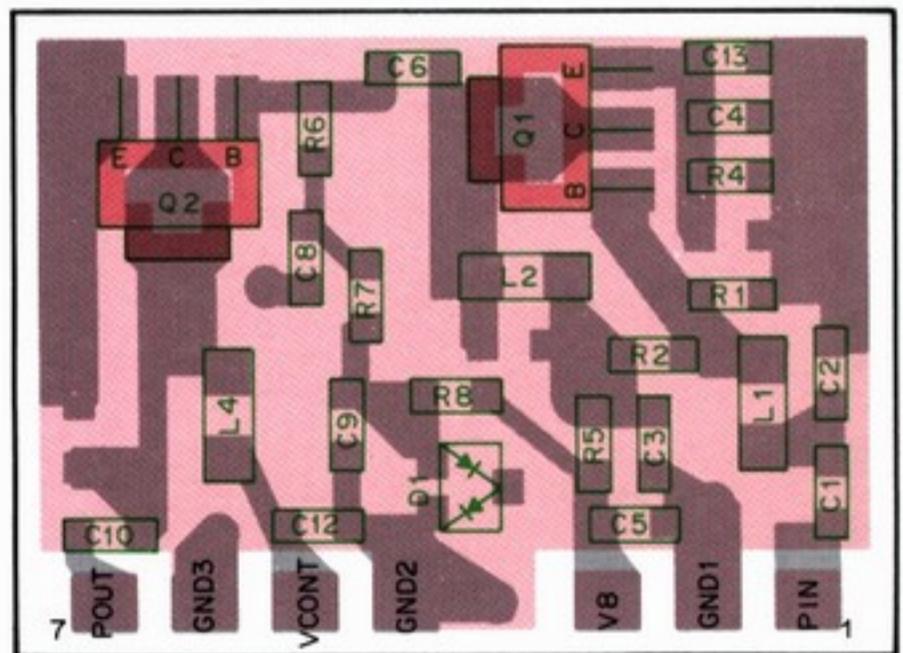
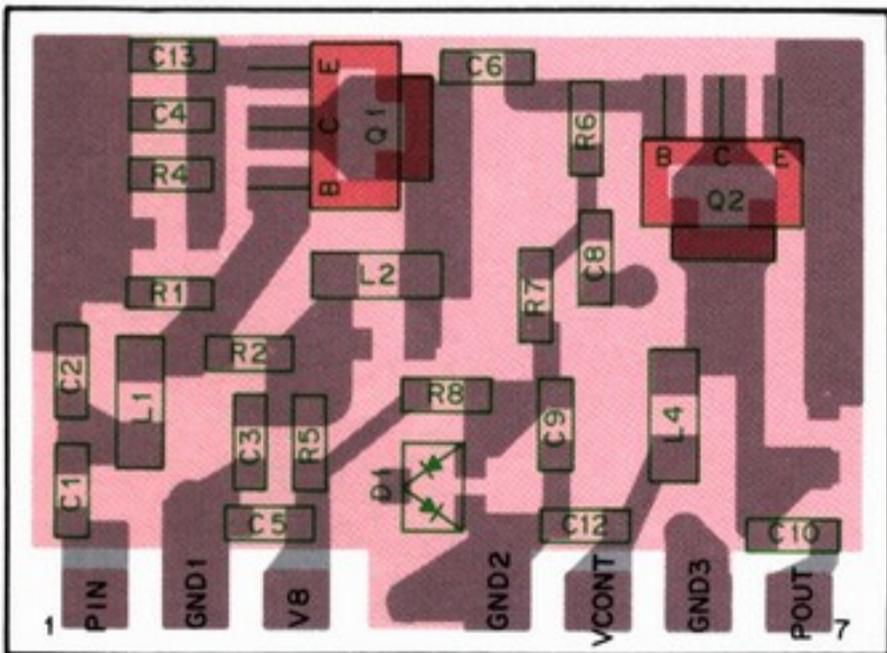


IC102 : RF AMP (W02-1831-08)



IC102 : RF AMP (W02-1831-08)
Component side view

IC102 : RF AMP (W02-1831-08)
Foil side view

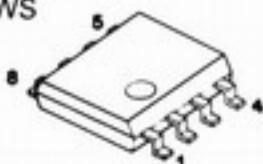


Component side
Foil side

2SC2954
2SC3357



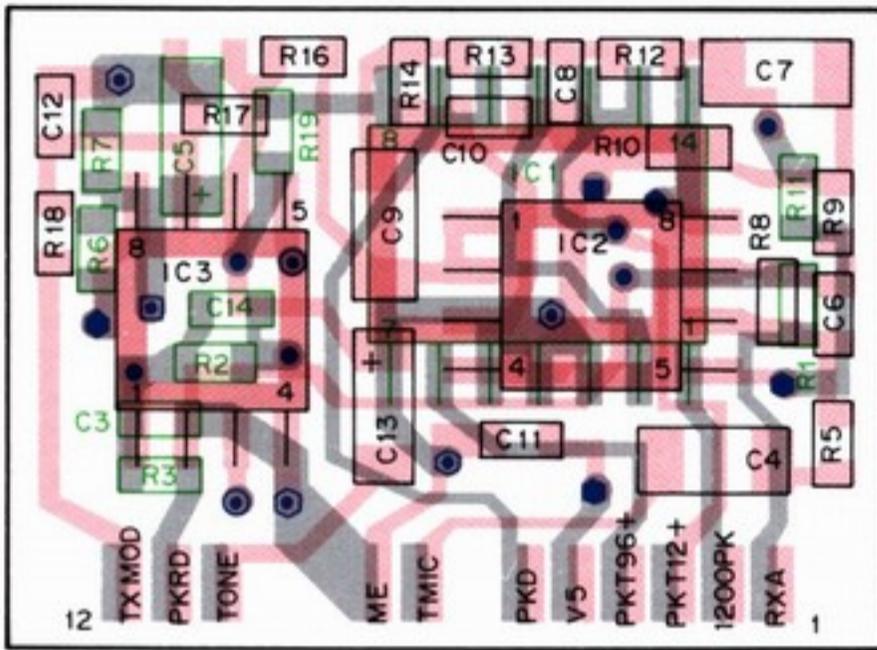
NJM3404AM
NJM4558M
X9313WS



TC4066BF

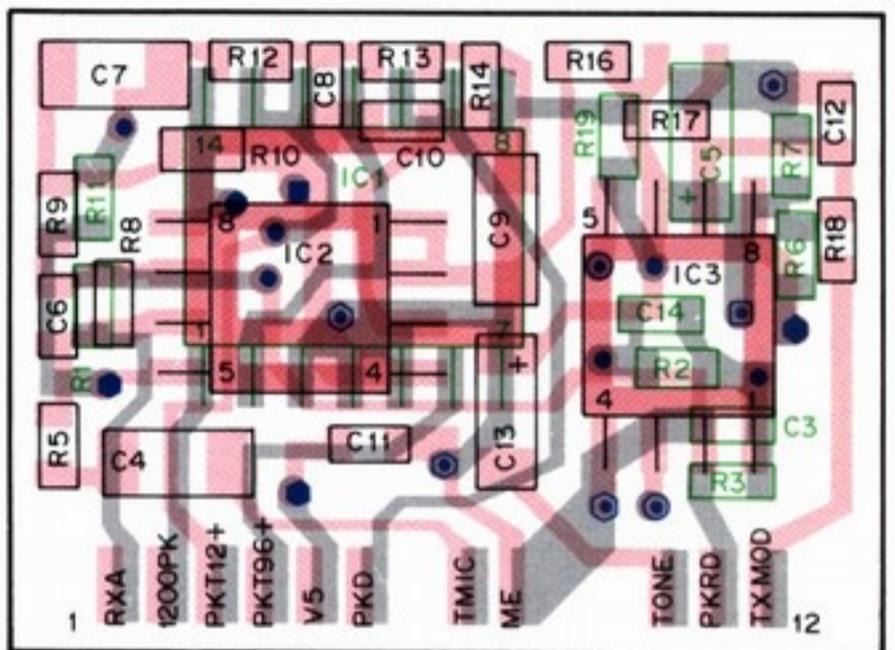


IC202 : TX AUDIO (W02-1828-08)
Component side view

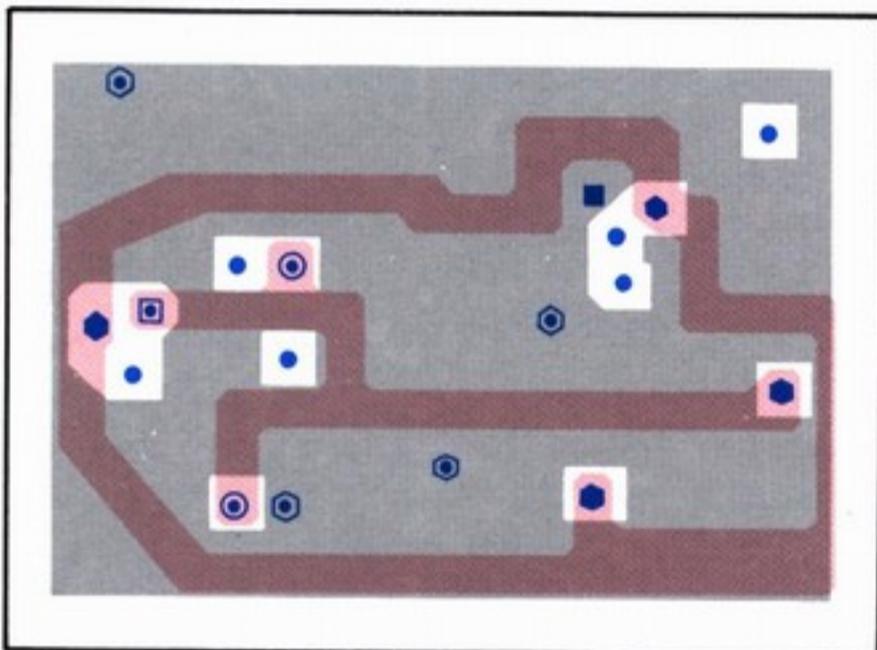


■ A pattern
■ B pattern

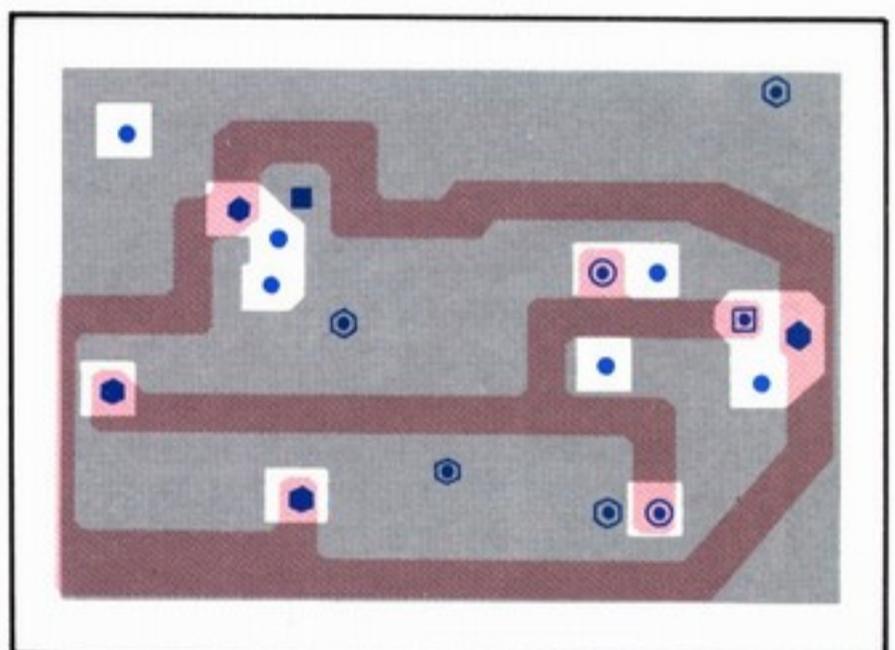
IC202 : TX AUDIO (W02-1828-08)
Foil side view



■ A pattern
■ B pattern

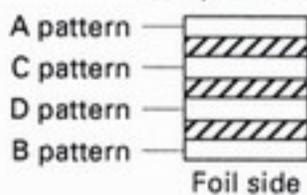


■ C pattern
■ D pattern



■ C pattern
■ D pattern

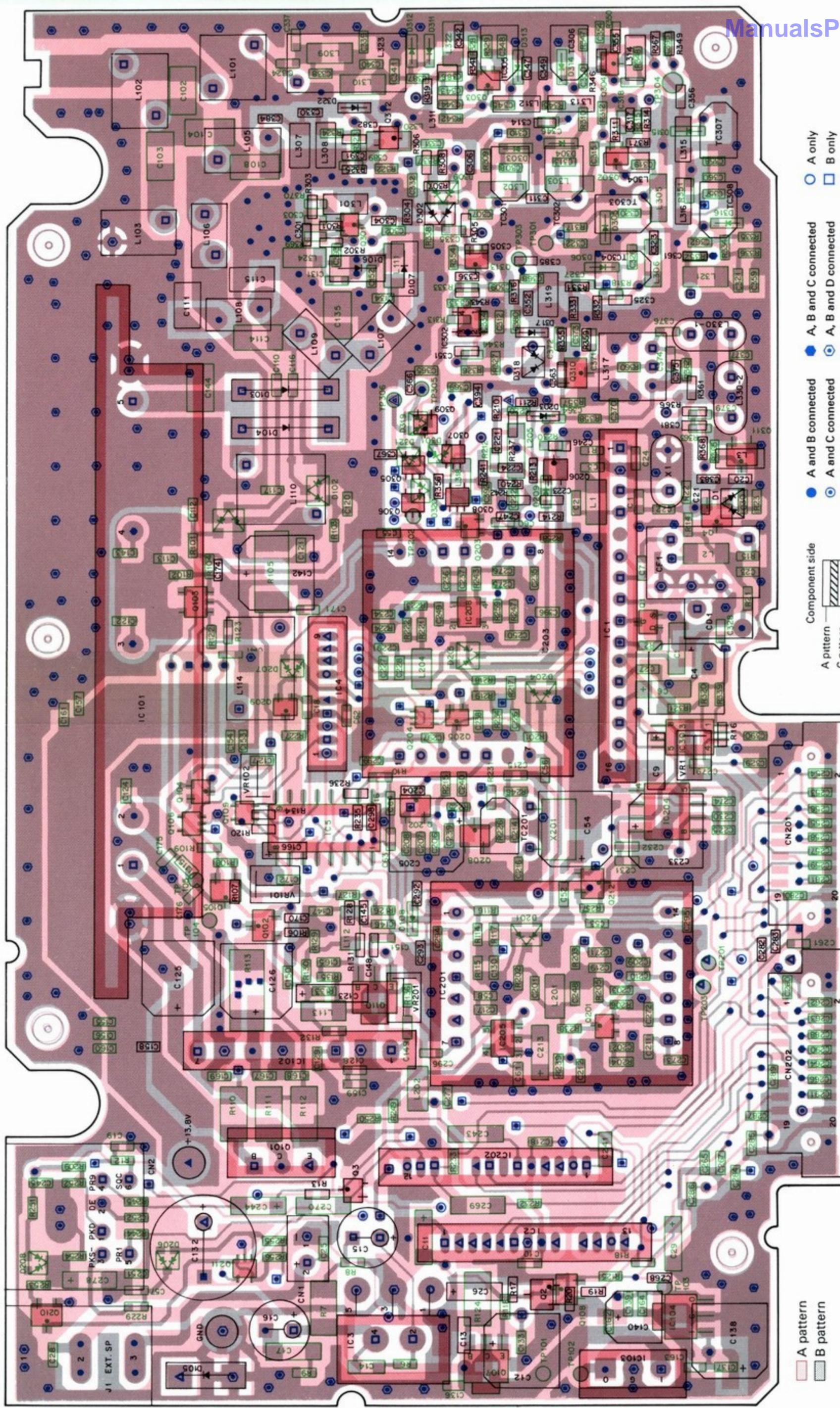
Component side



- A and B connected
- ⊙ A and C connected
- A and D connected
- ⊠ B and C connected
- ▲ B and D connected
- △ C and D connected
- A, B and C connected
- ⊙ A, B and D connected
- ⊙ A, C and D connected
- ⊠ B, C and D connected
- ▲ A, B, C and D connected
- A only
- B only
- △ C only
- D only
- No mark is not connected

TM-451A/E PC BOARD VIEWS

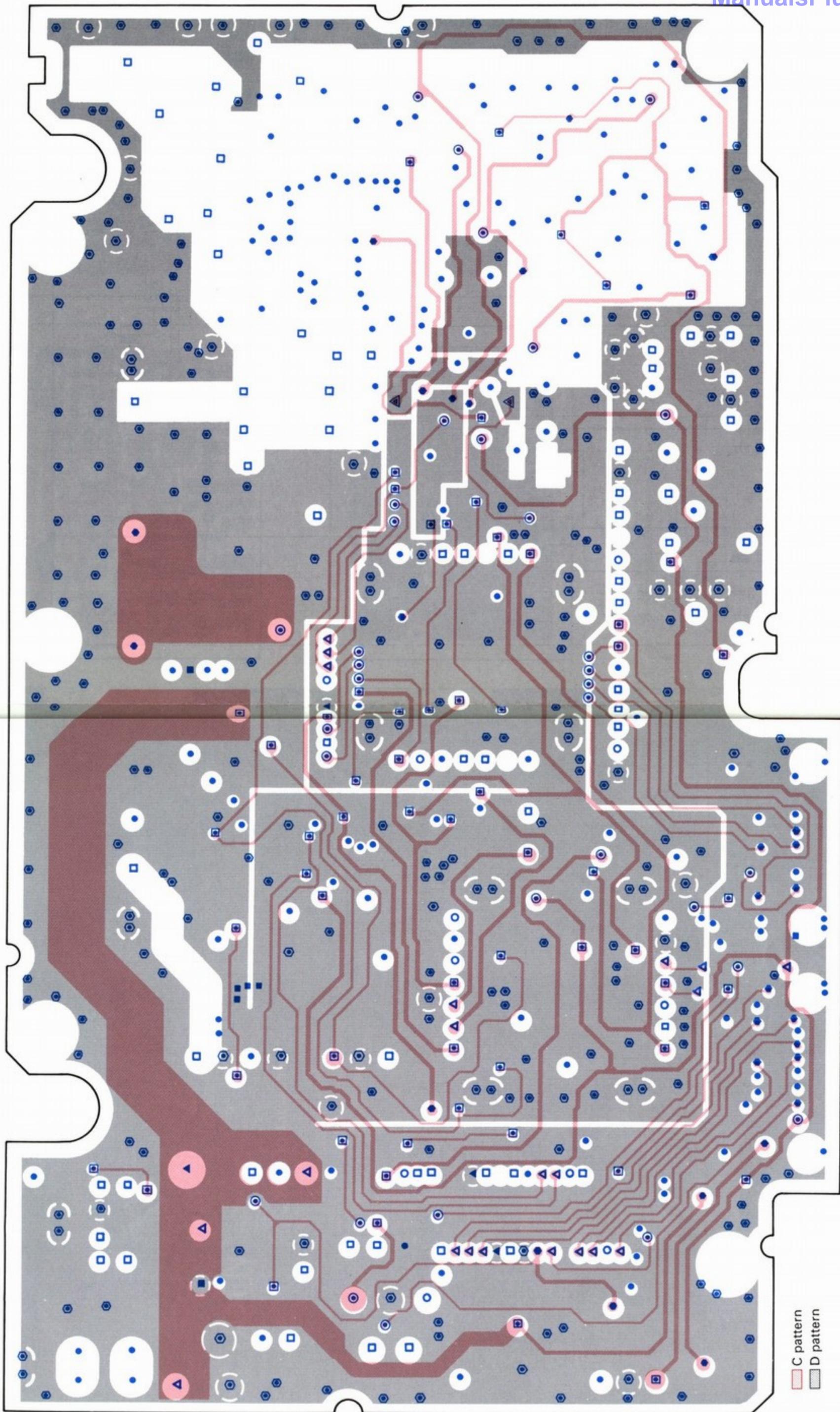
TX-RX UNIT (W02-18XX-08) 1849 : K,P 1850 : M,M2,E,E2,E3,E9 Component side view



A pattern
B pattern

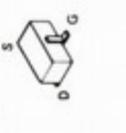
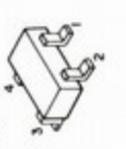
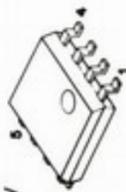
Component side
A pattern
C pattern
D pattern
B pattern
Foil side

- A and B connected
- A and C connected
- A and D connected
- B and C connected
- ▲ B and D connected
- △ C and D connected
- A only
- B only
- △ C only
- D only
- No mark is not connected
- A, B and C connected
- A, B and D connected
- A, C and D connected
- B, C and D connected
- ▲ A, B, C and D connected

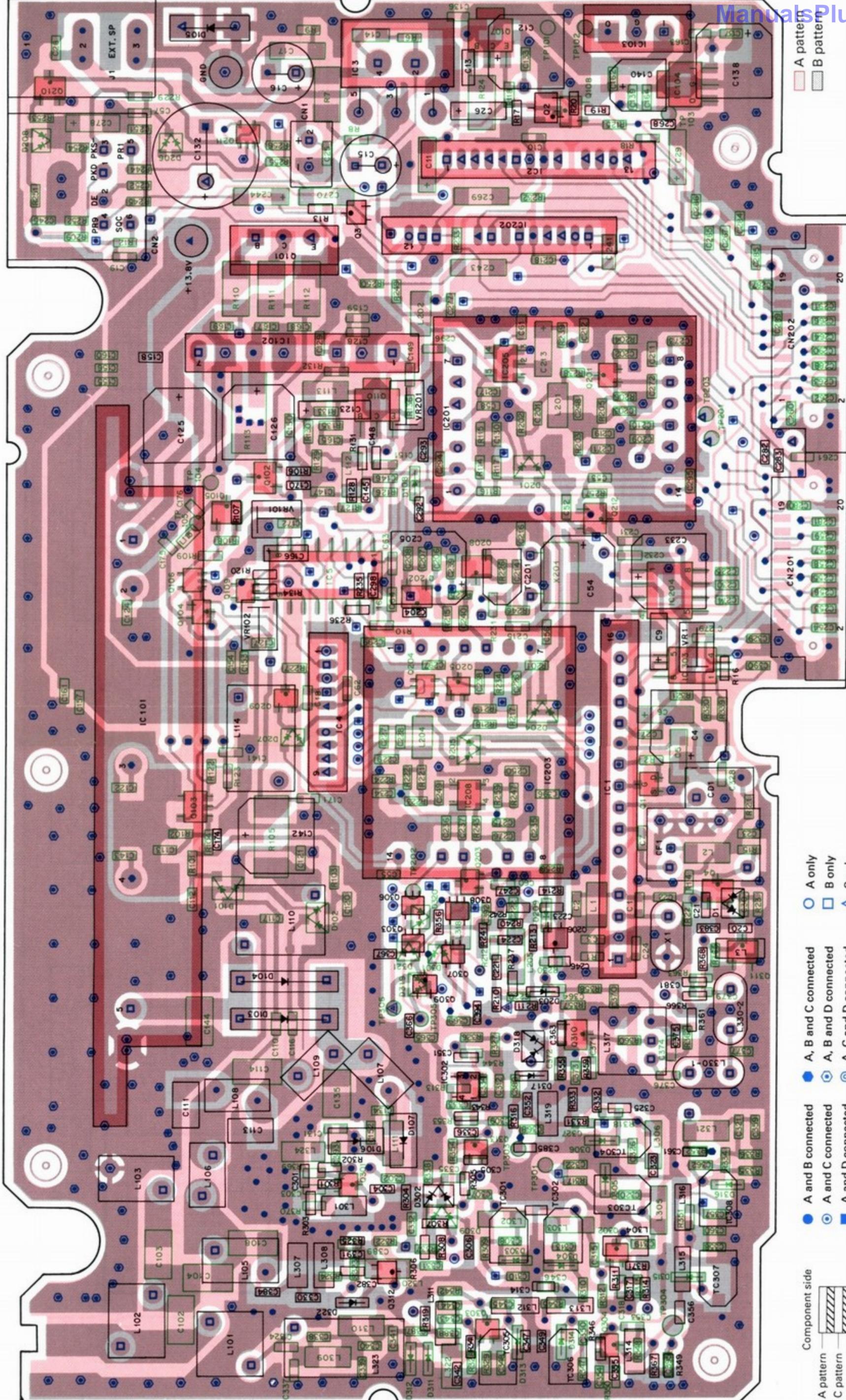


C pattern
 D pattern

- 25B624
- 25C2712
- 25C2714
- 25C3356
- 2SC4901YK-02TR
- RN1304
- RN2302
- 2SB1302
- 2SC3357
- 2SJ144
- NJM78L05UA
- µPC1676G
- M57788M-27-K2
- TC4S66F
- LA5010M
- NJM3404AV



TX-RX UNIT (W02-18XX-08) 1849 : K,P 1850 : M,M2,E,E2,E3,E9 Foil side view



Component side

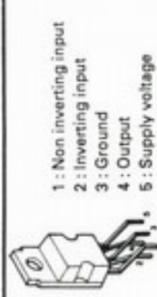
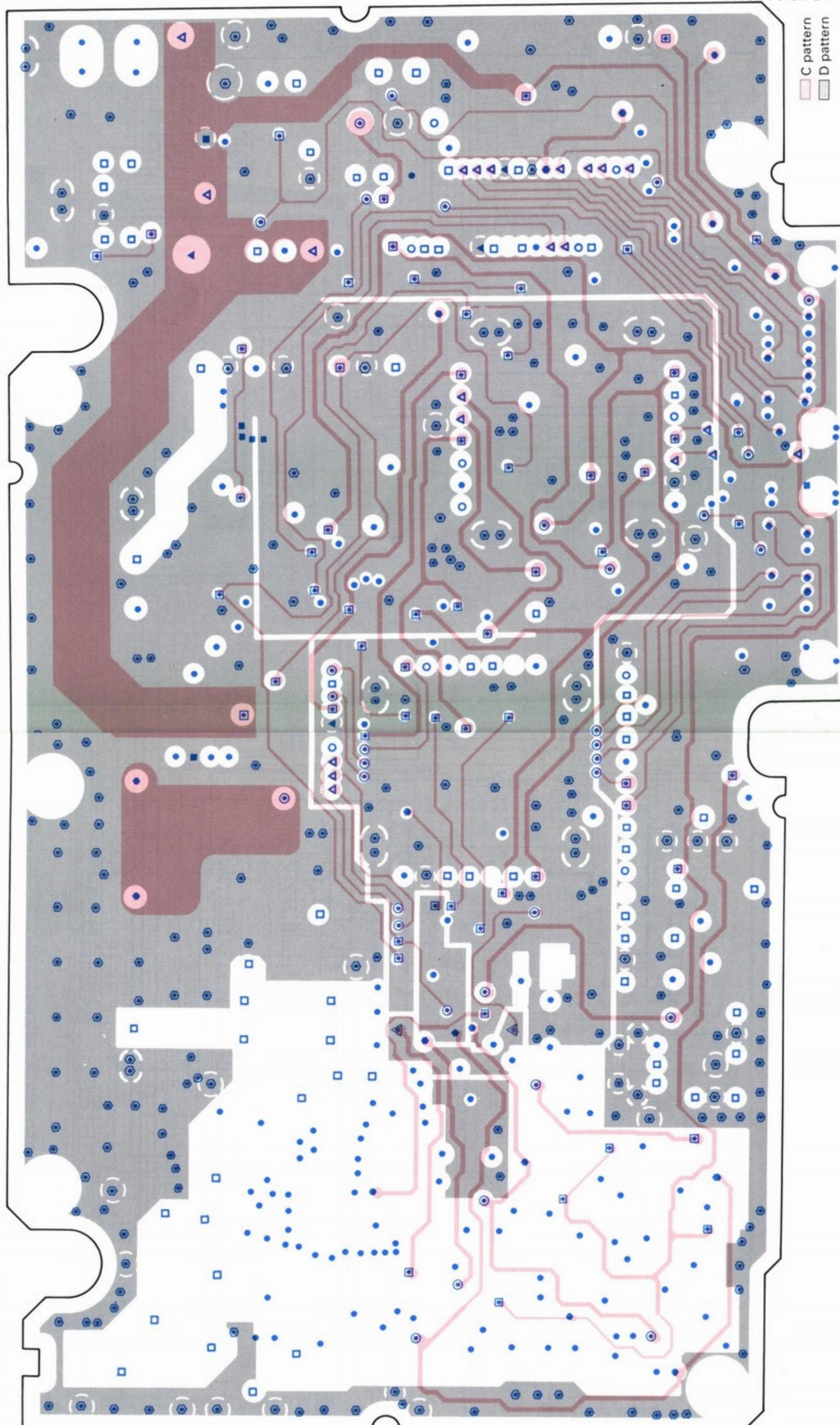
A pattern	Diagonal lines (top-left to bottom-right)
C pattern	Diagonal lines (top-right to bottom-left)
D pattern	Horizontal lines
B pattern	Vertical lines

Foil side

●	A and B connected	○	A only
⊙	A and C connected	□	B only
⊠	A and D connected	△	C only
⊡	B and C connected	◇	D only
▲	B and D connected	⬜	No mark is not connected
⬜	C and D connected		

J
I
H
G
F
E
D
C
B

PC BOARD VIEWS TM-451A/E



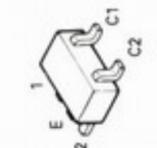
TDA2003V



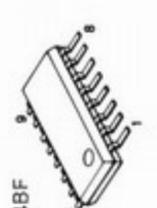
NJMM7808A



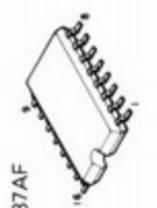
2SB1292



2SA1618GR
RN1704
RN2701

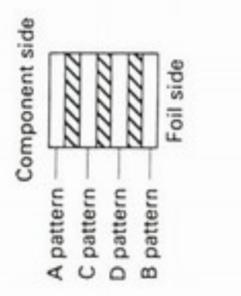
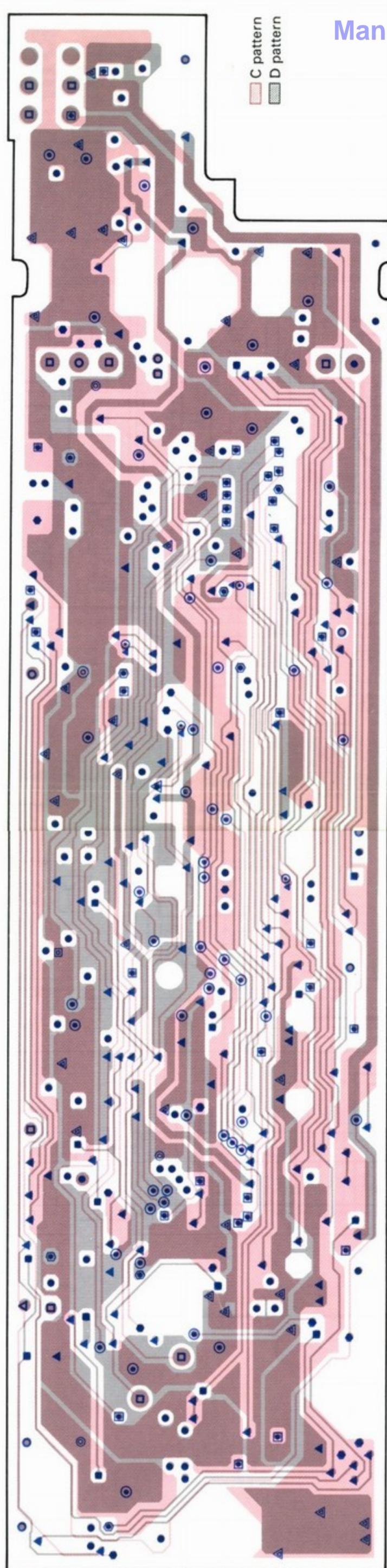
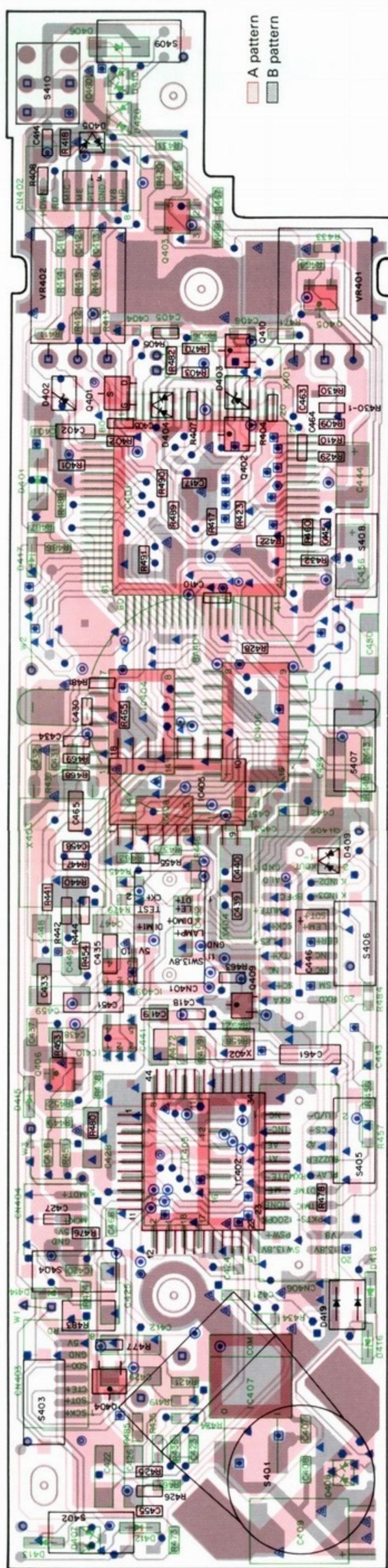


BU4094BF



TA7787AF

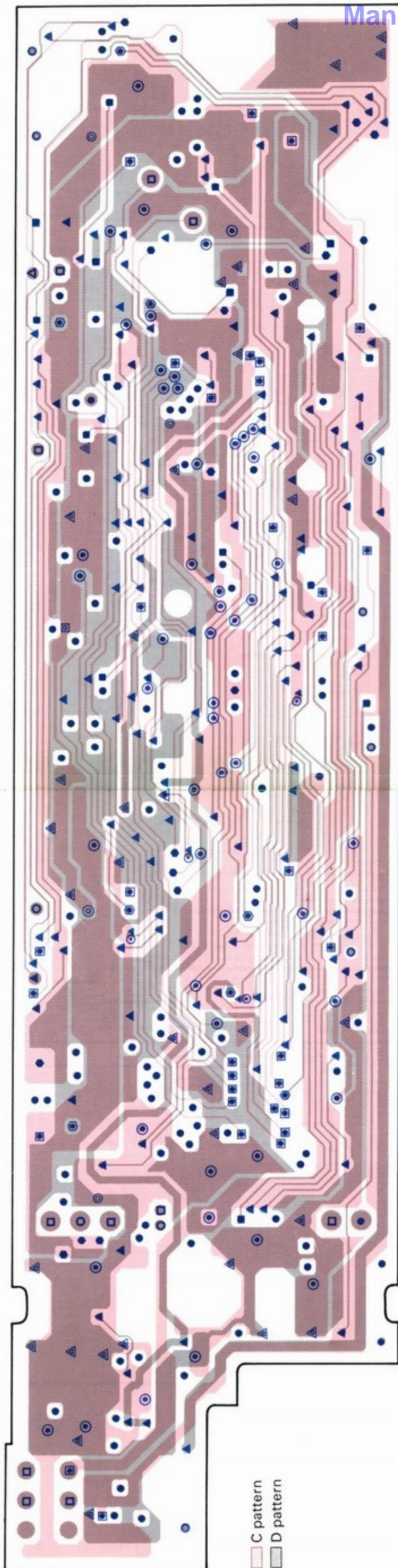
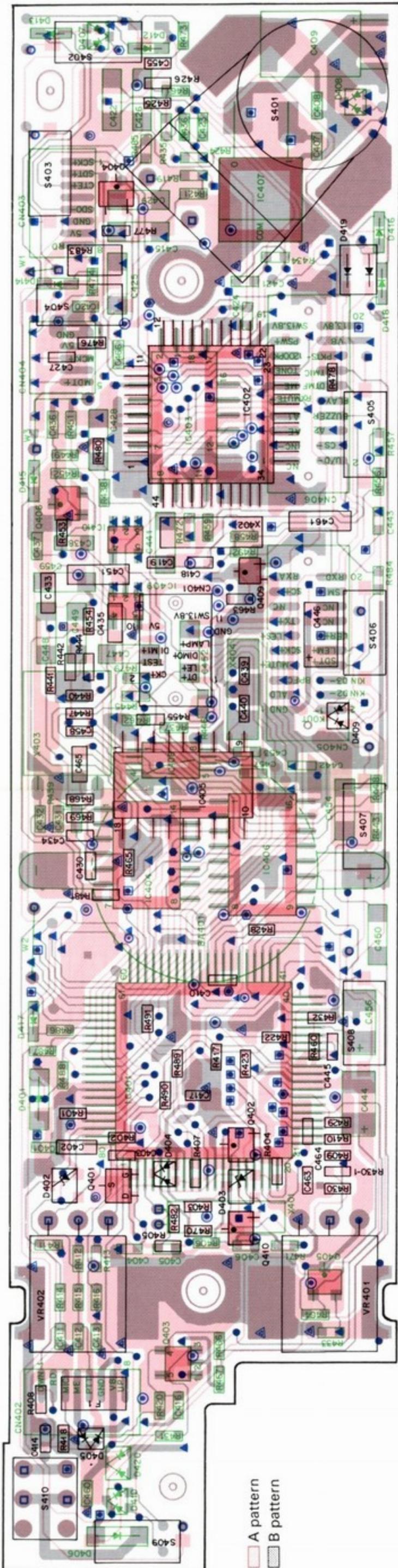
CONTROL UNIT (W02-18XX-08) 1852 : K,P 1853 : M 1854 : M2 1855 : E,E3,E9 1856 : E2
 Component side view



- A and B connected
 - A only
 - ⊙ A and C connected
 - B only
 - ⊙ A and D connected
 - △ C only
 - ⊙ B and C connected
 - B, C and D connected
 - ▲ A, B, C and D connected
 - △ C and D connected
- No mark is not connected

PC BOARD VIEWS TM-451A/E

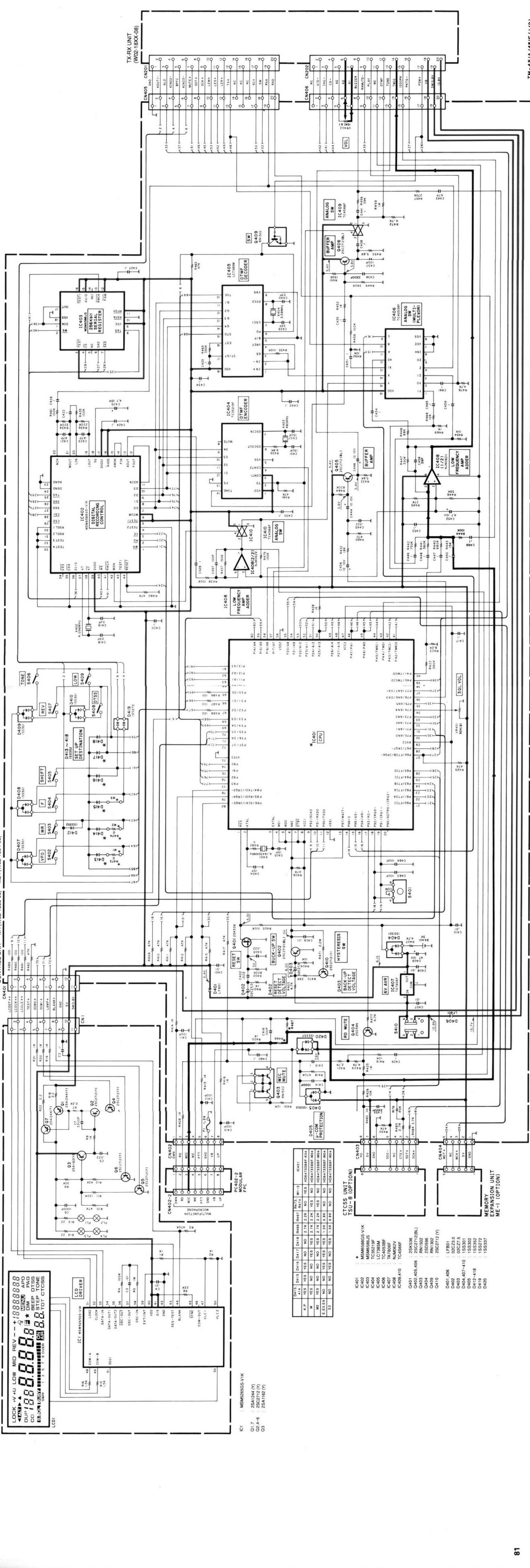
CONTROL UNIT (W02-18XX-08) 1852 : K,P 1853 : M 1854 : M2 1855 : E,E3,E9 1856 : E2
Foil side view



- 25C2712
- 25D596
- RN1302
- 2SK536
- RN1502
- TC4566F
- NUM062V
- TC35219F
- TC4053BF
- LC7385M
- MSM6586JS
- MSM6588GS-VIK
- HD6473388F
- TA7806F

TM-451A/E SCHEMATIC DIAGRAM

LCD ASSY (B38-0721-08) K.P. : (W02-1852-08) E.E3.E9 : (W02-1855-08) E2 : (W02-1856-08)
 CONTROL UNIT M : (W02-1853-08) M2 : (W02-1854-08)



IC1 : MSM526GS-V1K
 Q1,7 : 2SA1244 (Y)
 Q2,4-6 : 2SC2712 (Y)
 Q3 : 2SA1182 (Y)

IC401	IC402	IC403	IC404	IC405	IC406	IC407	IC408	IC409	IC410
MSM526GS-V1K									
MSM526GS-V1K									
MSM526GS-V1K									

Q1,7	Q2,4-6	Q3
2SA1244 (Y)	2SC2712 (Y)	2SA1182 (Y)
2SA1244 (Y)	2SC2712 (Y)	2SA1182 (Y)
2SA1244 (Y)	2SC2712 (Y)	2SA1182 (Y)
2SA1244 (Y)	2SC2712 (Y)	2SA1182 (Y)

D413	D415	D416	D417	D418	D419	D420
YES	NO	NO	NO	NO	NO	NO
NO						
NO						
NO						

IC401	IC402	IC403	IC404	IC405	IC406	IC407	IC408	IC409	IC410
MSM526GS-V1K									
MSM526GS-V1K									
MSM526GS-V1K									
MSM526GS-V1K									

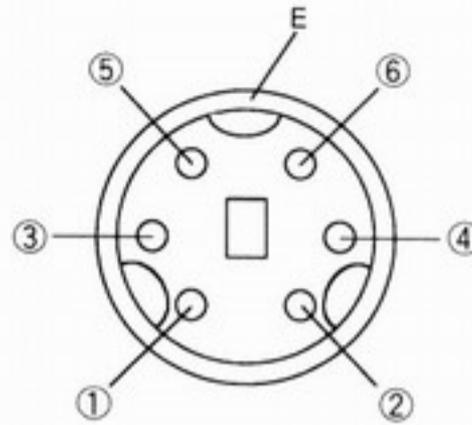
D401	D402	D403	D404	D405	D406	D407	D408	D409	D410
YES	NO								
NO									
NO									
NO									

PG-5A (DATA CABLE)

PG-5A External View



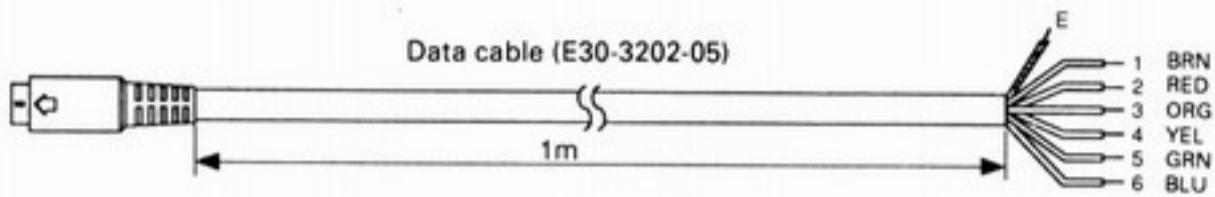
PG-5A Wiring



Pin No.	Wire color
1	Braun
2	Red
3	Orange
4	Yellow
5	Green
6	Blue
E	Shield

Plug (6P mini DIN)

PG-5A Dimension



SPECIFICATIONS

General

Frequency range	
Main band	438.000~449.995MHz : K,P 430.000~439.995MHz : M,M2,E,E2,E3,E9
Sub band (receive)	144.000~147.995MHz : K,P,M,M2 144.000~145.995MHz : E,E2,E3,E9
Mode	F3E
Antenna impedance	50Ω
Usable temperature range	-20°C~+60°C
Power supply	DC 13.8V ± 15% (11.7~15.8V)
Grounding method	Negative ground
Current	
Transmit (max.)	10.0A or less
Receive (no signal)	0.6A or less
Frequency stability	
Main band	Within ±10ppm
Sub band (receive)	Within ±10ppm
Dimensions (W x H x D) Projections not included	140 x 40 x 160mm
Weight	1 kg

Transmitter

Power output	
High	35W
Mid	Approx. 10W
Low	Approx. 5W
Modulation	Reactance
Spurious emissions	-60dB or less
Maximum frequency deviation	±5kHz
Audio distortion (at 60% modulation)	3% or less
Microphone impedance	600Ω

Receiver

Circuitry	Double conversion superheterodyne
Intermediate frequency (1st/2nd)	45.05MHz/455kHz
Sensitivity (12dB SINAD)	0.16μV or less
Selectivity	
-6dB	12kHz or more
-60dB	28kHz or less
Squelch sensitivity	0.1μV or less
Audio output (8Ω, 5% distortion)	2W or higher
Audio output impedance	8Ω

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