



Service Manual

AUDIO ANALYZER

UPD

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Chapter 6

Maintenance

6.1 Functional Description

This chapter gives an overview of the interaction between the different boards when executing a certain measurement or signal generation. The boards are discussed in detail in chapter 7.

6.1.1 Analog Measurements

6.1.1.1 Differences between the Various Analyzers

The UPD includes 3 analog instruments: ANLG 22 kHz, ANLG 100 kHz and ANLG 300 kHz. The frequency values indicate the specified analog test band limits.

1. ANLG 22 kHz

Depending on the magnitude of the test signals, the range is selected in the input section of the test channels either manually or fully automatically:

- Range 30 mV to 30 V with balanced test input
- Range 30 mV to 300 V with unbalanced test input

Following analog signal conditioning using an audio A/D converter, the data are acquired at a sampling rate of 3.072 MHz. To avoid aliasing problems, a 2nd-order analog lowpass filter connected ahead of the A/D converter is used in conjunction with the steep-edged digital lowpass incorporated in the converter. In the A/D converter, data reduction to the true output rate of 48 kHz is at the same time accomplished via the digital lowpass. The A/D converter operates according to the delta-sigma principle with a resulting resolution of 19 bits. The digital data stream is serially read into the DSP for further digital signal processing (data limit is 64 bits for each conversion cycle).

(see circuit diagrams Analog Analyzer 1030.9102.01S and ADC Board 1030.9260.01S)

2. ANLG 100 kHz

Analog signal conditioning as with instrument ANLG 22 kHz, however, for signals below 10 mV, a 30-dB post-amplifier is used in the ADC board to compensate for the lower resolution of the A/D converter. The different ranges are extended down to 1 mV to obtain higher sensitivity.

The data are acquired after analog signal conditioning with a high-speed A/D converter at a sampling rate of 341.33 kHz. A steep-edged 7th-order analog lowpass filter connected ahead of the A/D converter is used to avoid aliasing problems.

The converter operates according to the principle of a combination of flash converter and 2-stage comparison with internal fault correction and contains a S&H amplifier. It achieves a resolution of 12 bits. The digital data stream is read into the DSP in parallel mode according to the sampling rate for further digital signal processing.

(see circuit diagram ADC Board 1030.9260.01S)

3. ANLG 300 kHz

As with instrument ANLG 100 kHz with the same high-speed A/D converter, however, with a sampling rate of 1024 MHz and a steep-edged analog aliasing lowpass filter of 7th order complying with the larger test bandwidth and sampling rate.

(see circuit diagram ADC board 1030.9260.01S)

In the basic UPD model, the conditioned analog signals of both test channels are alternately recorded by only one ADC board and further processed in the DSP (Digital Analyzer 1).

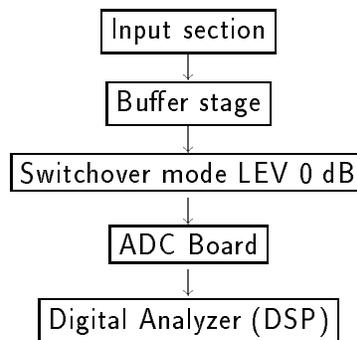
Using the Option UPD-B3 Highspeed, both test channels are simultaneously measured via their own ADC board and their digital signals also further processed simultaneously via a second DSP board (Digital Analyzer 2). (see section 6.1.2.3, page 6.10 and circuit diagram 1030.7500.01S sheets 2 and 3)

For differences in signal processing with the various analyzer models in the DSP see digital measurements, page 6.9.

6.1.1.2 Measurement of: Level, FFT, DFD-d3, DIM, Wow & Flutter

After selecting the appropriate range for the test signal, the analog signals are band-limited by analog aliasing filters and an additional digital filter in the audio ADC in the case of ANLG 22 kHz (see circuit diagram ADC Board 1030.9260.01S). Further processing in the modes of measurement mentioned is performed by direct digital signal processing in the DSP after A/D conversion (see section 6.1.2.1, page 6.7).

Signal flow:



6.1.1.3 Measurement of: THD, THD+N, MODDIST

- THD, THD+N:

First cycle similar to level measurement, with the rms value and, at the same time, the distortion factors as well as the fundamental frequency of the signal to be weighted being determined in the DSP.

Signal flow of first cycle: as with level measurement (see section 6.1.1.2, page 6.2)

Depending on the measurement result of the first cycle, two cases are distinguished:

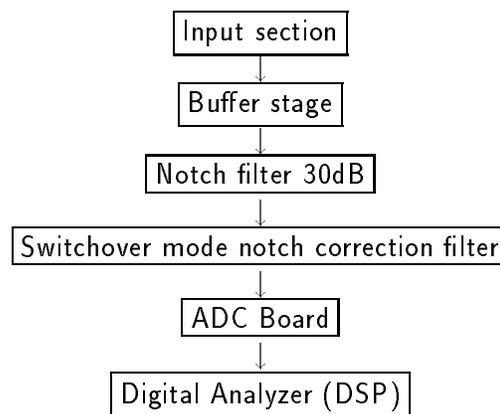
- THD, THD+N is worse than -60 dB or ≥ 0.1 % with ANLG 22 kHz, (-50 dB or ≥ 0.316 % with ANLG 100/300 kHz):

In this case, the measurement is finished, the measured value is output.

- THD, THD+N is better than -60 dB or < 0.1 % with ANLG 22 kHz, (-50 dB or < 0.316 % with ANLG 100/300 kHz):

In this case, a second cycle is automatically performed with an analog notch filter selected, which is set to the fundamental frequency with a post-amplification of 30 dB. In the processed signal, the fundamental is equal to or smaller than that of the original signal, however, the harmonic distortions and noise are amplified by 30 dB.

Signal flow of second cycle:



Result of second cycle:

The DSP again determines the distortion factors from the analog-weighted signal. In this case, THD, THD+N are output as measured value, a different range being selected due to the post-amplification of 30 dB.

- **MODDIST:**

A first cycle is performed, in which the DSP determines the levels and frequencies of the interfering AF carrier and the higher-frequency carrier and, simultaneously, the intermodulation factor of the signal to be weighted.

Signal flow of first cycle: as with level measurement (see section 6.1.1.2, page 6.2)

Depending on the measurement result of the first cycle, two cases are distinguished:

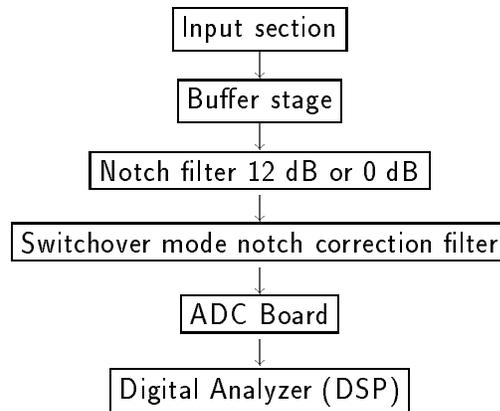
- MODDIST is worse than -55 dB or ≥ 0.18 % with ANLG 22 kHz, (-40 dB or ≥ 1 % with ANLG 100/300 kHz):

In this case, the measurement is finished and the measured value output.

- MODDIST is better than -55 dB or < 0.18 % with ANLG 22 kHz, (-40 dB or < 1 % with ANLG 100/300 kHz):

In this case, a second cycle is automatically performed with the analog notch filter selected, which is set to the AF interfering frequency and a post-amplification of 12 dB or 0 dB, depending on the ratio between interfering level and RF level. In the processed signal, the interfering level of the intermodulation signal is smaller than that of the original signal, the modulated RF carrier, however, is amplified by max. 12 dB (for level ratios of 4:1).

Signal flow of second cycle:



Result of second cycle:

The DSP again determines the intermodulation factor from the analog-weighted signal. The MODDIST value is output as measured value.

6.1.1.4 Measurement of: DFD-d2

A first cycle is performed, the DSP determining the levels and frequencies of the two differential-tone carriers of the signal to be weighted.

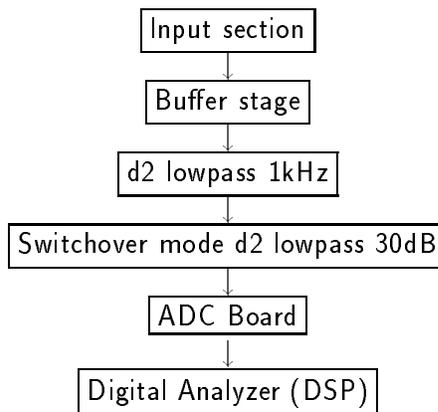
Signal flow of first cycle: as with level measurement (see section 6.1.1.2, page 6.2)

Depending on the measurement result of the first cycle, the following cases are distinguished:

- DFD-d2 is worse than -60 dB or $\geq 0.1\%$:
In this case, the measurement is finished and the measured value output.
- DFD-d2 is better than -70 dB or $< 0.0316\%$ with ANLG 22 kHz, (-50 dB or $< 0.316\%$ with ANLG 100/300 kHz):

In this case, a second cycle is automatically performed with a d2 1-kHz lowpass filter selected and with a post-amplification of 30 dB. In the processed signal, the differential-tone carriers are equal to or smaller than those of the original signal, the 2nd-order differential tone and other noise, however, are amplified by 30 dB.

Signal flow of second cycle:



Result of second cycle:

The DSP again determines the intermodulation distortion from the analog-weighted signal. In this case, DFD-d2 is output as measured value, a different range being selected due to the analog post-amplification of 30 dB.

6.1.1.5 Measurement of: Frequency and Phase

- Signal processing in Analog Analyzer 1/2:

After passing the input section with range selection, the test signals are taken via a differential amplifier (N410, test point P400.1, FRQIN) to the stage Freq Comparator.

Following a lowpass with a 3-dB cutoff frequency of 500 kHz, level threshold values are generated using detectors for +PK and -PK and applied to analog comparators. Two flip-flop stages subsequently generate pulse control signals for the digital frequency counter PFC.

The circuit parts involved are applied to the potential of the floating analog ground of the respective analog test channel. Further processing of the control signals for frequency measurement (FMESS) and phase measurement (PHMESS) is accomplished after conversion to the reference potential of the chassis using optocouplers (U465-A,B). (see circuit diagram Analog Analyzer 1030.9102.01S sheets 1 to 5)

- Single or two-channel frequency measurement:

After conditioning and conversion into digital control signals, the test signals are taken from the analog analyzers to the multiplexer (D510) of the phase comparison logic in the Analog Motherboard. The signals required for frequency measurement are passed on to cable connector W31 (FAMESS → f-measurement Ch 1, FBMESS → f-measurement Ch 2) and to the frequency counter logic in Digital Analyzer 1 (see circuit diagram Analog Motherboard 1030.9060.01S sheet 1, 5).

The measuring clock pulses of the two channels are applied to the counter gate array PFC and are simultaneously processed in a programmed cycle (two-channel counter A and B).

The principle of measurement is based on a combined procedure of frequency/gate time and period. To this end, the counting chains are activated with the rising edge of the test signal after the measurement has been started and are opened for a predefined minimum gate time. After this gate time has expired, the next rising edge of the test signal closes the respective counter gate. With the measuring counting chains, a reference counting chain is activated at the same time in the PFC, counting reference clocks with 10 MHz.

The AT computer controls the operation of the PFC. After successful status poll of the end of measurement, it reads in the counting registers for calculation of the test frequency.

(see circuit diagram Digital Analyzer 1030.8506.01S)

- Combined frequency/phase measurement:

The phase measurement hardware is configured such that frequency and phase are always measured at the same time with the function PHASE.

In the analog channel 1, the frequency is evaluated via the PFC-counter (A) (function as with pure frequency measurement).

At the same time, counter (A) controls the gate of counter (B) using the Ready Out signal, the phase signals provided by the phase comparator logic of the analog motherboard being measured by Analyzer 2 with respect to Analyzer 1. Phase counter (B) is always activated as long as frequency counter (A). To this end, phase counter (B) is configured such that its two counting chains Mescount as well as Refcount are activated at the same time. Mescount B counts an exclusive-OR signal clocked with $f_{ref} = 10$ MHz from channels 2-1, allowing to make a decision on the optimum hardware setting for the phase position (control line PSEL-180/0). Parallel to this, Refcount B counts the phase difference signal proper from

channels 2-1, which is also clocked with 10 MHz via a JK flip-flop (from board ID 06 on: D flip-flop).

Function of the four pulse signals from the two Analog Analyzers at MUX D510 and processing in the phase comparator logic in the Analog Motherboard:

Control line		Function
PSEL-180/0	PSEL-R/F	Phase comparison: Edge Channel
0	0	Rising Ch 1 - Rising Ch 2
1	0	Rising Ch 1 - Falling Ch 2
0	1	Falling Ch 1 - Falling Ch 2
1	1	Falling Ch 1 - Rising Ch 2

The phase comparison of the two analog channels is performed in two cycles with the rising and falling signal edge of reference channel Ch1 in order to eliminate phase measuring errors due to signal asymmetries and DC offset. Switchover is accomplished via the control line PSEL-R/F from the AT-SERPA of Digital Analyzer 1.

Function description of the phase comparison logic on the Analog Motherboard:

The phase comparison pulses from phase comparator D501-PC03 are first read into D flip-flop D505 using the clock signal 6.144 MHz, which is frequency-modulated with a triangular signal of about 90 Hz. The phase test signal is then applied to the output PHASB of D505 with a triangular time jitter of 90 Hz.

The jitter of the phase signal is required for test frequencies the period of which forms an integral ratio to that of the PFC reference clock. In such cases, a beat and thus a larger error in measurement would be obtained.

The counting error is eliminated by integration of the phase signal with triangular jitter over many measuring periods, in particular in the upper frequency range of the UPD.

Digital Analyzer 1 reads in the signal PHASB via a JK flip-flop (resp. D flip-flop) with the 10-MHz reference clock. Synchronously with the clock of the test frequency, these reference clock pulses are taken to a counting chain of the counter gate array PFC with a predefined gate time. After the gate time has expired, this counter result divided by the reference clock counter result constitutes a direct measure of the phase difference between the two channels. With the mode of measurement Kombi, this preselected gate time corresponds to a minimum gate time (see frequency measurement). Because of 2 partial cycles, this corresponds to half the predefined value.

The AT computer reads the counting registers of the PFC for each partial cycle - rising or falling edge of the reference signal Ch1- and calculates the frequency and the phase after averaging.

(see circuit diagrams as with frequency measurement)

6.1.1.6 Measurement of: DC

- Conditioning in Analog Analyzer 1/2:

After passing the DC-coupled input section with range selection, the test voltage is taken via a differential amplifier (N410, test point P400.1, FRQIN) to a voltage/frequency converter (DC/f converter D470). Because of its unipolar way of operation, a positive reference voltage is superimposed at the input on the DC/f converter for the bipolar DC measurement (via V467, $V_{ref} = +2.5V$). From the DC voltage at the input, the converter provides a frequency-proportional squarewave signal DCF at the output.

Nominal values for DC/f conversion:

DC test voltage	Frequency
Min. range value	5 kHz
Zero	10 kHz
Max. range value	15 kHz

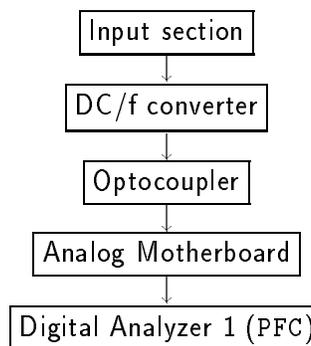
The circuit parts involved are applied to the potential of the floating ground of the respective analog test channel. With function DC, the control line SEL FRQ/DC switches the squarewave signal DCF of the DC/f converter via optocoupler U465-B to the same signal path as with frequency measurement (see section 6.1.1.5, page 6.5).

- Processing via frequency counter PFC in Digital Analyzer 1:

The DC input voltages of both test channels are taken as frequency-proportional squarewave signals to gate array PFC and are processed simultaneously in counter channels A and B.

As in the case of frequency measurement, the AT computer controls the procedure and calculates the DC measurement results from the DC/f conversion.

- Signal flow:



6.1.2 Digital Measurements

6.1.2.1 Booting the DSPs

After starting the instrument software, the following procedures are performed by the software:

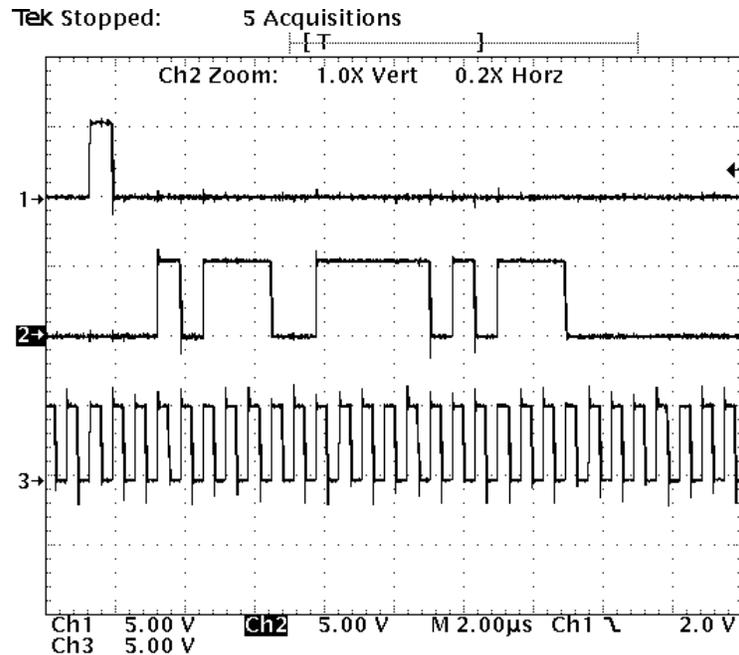
- The respective DSP ¹ is located; the boards (and thus the DSPs) are identified as follows:
 - ANALYZER, DSP A
The Digital Analyzer Board is searched for either at address 290H or 390H (default). This is done by reading out an identification register (device D25, address 02B92H), where either 4 or 5 (depending on the hardware version) must be read out. If the board is not found, the error message Digital Analyzer not found is output.
 - ANALYZER II (Option Highspeed), DSP B
The second Digital Analyzer Board is connected to the first one via a 50-contact flat cable. Line BDR0 is pulled to logic 0 via a resistor. (→ Register 2B90H, bit 5 must be 0 when it is read in). If the board is not found, the message Highspeed -NA- is output on the OPTION panel.

¹Digital Signal Processor, in the UPD TMS320C30

- GENERATOR, DSP G
The Digital Generator Board is searched for either at address 290H or 390H (default). This is done by reading out an identification register (device D25, address 0AB92H), where either 82 or 83 (depending on the hardware version) must be read out. If the board is not found, the error message Digital Generator not found is output.
- AES/EBU (Option), DSP D
The option AES/EBU is connected to the Digital Generator via a 40-contact flat cable. The line DDR0 is pulled to logic 0 via a resistor. Register AB90H, bit 5 must be 0 when it is read in. If the board is not found, the message AES/EBU -NA- is output on the OPTION panel.
- The respective DSP is booted. The ROM in the DSP contains a program that searches for a reserved word (0ABACABH) at the DSP address 200000H (Primary Bus). If it is found, the ROM code assumes that a useful program is loaded and executes it. If it is not found, the ROM code enters the operating status *RS232 boot*.

Booting:

- Activation and deactivation of RESET: (DSP A: D612, pin 13; DSP B: D612, pin 12; DSP G: D612, pin 13; DSP D: D612, pin 12;).
- Waiting for a response of the DSP operating system. If this response is not given within 10 ms, the RS232 boot is performed.
- Setting of line HOLD (D613, pin 13 or pin 12) to 0. As a result of this, address 2000000H can no longer be accessed by the DSP, which will then enter RS232 mode following reset. (HOLD is not activated by the AT in the case of DSP G and DSP D, it is assumed that memory location 200000H is deleted after switch-on).
- Switchover of the serial lines to RS232 operation.
- Activation and deactivation of RESET. The DSP starts up and switches to serial boot mode.
- Setting of line HOLD (D613, pin 13 or pin 12) to 1, so that the bus can again be accessed by the DSP.
- Serial transfer of the DSP operating system (DUMP.OUT); reception at pin 92 XF0 on the DSP.
- Further reset. If the DSP does not register now, the error message Can't boot DSP . . is output.
- After booting of the DSP operating system, the respective application software is loaded. This is done in high-speed serial mode with the 3 lines Data, Clock and Framesync. 32 bits are transferred per frame. The following chart shows Framesync (FSX) in trace 1, Data in trace 2 (MSB first) and the associated clock in trace 3.



The file ANAIN.OUT and an overlay required for the respective test function are transferred to the digital analyzers.

The file GENOUT.OUT is transferred to the digital generator.

The file AES.OUT is transferred to the option AES/EBU.

- Within this application software, the respective test function or generator waveform is selected and executed by means of an interrupt or by polling with the selected input or output.
- During all the interactions with the DSP, the AT remains in normal polling mode. Exception: Picture data and FFT result vectors are transferred by means of a DMA transfer (2 16-bit transmissions per serial transfer closely following each other).

6.1.2.2 Differences between the Various Analyzers

In the UPD, 3 digital analyzer models are implemented by the software: DIG 48 kHz, DIG 192 kHz and DIG 768 kHz, the frequency indicating the maximum sampling rate.

1. DIG 48 kHz

With this model, the measurements RMS, QUASI-PEAK, PEAK, WOW & FLUTTER are performed *online*, i.e. signal processing is carried out during signal acquisition. The signal acquisition is triggered by one interrupt for each sample. Unless the measurement is aborted (e.g. because of two-channel multiplexing without the Option UPD-B3 (Highspeed) or because of a sweep) repeated measurements are performed without interruption of the signal flow.

The measurements requiring time-consuming postprocessing (THD, THD+N, FFT, SMPTE, DFD, POSTFFT) acquire the input signal and subsequently process the data. Thus time intervals are produced during which the signal interrupts, for instance, are no longer processed. Repeated measurements restart interrupt processing.

2. DIG 192 kHz

With this model, all measurements are performed *offline*, i.e. signal processing is performed after signal acquisition. To this end, a sufficient number of samples is loaded into the internal memory. The measurement routines are then addressed from this memory instead of from the port. Signal acquisition into the memory is performed in polling mode, the sampled data are stored in the memory area starting at 408000H.

3. DIG 768 kHz

Same as DIG 192 kHz, however, the number of samples to be acquired is calculated with a higher minimum frequency.

6.1.2.3 Differences with the Option UPD-B3, Highspeed installed

The Option UPD-B3 consists of a further DSP board (Digital Analyzer) for signal analysis and a second ADC board. With this option, all signal paths are provided separately for each channel. In this case, simultaneous measurement on both channels is performed without switching over the input signal after a measurement result.

The second DSP board is connected to the digital analyzer via a 50-contact flat cable. Though inserted in the digital motherboard, it does **not** evaluate bus signals there. The control is performed via the SERPA on the Digital Analyzer of the basic instrument.

The additional DSP board is a different version (04) of the analyzer of the basic instrument. The bus interface devices, the PFC for frequency measurement and the crystals for clock generation are not fitted. In the case of version 04, control lines for the second DSP board (with the ending ..B) are short-circuited via 0- Ω resistors with the *normal* control lines (with the ending ..A).

6.1.2.4 Measurement with Parallel Port, Serial Port

For measuring digitalized audio signals, both a universal serial interface and a parallel interface are available.

1. Parallel port

The input signal is applied on the rear panel (37-contact DSUB connector) via an ESD protection circuit (220- Ω and diodes against +5V or ground) to the input latch.

The data are read into the input latch with a clock signal the polarity of which can be switched over with STRBP0LA or STRBP0LB and an exclusive OR (D64-A). At the same time, this clock signal is used to write a 1 into flip-flop D55-B. The output generates an interrupt on the DSP (INT2).

The DSP then picks up the received word at the port (ECSEXT = low), clearing the generated interrupt.

2. Serial port

The input signal is taken from the front panel (15-contact DSUB connector) via a 16-contact flat cable to the Digital Analyzer. There, the signals are applied to input buffer D42 after passing an ESD protection circuit (220- Ω and diodes against +5 V or ground).

Multiplexer D48 selects a channel (A or B) and connects it to serial input 1 of the SERPA.

The SERPA provides the clock signal SLROUT on the serial interface.

Both the serial connector and the parallel connector provide +5V with approx. 50 mA produced by a series regulator (D620) from the +12 V of the digital power supply unit.

6.1.2.5 Measurement with Internal Digital Connection

The input signal is transferred from the generator to the analyzer via the DSPLINK (16-contact flat cable). For this purpose, the input multiplexer must be set to G (=3). The data are directly taken to the serial interface 1 of the DSP. The sampling rate is permanently set to 43619.792 Hz in this mode of measurement. The measurement is only intended for demonstration purposes and is therefore only possible as a single-channel measurement.

6.1.3 Measurement with AES/EBU, S/P DIF, OPTICAL Interface

- AES-EBU: The input signal is taken from the connector via the Adapter Board and the 10-contact flat cable to the module UPD-B2 (AES-EBU), connector X51.
- S/P DIF: The input signal is taken directly from the front panel via a coaxial cable to the module UPD-B2 (AES-EBU), connector X510 (top).
- OPTICAL: The input signal is taken from the connector via the Adapter Board and a 10-contact flat cable to the module UPD-B2 (AES-EBU).

On module AES/EBU, the input samples are conditioned and applied to a multiplexer selecting the input.

This is followed by clock conditioning, the reconditioned clock being used to read the signal into the SERPA on the AES/EBU.

The reconditioned clock is made available to the generator after conditioning by a PLL and to the frequency counter PFC on the digital analyzer via the line CLOCKDI. Thus the applied clock rate can be measured.

On reception of a preamble (identified by the same level on line AES-DRO for three clocks), the SERPA sends an interrupt (INTO) to the DSP, which fetches the sample from the port, cuts off the report and transmits the audio section via the internal link (lines TXDD, FSXD, CLKXD) to the analyzer(s). 32-bit transmission is used, the LSB (i.e. bit 0) identifying the channel. The transfer via the internal link is not exactly equidistant but corresponds to twice the sampling rate (because stereo signal) on average only.

The link leads from the Option AES/EBU to the Digital Generator (40-contact flat cable), is through-connected and taken to the Digital Analyzer via the 16-contact flat cable.

There, the signal is applied to the serial input 1 of the DSP via the input multiplexer and processed *online* (since AES/EBU can only be used with 48 kHz).

The same INTO occurs when the option transmits data; the differentiation is made in the interrupt service routine. (see Generator, page 6.14).

6.1.4 Analog Signal Generation

In its basic version, the Analog Generator consists of the two modules DAC Board and Output Circuit. This basic version is referred to as universal generator.

- DAC Board:
 - Signal generation with D/A converter and lowpass filter
 - Squarewave generation
- Output Circuit:
 - Level setting
 - Balanced and unbalanced output stage
 - Channel switchover
 - Impedances

With Option UPD-B1 Low Distortion Generator installed:

- SINE, MODDIST and DFD with better signal-to-noise ratio
- DIM signal can be generated

6.1.4.1 Signal Generation without Low Distortion Generator

On the DAC Board, all signals (except for the squarewave signal) are generated by a 20-bit D/A converter which is controlled by the Digital Generator via a serial interface. A steep-edged lowpass filter is used to suppress the converter clock. The squarewave signal is generated from the sinewave signal using a comparator circuit.

At the input of the Output Circuit (ahead of the LEVEL CONTROL circuit), all the signals are set such that they feature the same peak value of $\approx 3.54V$ ($\hat{=} 2.5V_{rms}$ with sinewave).

Exception: The squarewave signal is set to $V_{peak} \approx 2.65V$ (even with DIM signal).

On the Output Circuit, further level setting of the signal as well as generation of the balanced output signal by two output amplifiers and channel switchover with different impedances are performed.

6.1.4.2 Signal Generation with Low Distortion Generator

(The Low Distortion Generator module is abbreviated by Low Dist Gen or LDG in the following)

The Low Distortion Generator is an RC oscillator generating a low-noise and low-distortion sinewave signal in the frequency range 10 Hz to 110 kHz with constant level $V_{rms} \approx 2.70V$.

It can be activated with the signals SINE, MODDIST and DFD. The generation of a DIM signal is only possible with the option installed.

The single components of the two-tone signals MODDIST, DFD and DIM are set on the modules generating the signals and with the circuit SIGNAL ADDER on the Output Circuit such that, ahead of the LEVEL CONTROL circuit, they feature the same peak value of $V_{peak} \approx 3.54V$ as with signal generation without Low Distortion Generator. The squarewave for the DIM signal is set to $V_{peak} \approx 2.65V$.

On the Output Circuit, further level setting of the signal as well as generation of the balanced output signal by two output amplifiers and channel switchover with different impedances are performed (as with signal generation without Low Dist Gen).

1. SINE

Instead of the signal from the DAC board, the signal from the Low Distortion Generator is fed into the LEVEL CONTROL circuit on the Output Circuit.

2. MODDIST

The sinewave signal from the DAC board passes a lowpass filter in order to improve the signal-to-noise ratio in the vicinity of the higher-frequency signal coming from the Low Dist Gen.

Signal from	Frequency range	Filter	Level set in	Signal Adder
Dac Board	30Hz ... 500Hz	LP SMPTE	SIGNAL DAC	0dB
Low Dist	4kHz ... 110kHz	—	IMD ATTEN	-6dB

The level setting in the SIGNAL DAC and IMD ATTEN depends on the ratio $V_{01t} LF:HF$ between lower-frequency and higher-frequency signal set in the panel.

3. DFD

The sinewave signal from the DAC board passes a highpass filter in order to improve the signal-to noise ratio with DFD d2. The Low Dist Gen provides the higher-frequency signal.

Signal from	Frequency range	Filter	Level set in	Signal Adder
Dac Board	5kHz ... 110kHz	HP DIFF	—	-6dB
Low Dist	5kHz ... 110kHz	—	IMD ATTEN	-6dB

The two single signals have the same value, the level in the IMD ATTEN is therefore ≈ 0 dB. The difference between the two frequencies is 80 Hz to 1 kHz.

4. DIM

The DAC Board provides a squarewave signal with the standard band limiting of 30 kHz or 100 kHz (LP DIM), the LDG provides the higher-frequency sinewave signal.

Signal from	Frequency range	Filter	Level set in	Signal Adder
Dac Board	2.96kHz / 3.15kHz	LP DIM	—	0dB
Low Dist	14kHz / 15kHz	—	IMD ATTEN	-6dB

The amplitude ratio between squarewave and sinewave signal is permanently set to 4:1 according to the standard. The level in IMD ATTEN is ≈ -9.2 dB.

6.1.5 Digital Signal Generation

After starting the UPD software, the DSP of the generator is booted, see section 6.1.2.1, page 6.7.

6.1.5.1 Signal Generation on Parallel Port, Serial Port

1. Parallel

The parallel audio signal is output on the rear panel via a 37-contact DSUB connector. The clock used can be provided either by the UPD (in this case ENA_EXCLK is high, page 4) or fed in externally via the line EXSTRBIN.

The internal clock signal FSX is generated by SERPA and output as STROBE_OUT via a delay line.

The signal comes from the DSP via the expansion bus and a two-stage latch to the interface; interrupt 2 is used.

2. Serial

The audio signal on the universal serial interface is output by the DSP via the SERPA. The signal is resynchronized using a latch. The clock of this latch (D43) is either internal (ENA_EXCLK = high) or external (input SCLKIN). Data, clock and a frame signal are output, the latter being either pulsed (FRAMEWS = high) or a symmetrical squarewave in the case of a multiplexed signal (FRAMEWS = low).

The bit clock polarity is switched over with the same multiplexer as the frame output.

The SERPA is supplied with 3 input crystals which are split up in the SERPA for generation of the desired output clock rate and switched to the output.

After the ESD protection circuit, the output signal is taken via a 16-contact flat cable to the front panel (15-contact DSUB connector).

Both the serial and the parallel connector provide +5 V with approx. 50 mA, generated from the +12 V of the digital power supply unit using a series regulator (D610).

6.1.5.2 Signal Generation on Internal Interface

For testing purposes, the generated signal can also be sent on the internal DSP link from the Digital Generator to the Digital Analyzer. The sampling rate is permanently set, and only one channel is possible (see page 6.11).

The signal output by the DSP on the serial interface 1 (of the DSP) is amplified by driver D614 and applied to the internal DSP link that connects all DSPs to one another. This link is also used with AES/EBU and S/P DIF.

6.1.5.3 Signal Generation on Interfaces AES/EBU, S/P DIF, OPTICAL

The output signal calculated on the Digital Generator (including rounding to the desired audio bits) is transmitted via the internal link (lines TXDG, FSXG, CLKXG) to the Option UPD-B2 AES/EBU. There, the report is added and the signal output via the SERPA. Depending on the output selected, the signal is taken to the front panel:

- OPTICAL: from SERPA via a driver (D100-B, switched by LS7) and a 10-contact flat cable to the Adapter Board, where the optical transmitter is located (system TOSLINK).

- AES/EBU: from SERPA via a multiplying D/A converter of discrete design to the output level setting with subsequent power amplifier. For potential isolation, its output is applied via a converter and switched to the appropriate output (X511) via a relay (nominal impedance: 110 Ω). From there, it is directly taken to the output socket via a shielded round conductor.
- S/P DIF: same as AES/EBU, however different relay position and nominal impedance: 75 Ω , the output socket is directly connected to the option (connector X512).

The output clock can be derived either by division of the crystal frequencies provided by the generator, from the analyzer input signal or from the externally applied clock frequency.

For this purpose, a PLL (D112) is used, the setpoint and feedback loop of which are selected with multiplexer D111 according to the clock source used.

To adapt to different sampling rates the Option AES/EBU and the Digital Generator are coupled only loosely. The option sends a query (by applying SNYC to LOW level), causing the generator to transfer 64 samples block by block. After transmission of a few samples, the query is cleared and only sent again on the next request.

The data are transferred internally by two-channel multiplexing, the LSB selecting the channel. The bit rate is 4 MBaud = 131k words/s.

6.1.6 Controller

A personal computer compatible with industrial standard is used as controller. This computer consists of the following boards:

- 386SX Mainboard, 20MHz, Coprocessor 80SX387, with AMI-BIOS
- IDE-Combicontroller with 1 parallel and 2 serial interfaces as well as 1 gameport (which is not connected in the UPD, however).
- 3.5 " Floppy disk drive, 1.44 MB (Drive A:)
- 3.5 " Hard disk, capacity 40 MB or 120 MB (Drive C:)
- VGA controller for simultaneous operation of LCD and external VGA monitor, resolution 640*480 pixels
- LCD 9.4 ", monochrome, with backlighting and high-voltage converter (can be switched off with PERIF, see page 7.241)
- optional: IEC-bus card

6.1.7 Additional Boards

The current supply of the digital section is implemented via a Connector Board, where the individual modules (floppy, hard disk, blower, high-voltage converter) are connected. The Digital Motherboard is directly supplied by the power supply.

Brightness and contrast control is connected from the front panel to the high-voltage converter or the LCD via the Connector Board.

The blower of the UPD is thermostat-controlled, the temperature sensor being located on the Connector Board. Operating voltage of the blower: 12 volts, from the digital power supply.

The front panel keyboard with the rotary knob is connected via a flat cable to the Connector Board and further to the Digital Generator module. The Digital Generator accommodates the gate array

PERIF for keyboard control. Like keystrokes on the external keyboard, keystrokes on the front panel are entered into the BIOS buffer by an interrupt routine.

The PERIF does not poll the keyboard continuously, but becomes only active on actuation of a key. The LEDs on the front panel (next to the keyboard) are controlled by the parallel outputs of the PERIF.

The LED indicating the front panel accesses (via the floppy disk) is addressed via a two-wire cable by the combicontroller.

Backlighting of the LCD is operated by a high-voltage converter mounted behind the LCD. Current supply is accomplished via the Connector Board, where it is taken via a relay controlled by the PERIF on the Digital Generator.

6.1.8 Power Supplies

The UPD includes separate power supplies for the analog and digital circuit parts.

6.1.8.1 Analog Power Supply

The input voltage is to be selected using the selector switch next to the power connector.

The analog power supply supplies the function groups of the Analog Generator and the Analog Analyzer. The current supplies of the Analog Generator and of the input sections of the two Analog Analyzers are independent of one another and isolated. The analyzer is further supplied with ± 15 V referred to chassis potential from the secondary side of the power transformer (T1) and with 5 V, 6 V from the 12 V of the digital power supply.

Special features of the configuration:

- Power transformer (T1) with special capacitive shielding of the secondary windings for supply of the floating Analog Generator
- Low-voltage transformer (T2), supplied by power transformer, with special capacitive shielding of the secondary windings for supply of the floating and isolated input channels of the Analog Analyzer
- High-quality magnetic shielding of the transformers
- Series stabilization of all operating voltages

(see circuit diagram 1030.7500.01S sheet 1)

6.1.8.2 Digital Power Supply

The digital circuit parts of the UPD are supplied by a primarily clocked switching power supply (on the partition between analog and digital section). This power supply provides +5 V, -5 V, +12 V und -12 V with a maximum output power of 130 watts.

The input voltage is detected automatically on switch-on.

6.2 Measurement Equipment and Additional Devices

Due to the different requirements of each device a description of the necessary equipment is given in the corresponding sections.

6.3 Troubleshooting

General Information:

Checking of the internal test points and interfaces is usually not necessary, since the instrument includes both an analyzer and a generator. A lot of faults can be located by means of loop measurements (analyzer setting INTERN).

Proper functioning of the digital section should be ensured by (internal) checking before testing of the analog circuit parts.

For measurements on individual cards, the Service Kit provides appropriate adapter cards for operating the respective boards outside the instrument.

During the selftest of the UPD (following switch-on) or during UPD operation, the following error messages may be displayed:

- General faults:
 - Faint beeps after switching on
The digital power supply cannot start, see section 7.6.11, page 7.302.
 - Loud beeps of the built-in loudspeaker after switching on
Faults detected by the BIOS, see page 7.274.
 - HDD-FFD failure ... press F1:
The AT combi controller fails. see page 7.287.
 - No DSP Boards found! ...
Neither Digital Analyzer nor Generator have been found; the AT bus may be faulty.
 - Cannot open file C:\UPD\DSP\GENOUT.OUT! Check installation!
Fault in hard disk or file system (installation)!
 - Cannot boot DSP ...! ...
See page 7.242 (Generator) or page 7.231 (Analyzer) or page 7.252 (AES/EBU).
 - Generator DSP not available!
See page 7.242.
 - Digital Generator not found!
See page 7.242.
 - Analyzer DSP not available!
See page 7.231.
 - Digital Analyzer not found!
See page 7.231.
 - XMM not found or not enough memory
Either SIMM memories of the AT have failed and the main memory of the AT has become too small as a result of this, or the XMM ² is not enabled (e.g. due to a crash of the preceding program run.
A further possible cause for this fault may be that the memory assigned under DOS-SHELL is too small.
 - GEN-Digital-Board not installed!
See page 7.242.
 - ANL-Digital-Board not installed!
See page 7.231.

²XMM = eXtended Memory

- Analyzer Board not present; ...
See page 7.231.
 - Timeout while waiting for analog done!
Fault in the internal setting interface to the analog boards
 - Cannot open file C:\UPD\DSP\DUMP.OUT!
Fault in the hard disk or file system (Installation)!
 - The graphic window is filled with pattern on the FFT
Fault in the Digital Analyzer or the memory on the PC is reserved. Control the BIOS parameters and on a 486 motherboard check and execute the file CPU.EXE. (This file recognizes the CPU and modifies the chip set for read/write access on the needed memory).
- Fault in the Analog Generator
These error messages are explained in greater detail in section 7.3.1.5 on page 7.112.
 - Fault in the Analog Analyzer
 - ADC-Board: Error in board ID. / Board not present
When reading out the board ID, the ADC board is missing. See page 7.91 or 7.75.
 - Analog motherboard: Error in board ID.
Fault in Motherboard, see page 7.91 or 7.75.
 - No analog analyzer boards detected.
Fault in Motherboard, see page 7.91 or 7.75.
 - Noname Board (Analyzer) not present; ...
 - Mother Board (Analyzer) not present; ...
Fault in Motherboard, see page 7.91 or 7.75.
 - Calibration Measurement failed, calibration data unchanged.
May occur during calibration of the Highspeed option; perhaps, the ADC board is not plugged in.

6.4 Testing and Adjustment

Testing and adjustment is different for analyzer and generator and therefore described in the corresponding sections.

6.5 Disassembly and Assembly of the UPD

Caution:
Before opening the instrument pull the power plug.

Opening:

Loosen the two rear-panel feet supports (with two captive screws each) and remove towards the rear. Pull the upper and lower cover towards the rear out of the guide. Loosen the security bracket above the digital section and unscrew and remove the cover above the analog section.

Assembly:

Fasten the cover above the analog section, making sure that the screw for the bracket above the digital section remains freely accessible. Mount the security bracket above the digital section so that the boards are positioned in the slots of the plastic guides.

Position the upper and lower cover and slide into the groove from the front. Make sure that no cables are caught with the lower cover. *Firmly tighten* the feet of the instrument to ensure minimum RF leakage of the instrument.

Chapter 7

Test and Repair of Boards

7.1 Power Supply and Motherboard

7.1.1 Analog Power Supply

Circuit diagram	1030.9560.01 S
Component location plan	1030.9560
Parts list	1030.9560.01 SA

Circuit diagram overview	
Sheet	Contents
1/4:	floating supply for input section Analyzer 1, pin assignment
2/4:	floating supply for input section Analyzer 2
3/4:	grounded supply for Analog Motherboard and Analyzer 1/2
4/4:	floating supply for Analog Generator

7.1.1.1 Function

The Analog Power Supply is supplied from the floating secondary windings of power transformer T1 and low-voltage transformer T2 as well as from the +12 V of the Digital Power Supply. All supply voltages for the two Analog Analyzers and the Analog Generator are stabilized via analog series regulators (N1 ..N3, N21 ..N23, N30 ..N33, N40 ..N45). The supply consists of 4 isolated groups that are independent of each other. Each group is provided with its own ground lines (GND ...) and its own potential reference (SENSE ...) to the Analog Motherboard. The stabilized output voltages are short-circuit-proof and protected against thermal overload.

7.1.1.2 Measuring Instruments and Auxiliary Means

Digital multimeter (voltage AC/DC, current 2A DC, resistor)
 Analog power adapter (incl. in Service Kit UPD-Z2, order No. 1031.3208.02)

7.1.1.3 Testing and Troubleshooting

- Testing the Operating Voltages
 - Switch off UPD, disconnect flat cable connection W20 at the bottom of the analog power supply and insert intermediate adapter according to the inscription.
 - Switch on UPD and measure voltage values at the bridges.
 - For test values, see section 7.1.1.5 External Interfaces, page 7.3.
 - NOTE: Check that the correct ground reference (SENSE ...) is used!
 - In the case of a fault: After disconnecting the appropriate bridges of the adapter, check the supply with no load applied.
- Measurement of the current consumption
 - A current meter for testing the current consumption can be cut in after disconnecting the bridges of the adapter.
- Checking the input voltages
 - For troubleshooting on rectifiers and series regulators, remove the analog power supply (see Disassembly and Assembly). The power supply can be partly disassembled and tilted towards

the rear in operating condition. To this end, plug adapter to W20 and unscrew the transformer, if necessary.

Check the rectifier voltages or the regulator input voltages (DC value and *ripple*) as well as the 12-V supply from the digital power supply.

7.1.1.4 Disassembly and Assembly

Pull the power plug

Remove lower instrument cover of UPD, disconnect cable W20 at the bottom of the power supply. Detach Bowden cable of power switch: for this purpose, switch on power supply, depress contact piece in the switching direction using a small tool and hold it. Take hold of the Bowden cable behind the adjusting screw using tweezers and lever it out of the contact piece with the brass part.

CAUTION: The adjusting screw of the Bowden cable is secured and should not be loosened!

Withdraw the power supply board towards the rear after removing the 5 outer screws on the rear side. Disconnect cable connectors W1/W10 and X16 to the digital power supply, then completely take out the module .

Loosen the rear 6-mm metric screws using socket wrench SW10 and put down the two transformers at the side. Unscrew the heat sink for the voltage regulators from the rear (5 screws). Unscrew the power supply board from inside (6 screws) and remove completely after disconnecting the cable connectors (plastic locking!).

When replacing the board in the reverse order note the following:

For fastening the transformers use open-end wrench SW12 to hold the hex-head screw in position.

Take care not to catch any cables and to keep the Bowden cable of the power switch freely accessible.

7.1.1.5 External Interfaces

Operating voltages						
name	Signal description	≡	source dest.	range	connector	comment
+12V	Ground		Digital power supply	12±0.5V typ. 600mA	X16.1	ref. to chassis
GND					X16.2	
Analyzer						
GND[A2]	Ground Ana 2	O	AnaMoth	-18±1V 75mA 18±1V 75mA 6±0.2V 370mA	X20.1,2	floating to Ana 2
-18V[A2]		O	AnaMoth		X20.3	
+18V[A2]		O	AnaMoth		X20.4	
+6V[A2]		O	AnaMoth		X20.5	
SENSE[A2]			AnaMoth		X20.6	
	Potential-reference Ana 2					meas. ref.
GND[A1]	Ground Ana 1	O	AnaMoth	-18±1V 75mA 18±1V 75mA 6±0.2V 370mA	X20.7,8	floating to Ana 1
-18V[A1]		O	AnaMoth		X20.9	
+18V[A1]		O	AnaMoth		X20.10	
+6V[A1]		O	AnaMoth		X20.11	
SENSE[A1]			AnaMoth		X20.12	
	Potential-reference Ana 1					Meas. ref.
GND	Ground	O	AnaMoth	-15±0.75V 450mA	X20.13,14	Chassis
-15V		O	AnaMoth		X20.15,16	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
+15V	Potential reference	O	AnaMoth	15±0.75V 450mA	X20.17,18	Meas. reference
+5V		O	AnaMoth	5±0.15V 350mA	X20.19,20	
+6V		O	AnaMoth	6±0.2V 200mA	X20.21,22	
SENSE		I	AnaMoth		X20.23,24	
Generator						
GND[G]	Ground	O			X20.25,26	floating
+24V[G]	Potential reference	O	AnaMoth	24±1.2V 250mA	X20.27,28	Meas. reference
-24V[G]		O	AnaMoth	-24±1.2V 250mA	X20.29,30	
-15V[G]		O	AnaMoth	-15±0.75V 315mA	X20.31,32	
+15V[G]		O	AnaMoth	15±0.75V 315mA	X20.33,34	
+6V[G]		O	AnaMoth	6±0.2V 840mA	X20.35,36	
+5V[G]		O	AnaMoth	5±0.15V 190mA	X20.37,38	
SENSE[G]		I	AnaMoth		X20.39	
GND[G]		O	AnaMoth		X20.40	
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

7.1.2 Analog Motherboard

Circuit diagram 1030.9060.01 S
Component location plan 1030.9060
Parts list 1030.9060.01 SA

Circuit diagram overview	
Sheet:	Contents
1/7:	Block diagram
2/7:	Analog Generator: DAC LINK, DATA LINK IN, GENCONN
3/7:	Connectors Analog Generator, DATA MUX, DATA LINK OUT, ENABLE BIT, spare connector Analog Analyzer
4/7:	Connectors Analog Analyzer, internal signal connection Generator ↔ Analyzer
5/7:	Analyzer Phase Comparator
6/7:	Analog Analyzer: Relay control, serial control interface/register, board identification, monitor outputs, ext. filter (not fitted)
7/7:	Cable connection W20 to analog power supply

7.1.2.1 Function

The Analog Motherboard is *no purely passive* module. It contains all connections for the operating voltages and the signals between the individual plug-in modules and, besides, *active* circuits for the generator and the analyzer.

The operating voltages for the Generator and the Analyzer are routed via cable connector W20B from the Analog Power Supply to the Analog Motherboard. The circuit parts in the power supply and the motherboard and thus the generator and analyzer grounds are completely independent of each other.

In the circuit diagram of the motherboard, the signal names are marked to indicate where they belong to:

Marking	Module
[D]	Digital Generator
[G]	Analog Generator
[A]	Analog Analyzer
none	Analog or Digital Analyzer

Generator: see section Analog Motherboard (Generator section), page 7.168

Analyzer: see section Analog Motherboard (Analyzer section), page 7.75

The internal connection Generator ↔ Analyzer is described with the Analyzer.

7.1.2.2 Disassembly and Assembly

- Remove upper and lower instrument cover and upper screening panel (front right).
- Remove analog plug-in modules A21...A26 (see also section 7.2.8.5, page 7.95)
- Disconnect cable connectors W800, W801 to the front panel and W802, W803 to the rear (plastic locking!)
- Disconnect cable connectors W31, W35 (34-contact each) on Digital Analyzer 1 and 2 as well as W32 (16-contact) on the Digital Generator and W20B (40-contact) at the bottom of the Analog Power Supply.
- Remove lower screening cover: for this purpose, remove 2 screws each from the top in the middle of the motherboard, from the bottom at cable W20, on the inside of the cover and on the outer side section (Do **not** remove fixing screw of the power supply partition on the side section).
- Unscrew 6 further screws of the Analog Motherboard at the bottom.
- Take out the board and carefully route connection cables W31, W32, W35 through the cutout of the partition.
- For replacement, proceed in the reverse order.

7.2 Analog Analyzer

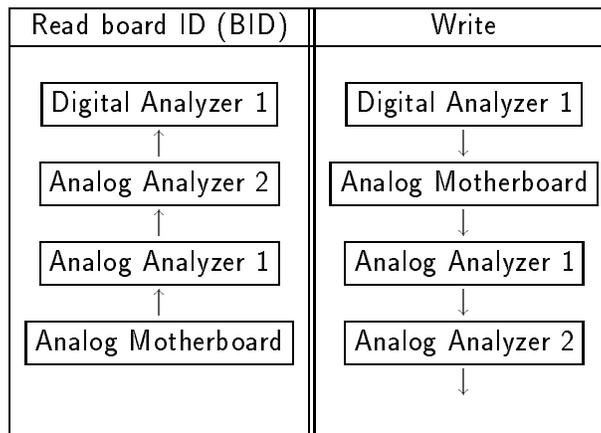
7.2.1 Overview

The Analog Analyzer consists of the two plug-in modules Analog Analyzer 1 and 2 as well as the Analog Motherboard, whose analyzer section includes the circuit parts for the internal signal connection Generator ↔ Analyzer, the monitor outputs and the phase comparator.

The Analog Analyzers 1 and 2 are of identical design, containing an ADC Board as subassembly (with channel 2 only with Option Highspeed UPD-B3).

Hardware control is performed via a serial interface by Digital Analyzer 1, all modules of the Analog Analyzer being series-connected like in a long shift register.

Control data flow:



See circuit diagrams: Analog Motherboard 1030.9060.01 S Sheet 1
 Analog Analyzer 1030.9102.01 S Sheet 1
 ADC Board 1030.9260.01 S Sheet 1
 and section 7.2.7.1, page 7.75

7.2.2 Board Replacement

This section explains the measures required for replacing an Analog Analyzer board. Removal and replacement of the boards is performed according to the section 'Disassembly and Assembly'. Replacement boards are factory-adjusted. In the event that an adjustment is required nevertheless, it is to be performed only for the respective board according to section 7.2.3 'Adjustment', page 7.7. After replacing an analyzer channel, increased tolerances due to delay differences of the comparator N502 may result in the case of phase measurement.

- Check the phase coincidence of the two channels according to section 7.2.5, page 7.17.
- Excessive tolerance can be corrected for one channel by installing a ceramic capacitor in parallel with R510 at the output of N502.
- approximate value for C
 - 10pF in channel 2 for $\Delta = + 0.5^\circ$ at $f = 20 \text{ kHz}$
 - 10pF in channel 1 for $\Delta = - 0.5^\circ$ at $f = 20 \text{ kHz}$

After replacing and, if necessary, adjusting the board, various calibration data are to be determined using the following table and section 7.2.4 'Calibration', page 7.12. After entering the values referred

- to be continued -			
Function	Element	Signal	Set analyzer
Unbalance rejection	C428	3V RMS, 16kHz	ANLG 22kHz, BAL Range FIX, 3V
distortion, low frequency	R435	3V RMS, 10Hz THD d2, d3 < -120 dB	ANLG 22kHz, UNBAL Range FIX, 3V Function THD
ADC Board:			Ch1, (Ch2 ²)
Frequency response Aliasing filter 100kHz	C215	3V RMS $\pm 0.02\%$ 100Hz, 20kHz	ANLG 100kHz, UNBAL Range FIX, 3V
300kHz	C216	3V RMS $\pm 0.02\%$ 100Hz, 20kHz	ANLG 300kHz, UNBAL Range FIX, 3V

7.2.3.3 Adjusting the Analog Analyzer modules Ch1 and Ch2

The two channels are to be adjusted independently of each other.

The adjustment is to be performed with at least one ADC Board for Analyzer 1.

- DC offset input buffer

- Switch off instrument
- Remove board A22 (channel 1) or A21 (channel 2), remove the left-hand screening cover on the component side and plug the respective board onto an adapter card. (Use Service Kit order No. 1031.3208.02).
The input coaxial connector may remain open.
- Switch the instrument on again.
- Test setup
Connect DC voltmeter (Hi) to test point X302.1 (N330.6) or X302.3 (N390.6). Reference connection (Lo) is test point X302.2 - connected with left-hand part of the screening panel, isolated from the chassis.
(indication in brackets, → terminals with pilot instruments SER 828443)
- UPD setting

Analyzer Panel:	Instrument	ANLG 22kHz
	Min Freq	10 Hz
	Channel(s)	1 \equiv 2
	Input	BAL XLR
	Impedance	20 k Ω
	Range	FIX, 3 V

- Adjustment with input voltage = 0 V

* to 0 \pm 0.2 mV at test point X302.1 (N330.6) using R338

²with Option Highspeed UPD-B3

- * to 0 ± 0.2 mV at test point X302.3 (N390.6) using R398
- After adjustment, switch off the instrument, complete the boards and replace. Check that the coaxial plugs are properly connected and take care **not** to catch any cables. Switch the instrument on again.
- NOTE: The calibration is independent of this adjustment.
- Frequency response unbalanced input voltage divider 20/40 dB
 - Test setup
Connect sinewave generator via coaxial cable to the unbalanced BNC inputs of the UPD Analog Analyzer Ch1, Ch2.
 - Test signals
Sine $V_{rms} = 10$ V ± 0.02 %, 100 V ± 0.02 %, 100 Hz and 20 kHz
Apply sinusoidal voltage $V_{rms} = 10$ V, 100 V, frequency 100 Hz and 20 kHz in sequence to the BNC input sockets Ch1/Ch2.
- Adjustment of 20-dB divider
 - UPD setting

Analyzer Panel:	Instrument	ANLG 22kHz
	Min Freq	10 Hz
	Channel(s)	1 \equiv 2
	Input	UNBAL BNC
	Range	FIX, 10 V
	Function	RMS
	Unit	V
	Meas Time	AUTO
	Filter	OFF
 - Measurement: Set AC generator to 10 V (± 0.02 %), 100 Hz, store UPD readout V_i as reference STORE Ch. . ., set Unit dBr, \rightarrow readout 0 dBr
 - Adjustment: Set AC generator to 10 V (± 0.02 %), 20 kHz, using C211 adjust to the readout at 100 Hz, $V_i \pm 0.005$ dBr
- Adjustment of 40-dB divider
 - UPD setting

Analyzer Panel:	Range	FIX, 100 V
-----------------	-------	------------
 - Measurement: Set AC generator to 100 V (± 0.02 %), 100 Hz, Store UPD readout V_i as reference STORE Ch. . ., set Unit dBr, \rightarrow readout 0 dBr
 - Adjustment: Set AC generator to 100V (± 0.02 %), 20 kHz, using C217 adjust to the readout at 100 Hz, $V_i \pm 0.005$ dBr
 - NOTE: Without calibration, readouts V_i may deviate max. ± 5 % from the nominal value of the input voltage. The calibration is independent of this adjustment.
- Unbalance rejection

– UPD setting

Analyzer Panel:	Instrument	ANLG 22kHz
	Min Freq	10 Hz
	Channel(s)	1 \equiv 2
	Input	BAL XLR
	Impedance	20 k Ω
	Range	FIX, 3 V
	Function	RMS SELECT
	Meas Time	AUTO
	Unit	dBr
	Bandwidth	3 %
FREQ MODE	FIX 16 kHz	

– Test setup

Connect unbalanced sinewave source (UPD Generator, Output UNBAL) to the balanced XLR input of the UPD via coaxial cable with two test adapters consisting of two 300- Ω resistors (Δ tolerance better than $\pm 0.01\%$) (see section 5, page 7.21).

– Adjustment

- * Apply common-mode signal $V_{com} = 3\text{ V}$, 16 kHz to the test adapter
- * Enter display reference 3 V on the UPD Analyzer Panel
- * Using C428 adjust readout to minimum (as a preference, use bargraph for optimum adjustment). Limit value: $< -60\text{ dBr}$ at 16 kHz

– NOTE: The calibration is independent of this adjustment.

● Distortion at low frequencies

– Test setup

Connect sinewave generator via coaxial cable to the unbalanced BNC inputs of the UPD Analog Analyzer Ch1, Ch2.

– Test signal

Low-distortion signal $V_{rms} = 3\text{ V}$, frequency 10 Hz, distortion d2, d3 better than 120 dB.

– UPD setting

Analyzer Panel:	Instrument	ANLG 22kHz
	Min Freq	10 Hz
	Channel(s)	1 \equiv 2
	Input	UNBAL BNC
	Range	FIX, 3 V
	Function	THD
	Meas Mode	All di
	Unit	dB
DISPLAY Panel	Operation	Spectrum
	Trace A	FUNC1
	Y-max	-70dB
	Y-min	-130dB

- Adjustment

Set to minimum total distortion factor using R435. In most cases, the optimal adjustment is obtained if the 2nd and 3rd-order harmonics are set to the same level in the graphical representation.

Limit values: d2, d3 lie at about < -110 dB at 10 Hz.

CAUTION: *This adjustment affects the calibration of the measurement range.*

7.2.3.4 Adjusting the ADC Board

In the basic configuration of the UPD, only the Analog Analyzer channel 1 contains an ADC board. With the Option UPD-B3, an ADC board is also installed in channel 2. In this case, channel 2 requires the same adjustment as channel 1. For retrofitting the option, the ADC board is already adjusted in the factory.

- Frequency response of aliasing filters ANLG 100/300kHz

- Test setup

Connect sinewave generator via coaxial cable to the unbalanced BNC inputs of the UPD Analog Analyzer Ch1, Ch2.

- Test signal

Sinewave voltage $V_{rms} = 3 \text{ V} \pm 0.02 \%$, frequency 100 Hz and 20 kHz

- Adjustment of instrument ANLG 100kHz

- UPD setting

Analyzer Panel:	Instrument	ANLG 100kHz
	Channel(s)	1 or 2
	Input	UNBAL BNC
	Range	FIX, 3 V
	Function	RMS
	Unit	V
	Meas Time	AUTO
	Filter	OFF

- Measurement

Set AC generator to 3 V ($\pm 0.02 \%$), 100 Hz, store UPD readout V_i as reference STORE Ch1 or Ch2, set Unit dBr, \rightarrow readout 0 dBr

- Adjustment

Set AC generator to 3 V ($\pm 0.02 \%$), 20 kHz, using C215 adjust to the readout at 100 Hz, $V_i \pm 0.005$ dBr

- Adjustment of Instrument ANLG 300kHz

- UPD setting

Analyzer Panel:	Instrument	ANLG 300kHz
-----------------	------------	-------------

- Measurement

Set AC generator to 3 V ($\pm 0.02 \%$), 100 Hz, store UPD readout V_i as reference STORE Ch... , set Unit dBr, \rightarrow readout 0 dBr

– Adjustment

Set AC generator to 3 V ($\pm 0.02\%$), 20 kHz, using C216 adjust to the readout at 100 Hz, $V_i \pm 0.005$ dBr

NOTE: Without calibration, readouts V_i may deviate max. $\pm 2\%$ from the nominal value of the input voltage. In the case of readjustment, this adjustment affects the calibration of the measurement range of the instruments ANLG 100/300 kHz. A slight correction, however, does not affect the calibration!

After adjustment, complete the instrument and, if necessary, calibrate the Analog Analyzer.

7.2.4 Calibration

7.2.4.1 General Information

Preparing the instrument: Connect external keyboard for editing the calibration file.
The UPD needs **not** be opened for calibration.

Calibration conditions: Ambient temperature 23 ± 3 °C
AC supply voltage, nom. value $\pm 5\%$
Warmup time approx. 60 min.

The Analog Analyzers 1 and 2 can be calibrated in any order of the calibration steps independently of each other.

EXCEPTION: When retrofitting the Option Highspeed UPD-B3, the RMS level calibration of channel 2 can be performed by means of the built-in routine without auxiliary equipment, assuming that channel 1 has already been calibrated. (Cal routine only fitted with firmware 1.Q.94 or greater)

The calibration procedures can be performed manually or via IEC bus for both channels at the same time. The calibration factors acquired (CF) are to be entered in the UPD software in a special cal file using a text editor. Prior to each calibration or partial calibration, the appropriate values are to be set to the *default* CF = 1.0000.

7.2.4.2 Calibration Overview

Function	Cal voltage	Frequency	Analyzer setting
Level:			Ch1, Ch2
RMS	3V RMS $\pm 0.05\%$	1kHz	ANLG 22kHz, Min Freq 10Hz, UNBAL, Range FIX 3V
RMS	3V RMS $\pm 0.05\%$	1kHz	ANLG 100kHz, UNBAL, Range FIX 3V
DC	+3V $\pm 0.05\%$	–	UNBAL, Range FIX 3V
Frequency:			Ch1 or Ch2
- to be continued -			

- to be continued -			
Function	Cal voltage	Frequency	Analyzer setting
FREQ	3V RMS	1kHz $\pm 0.0005\%$	Freq Meas Time FAST, UNBAL, Range FIX 3V
Notch filt.:			Ch1, Ch2
Range 0 ³	3V RMS	100kHz $\pm 0.05\%$	ANLG 300kHz, UNBAL, Range FIX 3V, Anlg Notch VALUE 100kHz
Range 1 ³	3V RMS	22kHz $\pm 0.05\%$	ANLG 100kHz, UNBAL, Range FIX 3V, Anlg Notch VALUE 22kHz
Range 2 ³	3V RMS	3200Hz $\pm 0.05\%$	ANLG 22kHz, UNBAL, Range FIX 3V, Anlg Notch VALUE 3200Hz
Range 3 ³	3V RMS	470Hz $\pm 0.05\%$	ANLG 22kHz, UNBAL, Range FIX 3V, Anlg Notch VALUE 470Hz
Range 4 ³	3V RMS	70Hz $\pm 0.05\%$	ANLG 22kHz, UNBAL, Range FIX 3V, Anlg Notch VALUE 70Hz

The calibration voltages may deviate $\pm 5\%$ from the nominal values, but must be known with the tolerances given above (\rightarrow nominal value).

7.2.4.3 Calibration of Measurement Range and Frequency

- Set calibration conditions by means of the table Calibration overview
- Apply calibration voltage, frequency to BNC connector(s) (nominal values)
- Determine readout on UPD \rightarrow actual values.
- Calculate calibration factors from actual/nominal value.

Prior to the DC calibration, a DC offset correction is to be performed: This is done automatically after activating the DC test function or after confirmation in the selection window of the OPTION Panel:

CALIBRATION ANL 'ZERO AUTO' 'ONCE' (with earlier firmware versions CALIBRATE 'OFF-SET').

7.2.4.4 Calibration of Notch Filter

- Set calibration conditions by means of the table Calibration overview
- Apply calibration voltage, frequency to BNC connector(s) (nominal values)
- Further UPD settings:

³UPD-internal

Generator Panel:	Instrument	ANLG 110kHz
	Ref Freq	= Notch nominal frequency
	Low Dist	OFF
	Sweep Ctrl	AUTO SWEEP
	Next Step	ANLR SYNC
	X Axis	FREQ
	Spacing	LIN POINTS
	Start	0.98 f/fr (0.95 at fr = 70Hz)
	Stop	1.02 f/fr (1.05 at fr = 70 Hz)
	Points	50
Voltage	3V	
Analyzer Panel:	Function	RMS
	Unit	dBr
	Meas Time	AUTO
	Reference	3V
	Anlg Notch	ON
	FREQ/PHASE	OFF
	Filter	OFF
DISPLAY Panel:	OPERATION	Curve Plot
	Unit	dBr
	Reference	3V
	Scale	MANUAL
	Spacing	LIN
	Top	0dBr
	Bottom	-60dBr
	X Axis Unit	f/fr
	Reference	= Notch nominal frequency
	Spacing	AUTO

- The measurement for calibration is performed after setting the generator sweep and the DISPLAY Panel by means of Start Single-Sweep and evaluation of the graphics. After the sweep, the notch filter minima are to be directly read out as measured values in graphics mode via the commands CURSOR, SET TO, MIN A or MIN B.
The calibration factors are thus determined from actual/nominal value(f/fr).

7.2.4.5 Calibration of ADC Board with Option Highspeed UPD-B3

RMS level calibration of channel 2 with Option Highspeed UPD-B3:

This calibration is required if the option is retrofitted.

It can be performed without auxiliary means after calling the calibration routine in the UPD OPTION Panel. The same procedure is required when removing the Option.

PREREQUISITES: Analyzer channel 1 is already calibrated and okay, because the cal routine uses channel 1 as reference! Properly functioning Analog Generator (function SINE, Low Dist OFF).

- Disconnect cable on Analog Generator and Analyzer
- Call cal routine by the following setting in the OPTION Panel: line CALIBRATION ANL 'Ch2 Auto' 'ONCE'

- Having finished the run automatically **without** error message, the calibration is completed successfully. The cal file contains the new cal values for channel 2. The file needs **not** be edited.

NOTE: The cal routine is available with firmware 1.Q.94 or greater. With earlier versions, the calibration is to be performed manually as with channel 1, or an *update* of the UPD software is required before.

7.2.4.6 Calibration Files

The UPD software contains two calibration files for the Analog Analyzer:

- File with all calibration parameters and the current calibration data, available in DOS system operation under

C:\UPD\REF\ANLRO.CAL.

This is the current CAL file which is read when the UPD program is started. It is **not** included with an UPD software *update* and is **not** overwritten either.

- File with all calibration parameters and *default* values CF = 1.0000 for all calibration data, available in DOS system operation under

C:\UPD\REF\ANLRO_UN.CAL.

This file is enclosed with an *update* of the UPD software.

Default file:

```

// Calibration ANALOG ANALYZER
// Notch filter Channel 1:
1.00000000 // cal_notch (Range 0); ±2%
1.00000000 // cal_notch (Range 1); ±2%
1.00000000 // cal_notch (Range 2); ±2%
1.00000000 // cal_notch (Range 3); ±2%
1.00000000 // cal_notch (Range 4); ±5%
// Notchfilter Channel 2:
1.00000000 // cal_notch (Range 0); ±2%
1.00000000 // cal_notch (Range 1); ±2%
1.00000000 // cal_notch (Range 2); ±2%
1.00000000 // cal_notch (Range 3); ±2%
1.00000000 // cal_notch (Range 4); ±5%
// RMS-Ranges:
1.00000000 // cal_range (ANLG 22kHz , Channel 1); ±5%
1.00000000 // cal_range (ANLG 22kHz , Channel 2); ±5%
1.00000000 // cal_range (ANLG 100/300kHz, Channel 1); ±2%
1.00000000 // cal_range (ANLG 100/300kHz, Channel 2); ±2%
// DC-Ranges:
1.00000000 // cal_dc (Channel 1); ±10%
1.00000000 // cal_dc (Channel 2); ±10%
// Frequency:
1.00000000 // cal_freq; ±0,01%

```

Using a text editor (e.g. EDIT under DOS), the results from the described cal procedures are to be entered into the lefthand column of the current CAL file ANLRO.CAL.

NOTE: The lefthand column may only be edited in the given format with decimal point and without further characters. Texts to the right of the characters // are comments, e.g. the permissible tolerances referred to the nominal value $CF = 1$.

(see section Error Messages during the Selftest)

Before performing a total calibration or if the current cal file has been lost, first copy the *Default* file from ANLRO_UN.CAL to ANLRO.CAL. The Analog Analyzer is then uncalibrated with all $CF = 1$.

In the case of subsequent calibration, e.g. of a particular calibration value, only this calibration factor can be set to 1.0000 by editing the file ANLRO.CAL.

If there is no error message, it is sufficient to multiply the values from the cal procedures with the previous values of the file and enter the results in the current file without editing the cal file before with $CF = 1$.

7.2.4.7 Error Messages during the Selftest

When the UPD is started, the calibration data are read in and checked for compliance with the permissible tolerances during the selftest. If the file is faulty or the tolerance exceeded, the following error messages are produced:

- Cannot open calibration file ANLRO.CAL

CANCEL: Run Analyzer uncal

ENTER: Restore old ANLRO.CAL from CMOS-RAM

The file ANLRO.CAL does not exist, or calibration factors CF are missing.

CANCEL: Analyzer not calibrated, all $CF = 1.0$, ANLRO.CAL unchanged

All $CF \rightarrow 1.0$

The file ANLRO.CAL is **not** changed.

The selftest is continued.

ENTER: If the CMOS RAM contains valid CF, the file ANLRO.CAL is created. It contains the previous CF from the CMOS RAM. The UPD calibration may be correct again.

The selftest is continued.

If the CMOS RAM does not contain any valid CF, the following error message is produced:

No valid calibration data in CMOS-RAM

Analyzer not calibrated, all $CF = 1.0$, ANLRO.CAL unchanged

All $CF \rightarrow 1$

The file ANLRO.CAL is **not** changed

The selftest is continued

- Calibration data in File ANLRO.CAL out of tolerance

CANCEL: Run Analyzer uncal

ENTER: Restore old ANLRO.CAL from CMOS-RAM

One or several calibration factors are out of tolerance. The permissible tolerances are indicated in the calibration file as comment (see page 7.15).

Further branching CANCEL/ENTER is the same as above.

7.2.5 Testing the Rated Specifications

7.2.5.1 Measuring Equipment and Auxiliary Means

Measuring instrument	Specifications	R & S
AC calibrator	10Hz ... 300kHz 1mV ... 300V ±0.05% 10Hz ... 22kHz ±0.2% 20kHz ... 50kHz ±0.5% 50kHz ... 100kHz ±1.5% 100kHz ... 300kHz	—
DC calibrator	0 ... ±300V ±0.1%	—
Digital multimeter	resistance measurement, ±0.1%	UDS5
Frequency counter	2Hz ... 300kHz, ±5ppm	—
Low distortion generator	Loop measurement THD, THD+N	UPD -B3
Multisine generator	Two-channel with phase setting -180° ... +180° 2Hz ... 300kHz Error < 0,1° 2Hz ... 22kHz Error < 0,25° 22kHz ... 100kHz	ADS
Test adapter for unbalance rejection (DIN 45404, 45405)	two 300-Ω resistors, ΔR ±0.01% fitted in XLR connector	— — —
Differential-tone highpass (HP DFD)	passive RC highpass for DFD-d2 measurement attenuation >40dB for f < 500Hz attenuation <5dB for f > 4kHz	—
Supply network 1	passive RC matrix for THD measurement	—
Supply network 2	passive RC matrix for MODDIST measurement	—
Supply network 3	passive RC matrix for DFD-d2 measurement	—

Test adapter unbalance rejection: see test sequence,
section 5, page 7.21

Differential-tone highpass: like intermodulation highpass,
see section 7.3.5.1, page 7.153

Supply network 1 ... 3: see test sequence,
section 7.2.5.2, page 7.18

7.2.5.2 Test Sequence

1. Level measurement RMS

Analyzer setting	Instrument	ANLG 22kHz, 100kHz, 300kHz
	Min Freq	2Hz and 10Hz
	Channel(s)	1 \equiv 2
	Input	UNBAL and BAL
	Impedance	20k Ω ⁴
	Range	FIX corresp. to input voltage
	Function	RMS
	Meas Time	AUTO
	Filter	OFF

- Level accuracy at 1kHz

Test device: AC calibrator

Measurement: Connect AC calibrator to input of UPD analyzer
UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 0.05\text{dB}$

To avoid errors in measurement due to noise or broadband interference of the signal source, small levels are to be measured with band limiting by means of lowpasses. Levels $< 30\text{mV}$ should be measured with an accurately defined 100:1 voltage divider, which is connected between signal source and analyzer input.

- Linearity

Test device: AC calibrator

Measurement: Connect AC calibrator to input of UPD analyzer, set various voltages and frequencies.
Relative readout V/V_r , The indicated value measured with 1 V is the reference.
UPD setting and measurement according to test report.

Tolerance:

Voltage	Tolerance V/V_r
0.3V ... 1.15	$\pm 0.1\%$
0.1V ... 0.2V	$\pm 0.25\%$

- Frequency response

⁴Input BAL

Test device: AC calibrator

Measurement: Connect AC calibrator to input of UPD analyzer, relative readout $\Delta\%$, reference is the voltage measured at 1 kHz, UPD setting and measurement according to the test report

Tolerance:

Frequency	Frequency response	Analyzer
2Hz ... 10Hz	$\pm 0.5\text{dB}$	Min Freq 2Hz
10Hz ... 20Hz	$\pm 0.03\text{dB}$	Min Freq 2Hz
10Hz ... 20Hz	$\pm 0.15\text{dB}$	Min Freq 10Hz
20Hz ... 22kHz	$\pm 0.03\text{dB}$	
22kHz ... 50kHz	$\pm 0.1\text{dB}$	Ana 100/300 kHz
50kHz ... 100kHz	$\pm 0.2\text{dB}$	Ana 100/300 kHz
100kHz ... 300kHz	$\pm 1.0\text{dB}$	Ana 100/300 kHz

2. Inherent noise

Analyzer setting	Instrument	ANLG 22kHz
	Min Freq	10 Hz
	Channel(s)	1 \equiv 2
	Input	UNBAL and BAL
	Impedance	300Ω ⁵
	Range	FIX 30mV
	Function	see measurement
	Meas Time	"
	Filter	"

Measurement: Short-circuit BNC inputs of UPD analyzer, XLR inputs of UPD analyzer remain open, UPD setting and measurement according to test report

Tolerance:

Function	Meas Time	Filter	max. readout
RMS	FAST	CCIR UNWTD	$2\mu\text{V}$
QPEAK	SLOW	CCIR WTD	$8\mu\text{V}$

3. Input impedance

Analyzer setting	Instrument	ANLG 22kHz
	Min Freq	2Hz
	Channel(s)	1 \equiv 2
	Input	UNBAL and BAL
	Impedance	see measurement
	Range	Fix 30V

⁵Input BAL

Meas. instr.: Digital multimeter for resistance measurement

Measurement: Measure input impedances of UPD analyzer using ohmmeter, UPD setting and measurement according to test report

Tolerance:

Input	Resistor	Tolerance
UNBAL	1M Ω	-0, +15k Ω
BAL	300 Ω	\pm 1.5 Ω
	600 Ω	\pm 3.0 Ω
	20k Ω	\pm 100 Ω

4. Crosstalk attenuation

Analyzer setting	Instrument	ANLG 22kHz
	Min Freq	10Hz
	Channel(s)	1 & 2
	Input	UNBAL and BAL
	Impedance	600 Ω ⁶
	Range	AUTO
	Function	RMS SELECT
	Unit	V and dBr
	Meas Time	AUTO
	FREQ MODE	GEN TRACK
Generator setting	Output	UNBAL and BAL
	Impedance	5 Ω and 10 Ω ⁷
	Function	SINE
	Low Dist	OFF
	Voltage	10V
	Frequency	20kHz

Test setup: Connect one analyzer channel via a shielded cable to an associated output of the Analog Generator. The other analyzer channel remains **without** signal and can be terminated either externally (UNBAL) or internally (BAL) with 600 Ω .

Measurement:

- UPD setting according to test report
- selective RMS measurement on both channels
- Store measured value of fully driven channel
- Switch to relative readout dBr
- The measured value of the other channel is the crosstalk

Tolerance: Crosstalk < -130dB

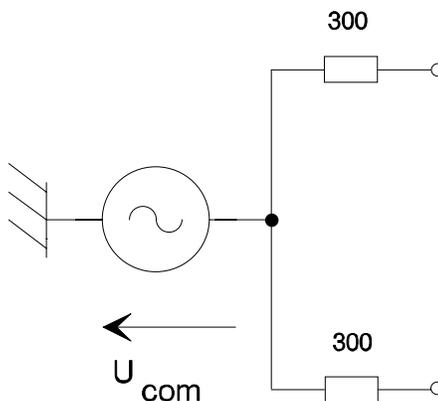
5. Unbalance rejection

⁶Input BAL

⁷Output BAL

Analyzer setting	Instrument	ANLG 22kHz
	Min Freq	2Hz and 10Hz
	Channel(s)	1 ≡ 2
	Input	BAL
	Impedance	20kΩ
	Range	AUTO
	Function	RMS SELECT
	Unit	dBr
	Meas Time	AUTO
	Reference	10V
Generator setting	Output	UNBAL
	Function	SINE
	Low Dist	OFF
	Voltage	10V
	Frequency	see measurement

Test setup: Connect unbalanced sinewave source (UPD Generator, Output UNBAL) to the balanced XLR input of the UPD via coaxial cable with test adapter of two 300-Ω resistors (Δ tolerance better than $\pm 0.01\%$).



Measurement: Set generator frequency on UPD, measurement according to test report

Tolerance:

Frequency	Readout
50Hz	< -110dB
1kHz	< -85dB
16kHz	< -60dB

6. Frequency measurement

Analyzer setting	Instrument	ANLG 22kHz
	Min Freq	2Hz and 10Hz
	Channel(s)	1 \equiv 2
	Input	UNBAL
	Range	FIX 1V
	FREQ/PHASE	FREQ 'COUNTER' ⁸
	Meas Time	FAST

Test device: Frequency counter

Measurement: Connect UPD sinewave generator to the input of the frequency counter and of the UPD analyzer
UPD setting and measurement according to the test report

Tolerance: ± 50 ppm

7. Phase measurement

Analyzer setting	Instrument	ANLG 22kHz and 100kHz
	Min Freq	2Hz and 10Hz
	Channel(s)	1 \equiv 2
	Input	UNBAL and BAL
	Range	FIX, see measurement
	FREQ/PHASE	PHASE
	Unit	$^{\circ}$
	Meas Time	FAST

- Phase coincidence of the two channels

Test device: UPD sinewave generator or AC calibrator or measuring amplifier for higher voltage ranges

Measurement: Connect signal source to the two inputs of the UPD analyzer
UPD setting and measurement according to the test report

Tolerance:

Frequency range	Phase difference	Analyzer
2Hz ... 20Hz	$\pm 1.0^{\circ}$	Min Freq 2Hz
10Hz ... 20Hz	$\pm 1.0^{\circ}$	Min Freq 10Hz
20Hz ... 22kHz	$\pm 0.4^{\circ}$	
22kHz ... 100kHz	$\pm 1.75^{\circ}$	Ana 100/300 kHz

- Phase measuring accuracy

⁸Mode COUNTER selectable with firmware 1.Q.94 or greater

- Test device: Sinewave function generator, two-channel, with phase setting
- Test setup: Connect both outputs of the signal source to the two inputs of the UPD analyzer
- Measurement: Prior to the measurement, determine the 0° phase error of the function generator:
- Connect both inputs of the analyzer to **one** output of the source
 - Measure phase from 20 Hz to 100 kHz (1)
 - Connect both outputs of the signal source to **both** inputs of the UPD analyzer
 - Again measure phase from 20 Hz to 100 kHz (2)
 - The difference from the two results (2) – (1) constitutes the phase error of the two-channel generator
- UPD setting and measurement according to the test report. The indicated result is to be corrected by the inherent phase error of the generator .
- Tolerance: as with phase coincidence

8. DC measurement

Analyzer setting	Instrument	ANLG 300 kHz
	Channel(s)	1 \equiv 2
	Input	UNBAL and BAL
	Impedance	20k Ω ⁹
	Range	FIX corresp. to input voltage
	Function	DC
	Meas Time	FAST

- Offset

Measurement: Short-circuit BNC inputs of UPD analyzer, XLR inputs of UPD analyzer remain open, UPD setting and measurement according to the test report

Tolerance:

Range	max. readout
100mV, 300mV, 1V	$\pm 2\text{mV}$
10V, 30V	$\pm 10\text{mV}$
100V, 300V ¹⁰	$\pm 30\text{mV}$

- Measuring accuracy

⁹Input BAL

¹⁰Input UNBAL

Test device: DC calibrator

Measurement: Connect DC calibrator to input of UPD analyzer
UPD setting and measurement according to the test report

<u>Tolerance:</u>	Voltage	max. indication error
	$\pm 0.3\text{V}$ and $\pm 4,0\text{V}$	$\pm 0.5\%$
	$\pm 0.5\text{V}$	$\pm 0.4\%$
	$\pm 1.0\text{V}$	$\pm 0.3\%$
	$\pm 1.5\text{V} \dots \pm 3,0\text{V}$	$\pm 0.2\%$

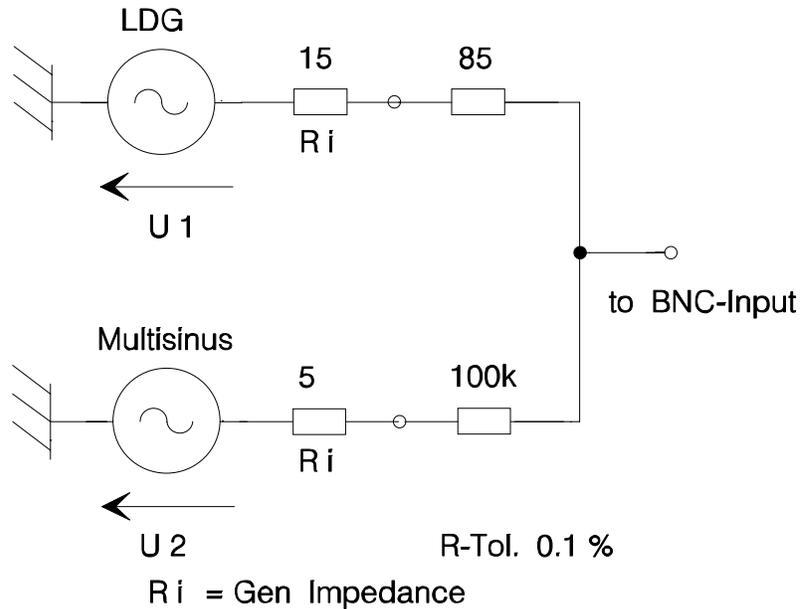
9. Distortion factor THD, THD+N

- Measuring accuracy THD

Analyzer setting	Instrument	ANLG 22kHz, 100kHz, 300kHz
	Channel(s)	1 \equiv 2
	Input	UNBAL
	Common	FLOAT
	Range	FIX 3V
	Function	THD all di
	Fundamentl	AUTO

Test devices: Low-distortion sinewave generator (THD and level accuracy as with UPD LDG Generator), Multisine generator (frequency and level accuracy as with UPD Universal Generator), supply network 1

Test setup:



Measurement: Sinewave generator 2V, different fundamentals
 Multisine: harmonic signal – with 60 dB attenuation, a multisine is added, ref 2V, set level of fundamental to -140dB , level of harmonic U_i in dB according to nominal value of $d_i + 60\text{dB}$ and frequency $i * \text{fundamental frequency}$
 UPD setting and measurement according to test report
 Measure harmonic d_i and compare with nominal readout $U_i - 60\text{dB}$

Tolerance:

THD Nom. value	max. indication error	Analyzer
-50dB	$\pm 0.5\text{dB}$	ANLG 22kHz
-80dB	$\pm 0.5\text{dB}$	"
-85dB	$\pm 0.75\text{dB}$	"
-90dB	$\pm 1.0\text{dB}$	"
-60dB	$\pm 0.5\text{dB}$	ANLG 100kHz
-75dB	$\pm 0.5\text{dB}$	"
-80dB	$\pm 1.0\text{dB}$	"
-65dB	$\pm 0.5\text{dB}$	ANLG 300kHz
-70dB	$\pm 0.75\text{dB}$	"
-80dB	$\pm 1.5\text{dB}$	"

- Inherent distortion THD, THD+N
 Testing of the THD, THD+N inherent distortion is performed as loop measurement together with the Low Distortion Generator of the UPD (see section 7.3.5.2, page 7.155).

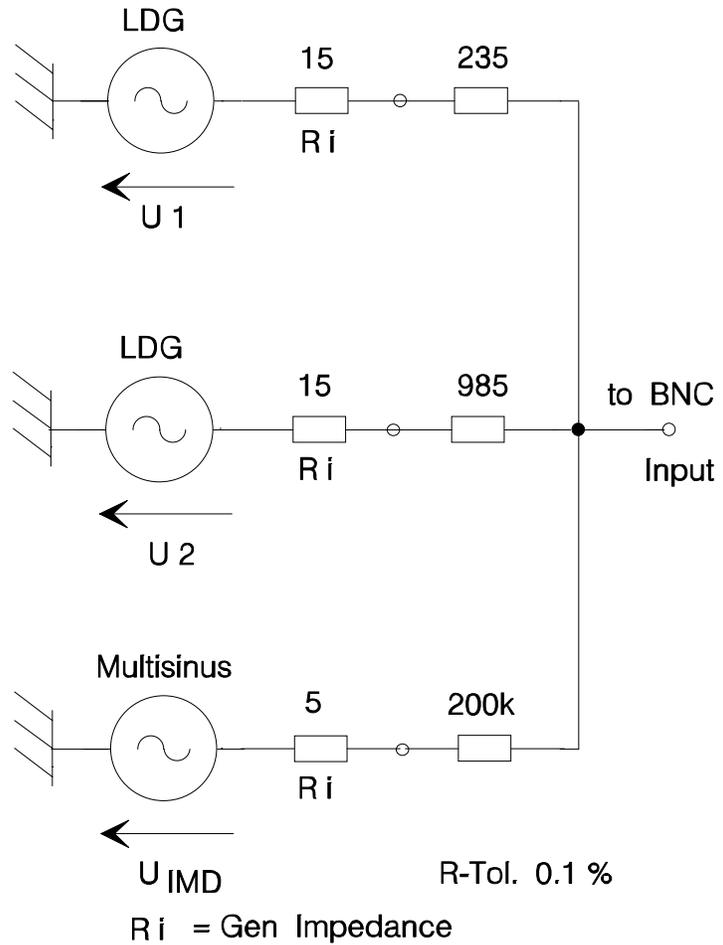
10. Intermodulation MOD DIST

Analyzer setting	Instrument	ANLG 22kHz. 100kHz. 300kHz
	Channel(s)	1 \equiv 2
	Input	UNBAL
	Common	GROUND
	Range	FIX corresp. to signal
	Function	MOD DIST

- Measuring accuracy MOD DIST

Test devices: two low-distortion sinewave generators (THD and level accuracy as with UPD LDG Generator), Multi-sine generator (frequency and level accuracy as with UPD Universal Generator), supply network 2

Test setup:



Signal: Sinewave generator 1: different RF carrier frequencies
 Sinewave generator 2: $AF_{level} = 4 * RF_{carrier}$, set different AF frequencies
 Multi-sine generator: Noise signal – with 60-dB attenuation a multi-sine is added, $Ref - Volt = V_{RF}$, $U_3 \dots U_6$ in dBr

No of Sine	Frequency	Level
1	f_{AF}	-140dBr
2	f_{RF}	-140dBr
3	$f_{RF} - 2 * f_{AF}$	U3
4	$f_{RF} - f_{AF}$	U4
5	$f_{RF} + f_{AF}$	U5
6	$f_{RF} + 2 * f_{AF}$	U6

Measurement: UPD setting and measurement according to test report
Measure MOD DIST and compare with nominal readout

Tolerance:

MOD DIST Nom. value	Error max.	Sine carrier		Multi-sine			
		f_{RF}	f_{AF}	U3	U4	U5	U6
-40dB	± 0.5 dB	4kHz	500Hz	20	-140	-140	-140
-50dB	± 0.5 dB			10	-140	-140	-140
-60dB	± 0.5 dB			0	-140	-140	-140
-70dB	± 0.5 dB			-10	-140	-140	-140
-80dB	± 1.0 dB			-20	-140	-140	-140
-80dB	± 1.0 dB			-23	-140	-140	-140
-71dB	± 0.5 dB	7kHz	60Hz	-14	-20	-20	-140
-71dB	± 0.5 dB	15kHz	200Hz	-20	-20	-20	-20
-70dB	± 0.5 dB	20kHz	500Hz	-140	-140	-140	-10

- Inherent distortion MOD DIST

Test devices: two low-distortion sinewave generators (THD as with UPD LDG Generator), supply network 2

Test setup: see illustration on page 7.27

Measurement: Sinewave generator 1: different RF carrier frequencies
Sinewave generator 2: $Level = 4 * RF_{carrier}$, set different AF frequencies
UPD setting and measurement according to the test report
Measure MOD DIST and compare with nominal readout

Tolerance:

Upper Freq	Lower Freq	Readout	Analyzer
4kHz, 7kHz, 15kHz	30Hz	< -90dB	ANLG 22kHz
	200Hz	< -96dB	"
	500Hz	< -96dB	"
	20kHz	60Hz	< -85dB
20kHz	200Hz	< -96dB	"
	500Hz	< -96dB	"
	4kHz...100kHz	200Hz...500Hz	< -80dB
4kHz...100kHz	500Hz	< -80dB	ANLG 300kHz

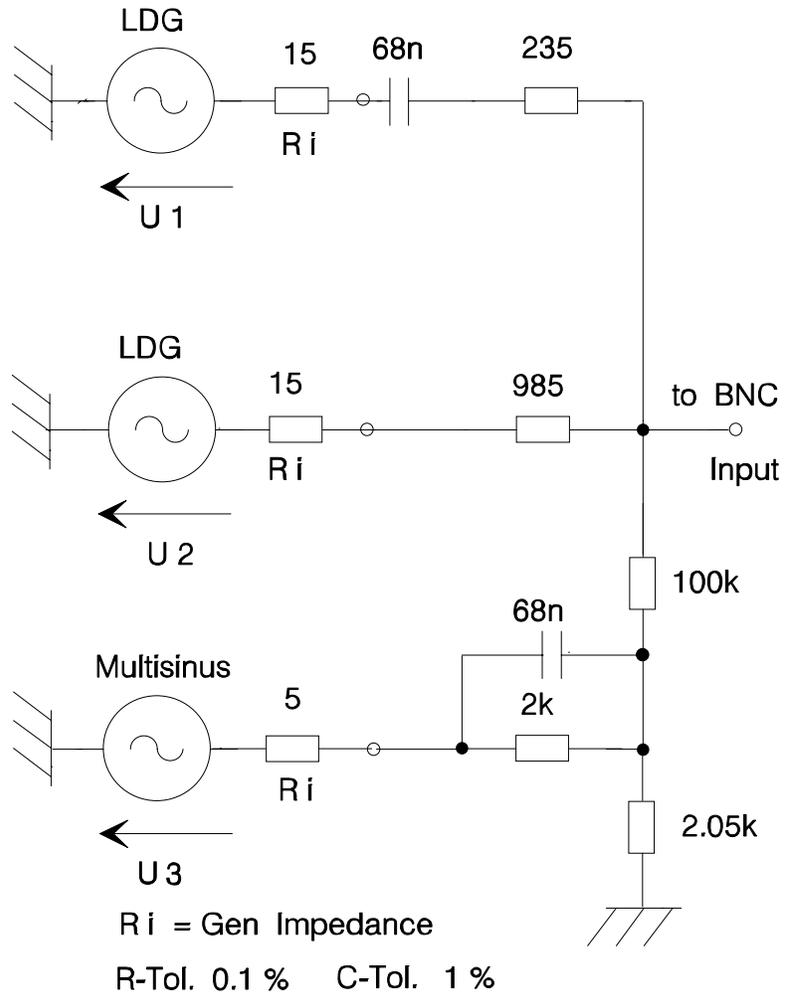
11. Difference frequency DFD

- Measuring accuracy DFD-d2

Analyzer setting	Instrument	ANLG 22kHz, 100kHz, 300kHz
	Channel(s)	1 \equiv 2
	Input	UNBAL
	Common	GROUND
	Range	FIX corresp. to measurement
	Function	DFD-d2

Test devices: two low-distortion sinewave generators (DFD-d2 and level accuracy as with UPD LDG Generator), multi-sine generator (frequency and level accuracy as with UPD Universal Generator), supply network 3

Test setup:



Signal: Sinewave generator 1: Level U_1 , different carrier frequencies $f_1 = \text{Mean_Freq} - \text{Diff_Freq}/2$
 Sinewave generator 2: Level $U_2 = U_1$, different carrier frequencies $f_2 = \text{Mean_Freq} + \text{Diff_Freq}/2$
 RMS value $V_{Total} = \sqrt{2} * U_2$
 Sinewave generator 3: with 46 dB attenuation, a sinewave is added, noise signal U_3 , $f_3 = \text{Diff_Freq}$, Ref-Volt = U_2 , U_3 in dB

Measurement: UPD setting and measurement according to the test report
Measure DFD-d2 and compare with nominal readout

Tolerance:

Mean Freq	Diff Freq	DFD-d2 Nom.	Error max.	U3 dBr	Setting
15kHz	100Hz	-80dB	±0.5dB	-34	ANLG 22kHz
	200Hz	-80dB	±0.5dB	-34	Range FIX 3V
	500Hz	-80dB	±0.5dB	-34	U1=U2 = 2.0V
	1000Hz	-80dB	±0.5dB	-34	U3-Ref = 2.0V
5kHz	800Hz	-46dB	±0.5dB	0	ANLG 22kHz
	700Hz	-60dB	±0.5dB	-14	Range FIX 1.8V
	600Hz	-70dB	±0.5dB	-24	U1=U2 = 2.0V
7kHz	500Hz	-84dB	±0.5dB	-38	U3-Ref = 2.0V
15kHz	400Hz	-100dB	±1.5dB	-54	
	100Hz	-80dB	±0.5dB	-34	
20kHz	200Hz	-90dB	±0.75dB	-44	
5kHz	200Hz	-90dB	±0.75dB	-44	ANLG 100kHz
20kHz	300Hz	-80dB	±0.5dB	-34	Range FIX 6V
50kHz	500Hz	-70dB	±0.75dB	-24	U1=U2 = 5.0V
90kHz	200Hz	-60dB	±0.75dB	-14	U3-Ref = 5.0V
7kHz	1000Hz	-80dB	±0.5dB	-34	ANLG 300kHz
15kHz	500Hz	-70dB	±0.5dB	-24	Range FIX 3V
75kHz	700Hz	-74dB	±0.75dB	-28	U1=U2 = 3.0V
100kHz	900Hz	-60dB	±0.75dB	-14	U3-Ref = 3.0V

NOTE: *Testing of the measuring accuracy of DFD-d3 is not required when servicing, since the proper functioning is ensured by the inherent distortion test DFD-d3 and the program algorithm of the UPD.*

- Inherent distortion DFD-d2

Analyzer setting	Instrument	ANLG 22kHz, 100kHz, 300kHz
	Channel(s)	1 ≡ 2
	Input	UNBAL
	Common	GROUND
	Range	FIX corresp. to measurement
	Function	DFD-d2
Generator setting	Instrument	ANLG 110kHz
	Output	UNBAL
	Impedance	15Ω
	Common	FLOAT
	Function	DFD
	Low Dist	ON
	Total Volt	see measurement
	Mean Freq	"
Diff Freq	"	

Test devices: Two-tone generator (inherent DFD-d2 as with UPD LDG Generator), DFD highpass

Measurement: Connect two-tone generator via a DFD highpass to the inputs of the UPD analyzer. The DFD highpass filter eliminates the influence of the inherent distortion of the generator. The generator level is to be increased by the attenuation value at Mean_Freq. The attenuation of the highpass filter in the passband does **not** affect the measurement. UPD setting and measurement according to the test report.

<u>Tolerance:</u>	Mean_Freq	Diff_Freq	Readout	Analyzer
	5kHz ... 20kHz	80Hz ... 1kHz	<-115dB	ANLG 22kHz
	5kHz ... 20kHz	200Hz ... 1kHz	<-110dB	ANLG 100kHz
	20kHz ... 50kHz	200Hz ... 1kHz	<-105dB	
	50kHz ... 100kHz	200Hz ... 1kHz	<-90dB	
	5kHz ... 20kHz	500Hz ... 1kHz	<-110dB	ANLG 300kHz
	20kHz ... 50kHz	500Hz ... 1kHz	<-105dB	
	50kHz ... 100kHz	500Hz ... 1kHz	<-90dB	

- Inherent distortion DFD-d3

Testing of the DFD-d3 inherent distortion is performed as loop measurement together with the Low Distortion Generator of the UPD (see section 7.3.5.2, page 7.159).

12. Dynamic intermodulation DIM

Testing of the DIM inherent distortion is performed as loop measurement together with the Low Distortion Generator of the UPD (see section 7.3.5.2, page 7.160).

NOTE: Further testing of the DIM measuring accuracy is not required when servicing, since the proper functioning is ensured by the inherent distortion test and the program algorithm of the UPD.

7.2.5.3 Test Protocol

measurement	min	act.	max	unit
Level Measurement RMS				
Level Accuracy at 1kHz				
Analyzer	ANLG 300kHz			
Channel(s)	1 ≡ 2			
Input	UNBAL			
Function	RMS			
Meas Time	AUTO			
Filter	OFF			
<i>measurement on ch. 1</i>				
Range FIX	input voltage	-Tol.	+Tol.	dB
1 mV	0.75 mV	-0.05	0.05	
3 mV	2.25 mV	-0.05	0.05	
10 mV	7.5 mV	-0.05	0.05	
30 mV	22.5 mV	-0.05	0.05	
100 mV	75 mV	-0.05	0.05	
300 mV	225 mV	-0.05	0.05	
1 V	0.75 V	-0.05	0.05	
1.8 V	1.35 V	-0.05	0.05	
3 V	2.25 V	-0.05	0.05	
6 V	4.5 V	-0.05	0.05	
10 V	7.5 V	-0.05	0.05	
18 V	13.5 V	-0.05	0.05	
30 V	22.5 V	-0.05	0.05	
60 V	45 V	-0.05	0.05	
100 V	75 V	-0.05	0.05	
180 V	135 V	-0.05	0.05	
300 V	225 V	-0.05	0.05	
<i>measurement on ch. 2</i>				
Range FIX	input voltage	-Tol.	+Tol.	dB
1 mV	0.75 mV	-0.05	0.05	
3 mV	2.25 mV	-0.05	0.05	
10 mV	7.5 mV	-0.05	0.05	
30 mV	22.5 mV	-0.05	0.05	
100 mV	75 mV	-0.05	0.05	
300 mV	225 mV	-0.05	0.05	
1 V	0.75 V	-0.05	0.05	
1.8 V	1.35 V	-0.05	0.05	
3 V	2.25 V	-0.05	0.05	
6 V	4.5 V	-0.05	0.05	
- continued -				

measurement		min	act.	max	unit
10 V	7.5 V	-0.05		0.05	
18 V	13.5 V	-0.05		0.05	
30 V	22.5 V	-0.05		0.05	
60 V	45 V	-0.05		0.05	
100 V	75 V	-0.05		0.05	
180 V	135 V	-0.05		0.05	
300 V	225 V	-0.05		0.05	
Analyzer	ANLG 300kHz				
Channel(s)	1 \equiv 2				
Input	BAL				
Impedance	20k Ω				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>					
Range FIX	input voltage	-Tol.		+Tol.	dB
1 mV	0.75 mV	-0.05		0.05	
3 mV	2.25 mV	-0.05		0.05	
10 mV	7.5 mV	-0.05		0.05	
30 mV	22.5 mV	-0.05		0.05	
100 mV	75 mV	-0.05		0.05	
300 mV	225 mV	-0.05		0.05	
1 V	0.75 V	-0.05		0.05	
1.8 V	1.35 V	-0.05		0.05	
3 V	2.25 V	-0.05		0.05	
6 V	4.5 V	-0.05		0.05	
10 V	7.5 V	-0.05		0.05	
18 V	13.5 V	-0.05		0.05	
30 V	22.5 V	-0.05		0.05	
<i>measurement on ch. 2</i>					
Range FIX	input voltage	-Tol.		+Tol.	dB
1 mV	0.75 mV	-0.05		0.05	dB
3 mV	2.25 mV	-0.05		0.05	
10 mV	7.5 mV	-0.05		0.05	
30 mV	22.5 mV	-0.05		0.05	
100 mV	75 mV	-0.05		0.05	
300 mV	225 mV	-0.05		0.05	
1 V	0.75 V	-0.05		0.05	
1.8	1.35 V	-0.05		0.05	
3 V	2.25 V	-0.05		0.05	
6 V	4.5 V	-0.05		0.05	
10 V	7.5 V	-0.05		0.05	
18 V	13.5 V	-0.05		0.05	
30 V	22.5 V	-0.05		0.05	
Analyzer	ANLG 100kHz				

- continued -

measurement		min	act.	max	unit
Channel(s)	1 ≡ 2				
Input	UNBAL				
Range	AUTO				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>		-Tol.		+Tol.	
input voltage	3 V	-0.05		0.05	dB
<i>measurement on ch. 2</i>		-Tol.		+Tol.	
input voltage	3 V	-0.05		0.05	dB
Analyzer	ANLG 22kHz				
Channel(s)	1 ≡ 2				
Input	UNBAL				
Range	AUTO				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>		-Tol.		+Tol.	
input voltage	3 V	-0.05		0.05	dB
<i>measurement on ch. 2</i>		-Tol.		+Tol.	
input voltage	3 V	-0.05		0.05	dB
linearity					
Analyzer	ANLG 22kHz				
Channel(s)	1 ≡ 2				
Input	UNBAL				
Range	FIX 1V				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>		-Tol.		+Tol.	
input signal	Voltage	-Tol.		+Tol.	%
1 kHz	0.1 V.	-0.25		0.25	
	0.2 V.	-0.25		0.25	
	0.3 V	-0.1		0.1	
	0.4 V	-0.1		0.1	
	0.5 V	-0.1		0.1	
	0.7 V	-0.1		0.1	
	1 V	-0.1		0.1	
	1.15 V	-0.1		0.1	
<i>measurement on ch. 2</i>		-Tol.		+Tol.	
input signal	Voltage	-Tol.		+Tol.	%
1 kHz	0.1 V.	-0.25		0.25	
	0.2 V.	-0.25		0.25	
	0.3 V	-0.1		0.1	
	0.4 V	-0.1		0.1	

- continued -

measurement		min	act.	max	unit
	0.5 V	-0.1		0.1	
	0.7 V	-0.1		0.1	
	1 V	-0.1		0.1	
	1.15 V	-0.1		0.1	
Analyzer	ANLG 100kHz				
Channel(s)	1 \equiv 2				
Input	UNBAL				
Range	FIX 1V				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>					
input signal	Voltage	-Tol.		+Tol.	%
20 kHz	0.1 V	-0.25		0.25	
	0.2 V	-0.25		0.25	
	0.3 V	-0.1		0.1	
	0.4 V	-0.1		0.1	
	0.5 V	-0.1		0.1	
	0.7 V	-0.1		0.1	
	1 V	-0.1		0.1	
	1.15 V	-0.1		0.1	
<i>measurement on ch. 2</i>					
input signal	Voltage	-Tol.		+Tol.	%
20 kHz	0.1 V	-0.25		0.25	
	0.2 V	-0.25		0.25	
	0.3 V	-0.1		0.1	
	0.4 V	-0.1		0.1	
	0.5 V	-0.1		0.1	
	0.7 V	-0.1		0.1	
	1 V	-0.1		0.1	
	1.15 V	-0.1		0.1	
frequency response					
Analyzer	ANLG 22kHz				
Channel(s)	1 \equiv 2				
Range	FIX 3V				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>					
Min Freq	2 Hz				
Input	UNBAL				
input signal	Freq	-Tol.		+Tol.	dB
2.25 V	2 Hz	-0.5		0.5	
	5 Hz	-0.5		0.5	
	20 Hz	-0.03		0.03	

- continued -

measurement		min	act.	max	unit
Min Freq Input Impedance input signal 2.25 V	2 Hz				
	BAL				
	20kΩ				
	Freq	-Tol.		+Tol.	dB
	2 Hz	-0.5		0.5	
	5 Hz	-0.5		0.5	
	20 Hz	-0.03		0.03	
Min Freq Input input signal 2.25 V	10 Hz				
	UNBAL				
	Freq	-Tol.		+Tol.	dB
	10 Hz	-0.15		0.15	
	20 Hz	-0.03		0.03	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	2 kHz	-0.03		0.03	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	20 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
Min Freq Input Impedance input signal 2.25 V	10 Hz				
	BAL				
	20kΩ				
	Freq	-Tol.		+Tol.	dB
	10 Hz	-0.15		0.15	
	20 Hz	-0.03		0.03	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	2 kHz	-0.03		0.03	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	20 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
<i>measurement on ch. 2</i>					
Min Freq Input input signal 2.25 V	2 Hz				
	UNBAL				
	Freq	-Tol.		+Tol.	dB
	2 Hz	-0.5		0.5	
	5 Hz	-0.5		0.5	
	20 Hz	-0.03		0.03	

- continued -

measurement		min	act.	max	unit
Min Freq	2 Hz				
Input	BAL				
Impedance	20k Ω				
input signal	Freq	-Tol.		+Tol.	dB
2.25 V	2 Hz	-0.5		0.5	
	5 Hz	-0.5		0.5	
	20 Hz	-0.03		0.03	
Min Freq	10 Hz				
Input	UNBAL				
input signal	Freq	-Tol.		+Tol.	dB
2.25 V	10 Hz	-0.15		0.15	
	20 Hz	-0.03		0.03	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	2 kHz	-0.03		0.03	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	20 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
Min Freq	10 Hz				
Input	BAL				
Impedance	20k Ω				
input signal	Freq	-Tol.		+Tol.	dB
2.25 V	10 Hz	-0.15		0.15	
	20 Hz	-0.03		0.03	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	2 kHz	-0.03		0.03	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	20 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
Analyzer	ANLG 100kHz				
Channel(s)	1 \equiv 2				
Input	UNBAL				
Range	FIX 3V				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>					
input signal	Freq	-Tol.		+Tol.	dB

- continued -

measurement		min	act.	max	unit
2.25 V	20 Hz	-0.03		0.03	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	2 kHz	-0.03		0.03	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	30 kHz	-0.1		0.1	
	50 kHz	-0.1		0.1	
	70 kHz	-0.2		0.2	
100 kHz	-0.2		0.2		
<i>measurement on ch. 2</i>					
input signal	Freq	-Tol.		+Tol.	dB
2.25 V	20 Hz	-0.03		0.03	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	2 kHz	-0.03		0.03	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	30 kHz	-0.1		0.1	
	50 kHz	-0.1		0.1	
	70 kHz	-0.2		0.2	
100 kHz	-0.2		0.2		
Analyzer	ANLG 300kHz				
Channel(s)	1 ≡ 2				
Function	RMS				
Meas Time	AUTO				
Filter	OFF				
<i>measurement on ch. 1</i>					
Input	UNBAL				dB
Range FIX	10 mV				
input signal	Freq	-Tol.		+Tol.	
7.5 mV	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	40 kHz	-0.1		0.1	
	50 kHz	-0.1		0.1	
	80 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
	200 kHz	-1.0		1.0	
300 kHz	-1.0		1.0		
					- continued -

measurement		min	act.	max	unit
Range FIX input signal 22.5 mV	30 mV				
	Freq	-Tol.		+Tol.	dB
	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	50 kHz	-0.1		0.1	
	80 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
200 kHz	-1.0		1.0		
300 kHz	-1.0		1.0		
Range FIX input signal 75 mV	100 mV				
	Freq	-Tol.		+Tol.	dB
	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	50 kHz	-0.1		0.1	
	100 kHz	-0.2		0.2	
	200 kHz	-1.0		1.0	
	300 kHz	-1.0		1.0	
Range FIX input signal 225 mV	300 mV				
	Freq	-Tol.		+Tol.	dB
	50 Hz	-0.05		0.05	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	50 kHz	-0.1		0.1	
	80 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
	300 kHz	-1.0		1.0	
Range FIX input signal 0.75 V	1 V				
	Freq	-Tol.		+Tol.	dB
	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
5 kHz	-0.03		0.03		

- continued -

measurement		min	act.	max	unit	
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	70 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
	Range FIX input signal 1.35 V	1.8 V Freq	-Tol.			+Tol.
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	100 kHz	-0.2		0.2		
	300 kHz	-1.0		1.0		
Range FIX input signal 2.25 V	3 V Freq	-Tol.		+Tol.	dB	
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	70 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
Range FIX input signal 4.5 V	6 V Freq	-Tol.		+Tol.		dB
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	100 kHz	-0.2		0.2		
	300 kHz	-1.0		1.0		

- continued -

measurement		min	act.	max	unit
Range FIX	30 V				
input signal	Freq	-Tol.		+Tol.	dB
22.5 V	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	50 kHz	-0.1		0.1	
	70 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
	200 kHz	-1.0		1.0	
	300 kHz	-1.0		1.0	
Range FIX	180 V				
input signal	Freq	-Tol.		+Tol.	dB
135 V	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	50 kHz	-0.1		0.1	
	70 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
	200 kHz	-1.0		1.0	
	300 kHz	-1.0		1.0	
<i>measurement on ch. 2</i>					
Input	UNBAL				
Range FIX	10 mV				
input signal	Freq	-Tol.		+Tol.	dB
7.5 mV	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	15 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	40 kHz	-0.1		0.1	
	50 kHz	-0.1		0.1	
	80 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
	200 kHz	-1.0		1.0	
	300 kHz	-1.0		1.0	
Range FIX	30 mV				

- continued -

measurement		min	act.	max	unit	
input signal 22.5 mV	Freq	-Tol.		+Tol.	dB	
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	15 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	80 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
	Range FIX input signal 75 mV	100 mV Freq	-Tol.			+Tol.
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
Range FIX input signal 225 mV	300 mV Freq	-Tol.		+Tol.	dB	
	50 Hz	-0.05		0.05		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	15 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	80 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	300 kHz	-1.0		1.0		
Range FIX input signal 0.75 V	1 V Freq	-Tol.		+Tol.		dB
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		

- continued -

measurement		min	act.	max	unit	
	50 kHz	-0.1		0.1		
	70 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
Range FIX input signal 1.35 V	1.8 V Freq	-Tol.		+Tol.	dB	
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	100 kHz	-0.2		0.2		
	300 kHz	-1.0		1.0		
Range FIX input signal 2.25 V	3 V Freq	-Tol.		+Tol.		dB
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	70 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
Range FIX input signal 4.5 V	6 V Freq	-Tol.		+Tol.	dB	
	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	100 kHz	-0.2		0.2		
	300 kHz	-1.0		1.0		
Range FIX input signal	30 V Freq	-Tol.		+Tol.		dB

- continued -

measurement		min	act.	max	unit	
22.5 V	50 Hz	-0.05		0.05	dB	
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	70 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
	Range FIX	180 V				
	input signal	Freq	-Tol.			+Tol.
	135 V	50 Hz	-0.05			0.05
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	70 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		
	200 kHz	-1.0		1.0		
	300 kHz	-1.0		1.0		
Analyzer	ANLG 300kHz					
Channel(s)	1 ≡ 2					
Input	BAL					
Impedance	20kΩ					
Function	RMS					
Meas Time	AUTO					
Filter	OFF					
<i>measurement on ch. 1</i>						
Input	BAL				dB	
Range FIX	3 V					
input signal	Freq	-Tol.		+Tol.		
2.25 V	50 Hz	-0.05		0.05		
	100 Hz	-0.03		0.03		
	1 kHz	0		0		
	5 kHz	-0.03		0.03		
	10 kHz	-0.03		0.03		
	22 kHz	-0.03		0.03		
	50 kHz	-0.1		0.1		
	70 kHz	-0.2		0.2		
	100 kHz	-0.2		0.2		

- continued -

measurement		min	act.	max	unit		
Range FIX input signal 7.5 V	200 kHz	-1.0		1.0	dB		
	300 kHz	-1.0		1.0			
	10 V Freq	-Tol.		+Tol.			
	50 Hz	-0.05		0.05			
	100 Hz	-0.03		0.03			
	1 kHz	0		0			
	5 kHz	-0.03		0.03			
	10 kHz	-0.03		0.03			
	22 kHz	-0.03		0.03			
	50 kHz	-0.1		0.1			
	70 kHz	-0.2		0.2			
	100 kHz	-0.2		0.2			
	200 kHz	-1.0		1.0			
	300 kHz	-1.0		1.0			
	Range FIX input signal 13.5 V	18 V Freq	-Tol.			+Tol.	dB
50 Hz		-0.05		0.05			
100 Hz		-0.03		0.03			
1 kHz		0		0			
5 kHz		-0.03		0.03			
10 kHz		-0.03		0.03			
22 kHz		-0.03		0.03			
50 kHz		-0.1		0.1			
70 kHz		-0.2		0.2			
100 kHz		-0.2		0.2			
200 kHz		-1.0		1.0			
300 kHz		-1.0		1.0			
<i>measurement on ch. 2</i>							
Input		BAL					
Range FIX		3 V					
input signal	Freq	-Tol.		+Tol.	dB		
2.25 V	50 Hz	-0.05		0.05			
	100 Hz	-0.03		0.03			
	1 kHz	0		0			
	5 kHz	-0.03		0.03			
	10 kHz	-0.03		0.03			
	22 kHz	-0.03		0.03			
	50 kHz	-0.1		0.1			
	70 kHz	-0.2		0.2			
	100 kHz	-0.2		0.2			
	200 kHz	-1.0		1.0			
	300 kHz	-1.0		1.0			

- continued -

measurement		min	act.	max	unit
Range FIX	10 V				
input signal	Freq	-Tol.		+Tol.	dB
7.5 V	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	50 kHz	-0.1		0.1	
	70 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
	200 kHz	-1.0		1.0	
	300 kHz	-1.0		1.0	
Range FIX	18 V				
input signal	Freq	-Tol.		+Tol.	dB
13.5 V	50 Hz	-0.05		0.05	
	100 Hz	-0.03		0.03	
	1 kHz	0		0	
	5 kHz	-0.03		0.03	
	10 kHz	-0.03		0.03	
	22 kHz	-0.03		0.03	
	50 kHz	-0.1		0.1	
	70 kHz	-0.2		0.2	
	100 kHz	-0.2		0.2	
	200 kHz	-1.0		1.0	
	300 kHz	-1.0		1.0	
Intrinsic Noise					
Analyzer	ANLG 22kHz				
Min Freq	10 Hz				
Channel(s)	1 ≡ 2				
Input	UNBAL				
Range	FIX 30 mV				
Function	RMS				
Meas Time	FAST				
Filter	CCIR UNWTD				
<i>measurement on ch. 1</i>				2	μV
<i>measurement on ch. 2</i>				2	μV
Function	QPEAK				
Meas Time	SLOW				
Filter	CCIR WTD				
<i>measurement on ch. 1</i>				8	μV
- continued -					

measurement		min	act.	max	unit
<i>measurement on ch. 2</i>				8	μV
Input	BAL				
Impedance	300 Ω				
Function	RMS				
Meas Time	FAST				
Filter	CCIR UNWTD				
<i>measurement on ch. 1</i>				2	μV
<i>measurement on ch. 2</i>				2	μV
Input	BAL				
Impedance	300 Ω				
Function	QPEAK				
Meas Time	SLOW				
Filter	CCIR WTD				
<i>measurement on ch. 1</i>				8	μV
<i>measurement on ch. 2</i>				8	μV
input resistance					
Analyzer	ANLG 22kHz				
Min Freq	2 Hz				
Channel(s)	1 \equiv 2				
Input	UNBAL				
Range	FIX 30 V				
<i>measurement on ch. 1</i>		1.00		1.015	M Ω
<i>measurement on ch. 2</i>		1.00		1.015	M Ω
Input	BAL				
<i>measurement on ch. 1</i>					
Impedance	300 Ω	298.5		301.5	Ω
	600 Ω	597		603	Ω
	20k Ω	19.10		20.10	k Ω
<i>measurement on ch. 2</i>					
Impedance	300 Ω	298.5		301.5	Ω
	600 Ω	597		603	Ω
	20k Ω	19.10		20.10	k Ω
crosstalk attenuation					
Analyzer	ANLG 22kHz				
Min Freq	10 Hz				
Channel(s)	1 & 2				
Input	UNBAL				
Range	AUTO				
input signal	20kHz, 2.25 V				
crosstalk	channel 1 \rightarrow 2			-130	dB
- continued -					

measurement		min	act.	max	unit
crosstalk	channel 2 → 1			-130	dB
Input Impedance	BAL 600Ω				
crosstalk	channel 1 → 2			-130	dB
crosstalk	channel 2 → 1			-130	dB
common mode attenuation					
Analyzer	ANLG 22kHz				
Min Freq	10 Hz				
Channel(s)	1 ≡ 2				
Input Impedance	BAL 20kΩ				
Range	AUTO				
<i>measurement on ch. 1</i>					
input signal	50 Hz. 10 V			-110	dB
	1 kHz			-85	dB
	16 kHz			-60	dB
<i>measurement on ch. 2</i>					
input signal	50 Hz. 10 V			-110	dB
	1 kHz			-85	dB
	16 kHz			-60	dB
Min Freq	2 Hz				
<i>measurement on ch. 1</i>					
input signal	50 Hz. 10 V			-110	dB
<i>measurement on ch. 2</i>					
input signal	50 Hz. 10 V			-110	dB
frequency measurement					
Analyzer	ANLG 22kHz				
Min Freq	2 Hz				
Channel(s)	1 ≡ 2				
Input	UNBAL				
Range	FIX 1V				
Freq/Phase	FREQ 'COUNTER'				
Meas Time	FAST				
<i>measurement on ch. 1</i>					
input signal	Freq	-Tol.		+Tol.	ppm
1 V	2 Hz	-50		50	
	10 Hz	-50		50	
	1 kHz	-50		50	
	300 kHz	-50		50	
0.3 V	2 Hz	-50		50	
	10 Hz	-50		50	
- continued -					

measurement		min	act.	max	unit		
0.1 V	1 kHz	-50		50			
	300 kHz	-50		50			
	2 Hz	-50		50			
	10 Hz	-50		50			
	100 Hz	-50		50			
	1 kHz	-50		50			
	300 kHz	-50		50			
<i>measurement on ch. 2</i>							
input signal	Freq	-Tol.		+Tol.	ppm		
1 V	2 Hz	-50		50			
	10 Hz	-50		50			
	1 kHz	-50		50			
	300 kHz	-50		50			
	0.3 V	2 Hz	-50			50	
0.3 V	10 Hz	-50		50			
	1 kHz	-50		50			
	300 kHz	-50		50			
	0.1 V	2 Hz	-50			50	
	0.1 V	10 Hz	-50			50	
100 Hz		-50		50			
1 kHz		-50		50			
300 kHz		-50		50			
Min Freq		2 Hz					
<i>measurement on ch. 1</i>							
input signal	Freq	-Tol.		+Tol.	ppm		
1 V	10 Hz	-50		50			
	100 Hz	-50		50			
	500 Hz	-50		50			
	1 kHz	-50		50			
	5 kHz	-50		50			
	10 kHz	-50		50			
	50 kHz	-50		50			
	100 kHz	-50		50			
	150 kHz	-50		50			
	200 kHz	-50		50			
	300 kHz	-50		50			
	input signal	Freq	-Tol.			+Tol.	ppm
	0.3 V	10 Hz	-50			50	
		100 Hz	-50			50	
500 Hz		-50		50			
1 kHz		-50		50			
5 kHz		-50		50			
10 kHz		-50		50			
	50 kHz	-50		50			
	100 kHz	-50		50			

- continued -

measurement		min	act.	max	unit		
input signal 0.1 V	150 kHz	-50		50	ppm		
	200 kHz	-50		50			
	300 kHz	-50		50			
	Freq	-Tol.		+Tol.			
	10 Hz	-50		50			
	100 Hz	-50		50			
	500 Hz	-50		50			
	1 kHz	-50		50			
	5 kHz	-50		50			
	10 kHz	-50		50			
	50 kHz	-50		50			
	100 kHz	-50		50			
	150 kHz	-50		50			
	200 kHz	-50		50			
	300 kHz	-50		50			
<i>measurement on ch. 2</i>							
input signal 1 V	Freq	-Tol.		+Tol.	ppm		
	10 Hz	-50		50			
	100 Hz	-50		50			
	500 Hz	-50		50			
	1 kHz	-50		50			
	5 kHz	-50		50			
	10 kHz	-50		50			
	50 kHz	-50		50			
	100 kHz	-50		50			
	150 kHz	-50		50			
	200 kHz	-50		50			
	300 kHz	-50		50			
	input signal 0.3 V	Freq	-Tol.			+Tol.	ppm
		10 Hz	-50			50	
		100 Hz	-50			50	
500 Hz		-50		50			
1 kHz		-50		50			
5 kHz		-50		50			
10 kHz		-50		50			
50 kHz		-50		50			
100 kHz		-50		50			
150 kHz		-50		50			
200 kHz		-50		50			
300 kHz		-50		50			
input signal 0.1 V		Freq	-Tol.		+Tol.	ppm	
		10 Hz	-50		50		
		100 Hz	-50		50		
	500 Hz	-50		50			
	1 kHz	-50		50			

- continued -

measurement		min	act.	max	unit
5 kHz		-50		50	
10 kHz		-50		50	
50 kHz		-50		50	
100 kHz		-50		50	
150 kHz		-50		50	
200 kHz		-50		50	
300 kHz		-50		50	
phase measurement					
phase coherence of both channels					
Analyzer	ANLG 22kHz				
Channel(s)	1 ≡ 2				
Freq/Phase	PHASE				
Meas Time	FAST				
Function	OFF				
Min Freq	2 Hz				
Input	BAL				
Range FIX	1 V				
input signal	Freq				
0.75 V	2 Hz	-1.0		1.0	°
	10 Hz	-1.0		1.0	°
Min Freq	2 Hz				
Input	UNBAL				
Range FIX	1 V				
input signal	Freq				
0.75 V	2 Hz	-1.0		1.0	°
	10 Hz	-1.0		1.0	°
Min Freq	10 Hz				
Input	BAL				
Range FIX	1 V				
input signal	Freq				
0.75 V	10 Hz	-1.0		1.0	°
	15 Hz	-1.0		1.0	°
	20 Hz	-1.0		1.0	°
Min Freq	10 Hz				
Input	UNBAL				
Range FIX	1 V				
input signal	Freq				
0.75 V	10 Hz	-1.0		1.0	°
	15 Hz	-1.0		1.0	°
	20 Hz	-0.4		0.4	°
Analyzer	ANLG 100kHz				
Input	BAL				
- continued -					

measurement		min	act.	max	unit
Range FIX	30 mV				
input signal	Freq				°
22.5 mV	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	300 mV				
input signal	Freq				°
225 mV	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	1 V				
input signal	Freq				°
0.75 V	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	1.8 V				
input signal	Freq				°
1.35 V	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	3 V				

- continued -

measurement		min	act.	max	unit
input signal 2.25 V	Freq				°
	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	6 V				
input signal 4.5 V	Freq				°
	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	10 V				
input signal 7.5 V	Freq				°
	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	30 V				
input signal 22.5 V	Freq				°
	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Input	UNBAL				
Range FIX	10 V				

- continued -

measurement		min	act.	max	unit
input signal 7.5 V	Freq				°
	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
Range FIX	100 V				
input signal 75 V	Freq				°
	20 Hz	-0.4		0.4	
	100 Hz	-0.4		0.4	
	1 kHz	-0.4		0.4	
	5 kHz	-0.4		0.4	
	10 kHz	-0.4		0.4	
	22 kHz	-0.4		0.4	
	50 kHz	-1.75		1.75	
	70 kHz	-1.75		1.75	
	100 kHz	-1.75		1.75	
phase measurement accuracy					
Analyzer	ANLG 100kHz				
Channel(s)	1 ≡ 2				
Input	UNBAL				
Range FIX	1 V				
Freq/Phase	PHASE				
Meas Time	FAST				
Function	OFF				
input signal	20Hz. 2 V	-Tol.		+Tol.	°
Phase (2 → 1)	-179°	-0.4		0.4	°
	-90°	-0.4		0.4	°
	0°	-0.4		0.4	°
	90°	-0.4		0.4	°
	179°	-0.4		0.4	°
input signal	200Hz. 2 V	-Tol.		+Tol.	°
Phase (2 → 1)	-179°	-0.4		0.4	°
	-90°	-0.4		0.4	°
	0°	-0.4		0.4	°
	90°	-0.4		0.4	°
	179°	-0.4		0.4	°
input signal	22 kHz. 2 V	-Tol.		+Tol.	°
Phase (2 → 1)	-135°	-0.4		0.4	°
	-45°	-0.4		0.4	°
	0°	-0.4		0.4	°

- continued -

measurement	min	act.	max	unit
input signal Phase (2 → 1)	45°	-0.4	0.4	°
	135°	-0.4	0.4	°
	100 kHz. 2 V	-Tol.	+Tol.	
	-135°	-1.75	1.75	°
	-45°	-1.75	1.75	°
	0°	-1.75	1.75	°
	45°	-1.75	1.75	°
	135°	-1.75	1.75	°
DC measurement				
offset voltage				
Analyzer	ANLG 300kHz			
Channel(s)	1 ≡ 2			
Function	DC			
Meas Time	FAST			
<i>measurement on ch. 1</i>				
Input	BAL			
Range FIX	input voltage			
100 mV	0 V	-2	2	mV
300 mV		-2	2	mV
1 V		-2	2	mV
3 V		-10	10	mV
10 V		-10	10	mV
30 V		-10	10	mV
Input	UNBAL			
Range FIX	input voltage			
100 mV	0 V	-2	2	mV
300 mV		-2	2	mV
1 V		-2	2	mV
3 V		-10	10	mV
10 V		-10	10	mV
30 V		-10	10	mV
100 V		-30	30	mV
300 V		-30	30	mV
<i>measurement on ch. 2</i>				
Input	BAL			
Range FIX	input voltage			
100 mV	0 V	-2	2	mV
300 mV		-2	2	mV
1 V		-2	2	mV
3 V		-10	10	mV
10 V		-10	10	mV
30 V		-10	10	mV
Input	UNBAL			
- continued -				

measurement		min	act.	max	unit
Range FIX	input voltage				
100 mV	0 V	-2		2	mV
300 mV		-2		2	mV
1 V		-2		2	mV
3 V		-10		10	mV
10 V		-10		10	mV
30 V		-10		10	mV
100 V		-30		30	mV
300 V		-30		30	mV
DC measurement accuracy					
Analyzer	ANLG 300kHz				
Channel(s)	1 ≡ 2				
Range	FIX 3V				
Function	DC				
Meas Time	FAST				
<i>measurement on ch. 1</i>					
Input	BAL	-Tol.		+Tol.	%
input voltage	+4.5 V	-0.5		0.5	
	-4.5 V	-0.5		0.5	
	+3.0 V	-0.2		0.2	
	-3.0 V	-0.2		0.2	
	+2.5 V	-0.2		0.2	
	-2.5 V	-0.2		0.2	
	+2.0 V	-0.2		0.2	
	-2.0 V	-0.2		0.2	
	+1.5 V	-0.2		0.2	
	-1.5 V	-0.2		0.2	
	+1.0 V	-0.3		0.3	
	-1.0 V	-0.3		0.3	
	+0.5 V	-0.4		0.4	
	-0.5 V	-0.4		0.4	
	+0.3 V	-0.5		0.5	
	-0.3 V	-0.5		0.5	
Input	UNBAL	-Tol.		+Tol.	%
input voltage	+4.5 V	-0.5		0.5	
	-4.5 V	-0.5		0.5	
	+3.0 V	-0.2		0.2	
	-3.0 V	-0.2		0.2	
	+2.5 V	-0.2		0.2	
	-2.5 V	-0.2		0.2	
	+2.0 V	-0.2		0.2	
	-2.0 V	-0.2		0.2	
	+1.5 V	-0.2		0.2	
	-1.5 V	-0.2		0.2	
	+1.0 V	-0.3		0.3	
- continued -					

measurement		min	act.	max	unit
	-1.0 V	-0.3		0.3	
	+0.5 V	-0.4		0.4	
	-0.5 V	-0.4		0.4	
	+0.3 V	-0.5		0.5	
	-0.3 V	-0.5		0.5	
<i>measurement on ch. 1</i>					
Input	BAL	-Tol.		+Tol.	%
input voltage	+4.5 V	-0.5		0.5	
	-4.5 V	-0.5		0.5	
	+3.0 V	-0.2		0.2	
	-3.0 V	-0.2		0.2	
	+2.5 V	-0.2		0.2	
	-2.5 V	-0.2		0.2	
	+2.0 V	-0.2		0.2	
	-2.0 V	-0.2		0.2	
	+1.5 V	-0.2		0.2	
	-1.5 V	-0.2		0.2	
	+1.0 V	-0.3		0.3	
	-1.0 V	-0.3		0.3	
	+0.5 V	-0.4		0.4	
	-0.5 V	-0.4		0.4	
	+0.3 V	-0.5		0.5	
	-0.3 V	-0.5		0.5	
Input	UNBAL	-Tol.		+Tol.	%
input voltage	+4.5 V	-0.5		0.5	
	-4.5 V	-0.5		0.5	
	+3.0 V	-0.2		0.2	
	-3.0 V	-0.2		0.2	
	+2.5 V	-0.2		0.2	
	-2.5 V	-0.2		0.2	
	+2.0 V	-0.2		0.2	
	-2.0 V	-0.2		0.2	
	+1.5 V	-0.2		0.2	
	-1.5 V	-0.2		0.2	
	+1.0 V	-0.3		0.3	
	-1.0 V	-0.3		0.3	
	+0.5 V	-0.4		0.4	
	-0.5 V	-0.4		0.4	
	+0.3 V	-0.5		0.5	
	-0.3 V	-0.5		0.5	
Total Harmonic Distortion					
THD measurement accuracy					
Analyzer	ANLG 22kHz				
- continued -					

measurement		min	act.	max	unit
Min Freq	10 Hz				
Channel(s)	1 ≡ 2				
Input	UNBAL				
Range	FIX 3V				
<i>measurement on ch. 1</i>					
input signal	9 kHz. 2 V				
harmonic d2	-50 dB	-50.5		-49.5	dB
	-80 dB	-80.5		-79.5	
	-85 dB	-85.75		-84.25	
	-90 dB	-91.0		-89.0	
<i>measurement on ch. 2</i>					
input signal	9 kHz. 2 V				
harmonic d2	-50 dB	-50.5		-49.5	dB
	-80 dB	-80.5		-79.5	
	-85 dB	-85.75		-84.25	
	-90 dB	-91.0		-89.0	
<i>Analyzer ANLG 100kHz</i>					
<i>measurement on ch. 1</i>					
input signal	25 kHz. 2 V				
harmonic d2	-60 dB	-60.5		-59.5	dB
	-70 dB	-70.5		-69.5	
	-75 dB	-75.5		-75.5	
	-80 dB	-81.0		-79.0	
<i>measurement on ch. 2</i>					
input signal	25 kHz. 2 V				
harmonic d2	-60 dB	-60.5		-59.5	dB
	-70 dB	-70.5		-69.5	
	-75 dB	-75.5		-74.5	
	-80 dB	-81.0		-79.0	
<i>Analyzer ANLG 300kHz</i>					
<i>measurement on ch. 1</i>					
input signal	50 kHz. 2 V				
harmonic d2	-50 dB	-50.5		-49.5	dB
	-65 dB	-65.5		-64.5	
	-70 dB	-70.75		-69.25	
	-75 dB	-75.5		-74.5	
	-80 dB	-81.5		-78.5	
<i>measurement on ch. 2</i>					
input signal	50 kHz. 2 V				
harmonic d2	-50 dB	-50.5		-49.5	dB
	-65 dB	-65.5		-64.5	
	-70 dB	-70.75		-69.25	
	-75 dB	-75.5		-74.5	
	-80 dB	-81.5		-78.5	
<i>measurement on ch. 1</i>					

- continued -

measurement		min	act.	max	unit	
harmonic d2	-60 dB					
input signal 2 V	Freq f_0					
	100 Hz	-60.5		-59.5	dB	
	1 kHz	-60.5		-59.5		
	7 kHz	-60.5		-59.5		
	20 kHz	-60.5		-59.5		
	30 kHz	-60.5		-59.5		
	40 kHz	-60.5		-59.5		
	50 kHz	-60.5		-59.5		
<i>measurement on ch. 2</i>						
harmonic d2	-60 dB					
input signal 2 V	Freq f_0					
	100 Hz	-60.5		-59.5	dB	
	1 kHz	-60.5		-59.5		
	7 kHz	-60.5		-59.5		
	20 kHz	-60.5		-59.5		
	30 kHz	-60.5		-59.5		
	40 kHz	-60.5		-59.5		
	50 kHz	-60.5		-59.5		
Intermodulation MOD DIST						
MOD DIST measurement accuracy						
Analyzer	ANLG 22kHz					
Min Freq	10 Hz					
Channel(s)	1 \equiv 2					
Input	UNBAL					
Range	FIX 3V					
<i>measurement on ch. 1</i>						
input signal	dist.					
$U_{RF} = 0.7V$	TRUE					
f_{RF}	f_{AF}				dB	
4kHz	500Hz	-40 dB	-40.5	-39.5		
	500Hz	-50 dB	-50.5	-49.5		
	500Hz	-60 dB	-60.5	-59.5		
	500Hz	-70 dB	-70.5	-69.5		
	500Hz	-80 dB	-81	-79		
	500Hz	-80 dB	-81	-79		
7kHz	60Hz	-71 dB	-71.5	-70.5		
15kHz	200Hz	-71 dB	-71.5	-70.5		
20kHz	500Hz	-70 dB	-70.5	-69.5		
<i>measurement on ch. 2</i>						
input signal	dist.					
$U_{RF} = 0.7V$	TRUE					
f_{RF}	f_{AF}				dB	

- continued -

measurement		min	act.	max	unit	
4kHz	500Hz -40 dB	-40.5		-39.5		
	500Hz -50 dB	-50.5		-49.5		
	500Hz -60 dB	-60.5		-59.5		
	500Hz -70 dB	-70.5		-69.5		
	500Hz -80 dB	-81		-79		
	500Hz -80 dB	-81		-79		
7kHz	60Hz -71 dB	-71.5		-70.5		
15kHz	200Hz -71 dB	-71.5		-70.5		
20kHz	500Hz -70 dB	-70.5		-69.5		
MOD DIST intrinsic distortion						
Analyzer	ANLG 22kHz					
Min Freq	10 Hz					
Channel(s)	1 ≡ 2					
Input	UNBAL					
<i>measurement on ch. 1</i>						
Range	FIX 6V					
input signal	$V_{rms} = 5V$					
f_{HF}	f_{NF}					
4kHz	30Hz			-90	dB	
	200Hz			-96		
	500Hz			-96		
7kHz	30Hz			-90		
	200Hz			-96		
	500Hz			-96		
15kHz	30Hz			-85		
	200Hz			-96		
	500Hz			-96		
20kHz	60Hz			-85		
	200Hz			-96		
	500Hz			-96		
Range	FIX 3V					
input signal	$V_{rms} = 3V$					
f_{RF}	f_{AF}					
4kHz	30Hz			-90	dB	
	200Hz			-96		
	500Hz			-96		
7kHz	30Hz			-90		
	200Hz			-96		
	500Hz			-96		
15kHz	30Hz			-85		
	200Hz			-96		
	500Hz			-96		
20kHz	60Hz			-85		
	200Hz			-96		
	500Hz			-96		
- continued -						

measurement		min	act.	max	unit
	500Hz			-96	
<i>measurement on ch. 2</i>					
Range	FIX 6V				
input signal	$V_{rms} = 5V$				
f_{RF}	f_{AF}				dB
4kHz	30Hz			-90	
	200Hz			-96	
	500Hz			-96	
7kHz	30Hz			-90	
	200Hz			-96	
	500Hz			-96	
15kHz	30Hz			-85	
	200Hz			-96	
	500Hz			-96	
20kHz	60Hz			-85	
	200Hz			-96	
	500Hz			-96	
Range	FIX 3V				
input signal	$V_{rms} = 3V$				
f_{RF}	f_{AF}				dB
4kHz	30Hz			-90	
	200Hz			-96	
	500Hz			-96	
7kHz	30Hz			-90	
	200Hz			-96	
	500Hz			-96	
15kHz	30Hz			-85	
	200Hz			-96	
	500Hz			-96	
20kHz	60Hz			-85	
	200Hz			-96	
	500Hz			-96	
Analyzer	ANLG 100kHz				
<i>measurement on ch. 1</i>					
Range	FIX 6V				
input signal	$V_{rms} = 5V$				
f_{RF}	f_{AF}				dB
4kHz	200Hz			-80	
	500Hz			-80	
7kHz	200Hz			-80	
	500Hz			-80	
20kHz	200Hz			-80	
	500Hz			-80	
50kHz	200Hz			-80	
					- continued -

measurement		min	act.	max	unit	
100kHz	500Hz			-80		
	200Hz			-80		
	500Hz			-80		
Range	FIX 3V				dB	
input signal	$V_{rms} = 3V$					
f_{RF}	f_{AF}					
4kHz	200Hz			-80		
	500Hz			-80		
7kHz	200Hz			-80		
	500Hz			-80		
20kHz	200Hz			-80		
	500Hz			-80		
50kHz	200Hz			-80		
	500Hz			-80		
100kHz	200Hz			-80		
	500Hz			-80		
<i>measurement on ch. 2</i>						
Range	FIX 6V					dB
input signal	$V_{rms} = 5V$					
f_{RF}	f_{AF}					
4kHz	200Hz			-80		
	500Hz			-80		
7kHz	200Hz			-80		
	500Hz			-80		
20kHz	200Hz			-80		
	500Hz			-80		
50kHz	200Hz			-80		
	500Hz			-80		
100kHz	200Hz			-80		
	500Hz			-80		
Range	FIX 3V				dB	
input signal	$V_{rms} = 3V$					
f_{RF}	f_{AF}					
4kHz	200Hz			-80		
	500Hz			-80		
7kHz	200Hz			-80		
	500Hz			-80		
20kHz	200Hz			-80		
	500Hz			-80		
50kHz	200Hz			-80		
	500Hz			-80		
100kHz	200Hz			-80		
	500Hz			-80		

- continued -

measurement		min	act.	max	unit
Analyzer ANLG 300kHz					
<i>measurement on ch. 1</i>					
Range	FIX 6V				
input signal	$V_{rms} = 5V$				
f_{RF}	f_{AF}				dB
5kHz	500Hz			-80	
10kHz	500Hz			-80	
15kHz	500Hz			-80	
30kHz	500Hz			-80	
60kHz	500Hz			-80	
90kHz	500Hz			-80	
Range	FIX 3V				
input signal	$V_{rms} = 3V$				
f_{RF}	f_{AF}				dB
5kHz	500Hz			-80	
10kHz	500Hz			-80	
15kHz	500Hz			-80	
30kHz	500Hz			-80	
60kHz	500Hz			-80	
90kHz	500Hz			-80	
<i>measurement on ch. 2</i>					
Range	FIX 6V				
input signal	$V_{rms} = 5V$				
f_{RF}	f_{AF}				dB
5kHz	500Hz			-80	
10kHz	500Hz			-80	
15kHz	500Hz			-80	
30kHz	500Hz			-80	
60kHz	500Hz			-80	
90kHz	500Hz			-80	
Range	FIX 3V				
input signal	$V_{rms} = 3V$				
f_{RF}	f_{AF}				dB
5kHz	500Hz			-80	
10kHz	500Hz			-80	
15kHz	500Hz			-80	
30kHz	500Hz			-80	
60kHz	500Hz			-80	
90kHz	500Hz			-80	
differential tone DFD-d2					
DFD-d2 measurement accuracy					
- continued -					

measurement		min	act.	max	unit
Analyzer	ANLG 22kHz				
Min Freq	10 Hz				
Channel(s)	1 ≡ 2				
Input	UNBAL				
<i>measurement on ch. 1</i>					
Range	FIX 3V				
input signal	DFD-d2				
U1 = U2 = 1V	TRUE				
f_{Mean}	f_{Diff}				dB
15kHz	100Hz	-80 dB	-80.5	-79.5	
	200Hz	-80 dB	-80.5	-79.5	
	500Hz	-80 dB	-80.5	-79.5	
	1000Hz	-80 dB	-80.5	-79.5	
Range	FIX 1.8V				
input signal	DFD-d2				
U1 = U2 = 1V	TRUE				
f_{Mean}	f_{Diff}				dB
5kHz	800Hz	-46 dB	-46.5	-45.5	
	700Hz	-60 dB	-60.5	-59.5	
	600Hz	-70 dB	-70.5	-69.5	
7kHz	500Hz	-84 dB	-84.5	-83.5	
15kHz	400Hz	-100 dB	-101.5	-98.5	
	100Hz	-80 dB	-80.5	-79.5	
20kHz	200Hz	-90 dB	-90.75	-89.25	
<i>measurement on ch. 2</i>					
Range	FIX 3V				
input signal	DFD-d2				
U1 = U2 = 1V	TRUE				
f_{Mean}	f_{Diff}				dB
15kHz	100Hz	-80 dB	-80.5	-79.5	
	200Hz	-80 dB	-80.5	-79.5	
	500Hz	-80 dB	-80.5	-79.5	
	1000Hz	-80 dB	-80.5	-79.5	
Range	FIX 1.8V				
input signal	DFD-d2				
U1 = U2 = 1V	TRUE				
f_{Mean}	f_{Diff}				dB
5kHz	800Hz	-46 dB	-46.5	-45.5	
	700Hz	-60 dB	-60.5	-59.5	
	600Hz	-70 dB	-70.5	-69.5	
7kHz	500Hz	-84 dB	-84.5	-83.5	
15kHz	400Hz	-100 dB	-101.5	-98.5	
	100Hz	-80 dB	-80.5	-79.5	

- continued -

measurement			min	act.	max	unit
20kHz	200Hz	-90 dB	-90.75		-89.25	
Analyzer ANLG 100kHz						
<i>measurement on ch. 1</i>						
Range	FIX 6V					
input signal	DFD-d2					
U1 = U2 =	2.5V TRUE					
f_{Mean}	f_{Diff}					dB
5kHz	200Hz	-90 dB	-90.75		-89.25	
20kHz	300Hz	-80 dB	-80.5		-79.5	
50kHz	500Hz	-70 dB	-70.75		-69.25	
90kHz	200Hz	-60 dB	-60.75		-59.25	
<i>measurement on ch. 2</i>						
Range	FIX 6V					
input signal	DFD-d2					
U1 = U2 =	2.5V TRUE					
f_{Mean}	f_{Diff}					dB
5kHz	200Hz	-90 dB	-90.75		-89.25	
20kHz	300Hz	-80 dB	-80.5		-79.5	
50kHz	500Hz	-70 dB	-70.75		-69.25	
90kHz	200Hz	-60 dB	-60.75		-59.25	
Analyzer ANLG 300kHz						
<i>measurement on ch. 1</i>						
Range	FIX 3V					
input signal	DFD-d2					
U1 = U2 =	1.5V TRUE					
f_{Mean}	f_{Diff}					dB
7kHz	1000Hz	-80 dB	-90.5		-89.5	
15kHz	500Hz	-70 dB	-70.5		-69.5	
75kHz	700Hz	-74 dB	-74.75		-73.25	
100kHz	900Hz	-60 dB	-60.75		-59.25	
<i>measurement on ch. 2</i>						
Range	FIX 3V					
input signal	DFD-d2					
U1 = U2 =	1.5V TRUE					
f_{Mean}	f_{Diff}					dB
7kHz	1000Hz	-80 dB	-90.5		-89.5	
15kHz	500Hz	-70 dB	-70.5		-69.5	
75kHz	700Hz	-74 dB	-74.75		-73.25	
100kHz	900Hz	-60 dB	-60.75		-59.25	
DFD-d2 intrinsic distortion						
Analyzer	ANLG 22kHz					
Min Freq	10 Hz					

- continued -

measurement		min	act.	max	unit
Channel(s)	1 ≡ 2				
Input	UNBAL				
<i>measurement on ch. 1</i>					
Range	FIX 6V				
input signal	$V_{rms} = 4V$				
f_{Mean}	f_{Diff}				dB
5kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
7kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
15kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
20kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
Range	FIX 3V				
input signal	$V_{rms} = 2.3V$				
f_{Mean}	f_{Diff}				dB
5kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
7kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
15kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
20kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
<i>measurement on ch. 2</i>					
Range	FIX 6V				
input signal	$V_{rms} = 4V$				

- continued -

measurement		min	act.	max	unit
f_{Mean}	f_{Diff}				dB
5kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
7kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
15kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
20kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
Range input signal	FIX 3V $V_{rms} = 2.3V$				dB
f_{Mean}	f_{Diff}				dB
5kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
7kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
15kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
20kHz	80Hz			-115	
	225Hz			-115	
	525Hz			-115	
	975Hz			-115	
Analyzer <i>measurement on ch. 1</i>	ANLG 100kHz				dB
Range input signal	FIX 6V $V_{rms} = 4V$				dB
f_{Mean}	f_{Diff}				dB
5kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	

- continued -

measurement		min	act.	max	unit
7kHz	225Hz			-110	dB
	525Hz			-110	
	975Hz			-110	
20kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	
50kHz	225Hz			-105	
	525Hz			-105	
	975Hz			-105	
100kHz	225Hz			-90	
	525Hz			-90	
	975Hz			-90	
Range	FIX 3V				
input signal	$V_{rms} = 2.3V$				
f_{Mean}	f_{Diff}				
5kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	
7kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	
20kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	
50kHz	225Hz			-105	
	525Hz			-105	
	975Hz			-105	
100kHz	225Hz			-90	
	525Hz			-90	
	975Hz			-90	
<i>measurement on ch. 2</i>					
Range	FIX 6V				
input signal	$V_{rms} = 4V$				
f_{Mean}	f_{Diff}				
5kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	
7kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	
20kHz	225Hz			-110	
	525Hz			-110	
	975Hz			-110	
50kHz	225Hz			-105	

- continued -

measurement		min	act.	max	unit
100kHz	525Hz			-105	dB
	975Hz			-105	
	225Hz			-90	
	525Hz			-90	
	975Hz			-90	
Range	FIX 3V				
input signal	$V_{rms} = 2.3V$				
f_{Mean}	f_{Diff}				
5kHz	225Hz			-110	dB
	525Hz			-110	
	975Hz			-110	
7kHz	225Hz			-110	dB
	525Hz			-110	
	975Hz			-110	
20kHz	225Hz			-110	dB
	525Hz			-110	
	975Hz			-110	
50kHz	225Hz			-105	dB
	525Hz			-105	
	975Hz			-105	
100kHz	225Hz			-90	dB
	525Hz			-90	
	975Hz			-90	
Analyzer	ANLG 300kHz				
<i>measurement on ch. 1</i>					
Range	FIX 6V				
input signal	$V_{rms} = 4V$				
f_{Mean}	f_{Diff}				
5kHz	525Hz			-110	dB
	975Hz			-110	
10kHz	525Hz			-110	dB
	975Hz			-110	
15kHz	525Hz			-110	dB
	975Hz			-110	
20kHz	525Hz			-110	dB
	975Hz			-110	
30kHz	525Hz			-105	dB
	975Hz			-105	
50kHz	525Hz			-105	dB
	975Hz			-105	
60kHz	525Hz			-90	dB
	975Hz			-90	
90kHz	525Hz			-90	dB
	975Hz			-90	
					- continued -

measurement		min	act.	max	unit	
Range	FIX 3V					
input signal	$V_{rms} = 2.3V$					
f_{Mean}	f_{Diff}				dB	
5kHz	525Hz			-110		
	975Hz			-110		
10kHz	525Hz			-110		
	975Hz			-110		
15kHz	525Hz			-110		
	975Hz			-110		
20kHz	525Hz			-110		
	975Hz			-110		
30kHz	525Hz			-105		
	975Hz			-105		
50kHz	525Hz			-105		
	975Hz			-105		
60kHz	525Hz			-90		
	975Hz			-90		
90kHz	525Hz			-90		
	975Hz			-90		
<i>measurement on ch. 2</i>						
Range	FIX 6V					
input signal	$V_{rms} = 4V$					
f_{Mean}	f_{Diff}				dB	
5kHz	525Hz			-110		
	975Hz			-110		
10kHz	525Hz			-110		
	975Hz			-110		
15kHz	525Hz			-110		
	975Hz			-110		
20kHz	525Hz			-110		
	975Hz			-110		
30kHz	525Hz			-105		
	975Hz			-105		
50kHz	525Hz			-105		
	975Hz			-105		
60kHz	525Hz			-90		
	975Hz			-90		
90kHz	525Hz			-90		
	975Hz			-90		
Range	FIX 3V					
input signal	$V_{rms} = 2.3V$					
f_{Mean}	f_{Diff}					dB
5kHz	525Hz			-110		

- continued -

measurement	min	act.	max	unit
10kHz			975Hz	-110
			525Hz	-110
15kHz			975Hz	-110
			525Hz	-110
20kHz			975Hz	-110
			525Hz	-110
30kHz			975Hz	-110
			525Hz	-105
50kHz			975Hz	-105
			525Hz	-105
60kHz			975Hz	-105
			525Hz	-90
90kHz			975Hz	-90
			525Hz	-90

7.2.6 Service Mode

Service functions for the Analog Analyzer:

For testing and troubleshooting of the analog hardware, a service mode is provided, which can be called in the OPTION panel under SERVICE. It permits configurations of the hardware other than possible with the entries in the ANALYZER Panel (see also section 7.3.6, page 7.165, Service Mode, Analog Generator).

All the possible settings of the service mode are also available in IEC-bus operation (see Operating Manual, DIAGNOSTIC Commands).

Bit groups of 1 to 16 bits can be varied in the serial data stream of the analyzer. A single bit permits, e.g., to switch a particular relay, 12 bits switch a Monitor-Out-DAC, 5 bits or 12 bits permit new setting of the frequency of the analog notch filter.

The board descriptions include the hardware function tables from which position, number, value range and function of the bits can be obtained.
--

- Calling the service mode

- Change to OPTION Panel
- Enter the password in the line 'SERVICE password ?'

After entering the correct password:

OPTION Panel	SERVICE	password ok
	Diag State	OFF

- Activate service mode

Diag State ON

ON Activate service mode for all analog boards

UPD setup is stored

normal operation via the panels remains active

NOTE: A further setting in the Analyzer Panel and the cycle of an active test function may overwrite the entries of service mode.

OFF Switch off service mode

UPD is set to the status valid before calling the service mode

- After selecting 'Diag State ON', the OPTION Panel may appear as follows:

OPTION Panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.000

	ANLR Board	MOT
	Position	0
	Count(Bit)	0
	Bitvalue	0
	Execute	NO

- Setting the analog hardware

- Selecting the board (ANLR Board \equiv Analyzer)
 - ANLR Board MOT → Analog Motherboard (Analyzer section)
 - ANA1 → Analog Analyzer 1
 - ANA2 → Analog Analyzer 2
 - NONAME ANL → Spare slot X23
(currently not used)

- Setting the bits

Position Position of the first bit to be changed
Count(Bit) Word length of the bits to be changed (maximal 16)
Bitvalue new bits (decimal 0 ... 65535)

The value to be entered for Count is ≥ 1 . Bit value is to be confirmed anew for each bit position, even with the same value.

- Executing the setting

Execute NO nothing happened, internal preadjustment
 YES Send bit stream
 ⇒ Hardware is set

7.2.7 Analog Motherboard (Analyzer Section)

Circuit diagram	1030.9060.01 S
Component location plan	1030.9060
Parts list	1030.9060.01 SA

Circuit diagram overview see section 7.1.2, 7.4

7.2.7.1 Function

General information on the Analog Motherboard: see section 7.1.2.1, page 7.4.

Control of the Analog Analyzer and its data communication with the DSP A is performed by Digital Analyzer 1 via the 34-contact flat cable W31. If the Option Highspeed UPD-B3 is fitted, a parallel data communication takes place from the DSP B of the Digital Analyzer 2 with the ADC Board of analyzer channel 2 via the 34-contact connection W35.

- Connection between Digital and Analog Analyzer
(W31, W35 to Digital Analyzer 1, 2, Circuit diagram sheet 4)

Part of the signals on the Digital Analyzer board are not referred to with the same signal names as on the Analog Motherboard. The opposite table shows the relationship:

Analyzer	
Analog	Digital
PSEL-R/F	WREN
SCLK[A]	CCLK
L/R[A]	CLR
SOC[A]	SOC
CLKIN[A]	SCKLOUT
PK-INTR[A1]	PEAKA
PK-INTR[A2]	PEAKB

- Serial hardware control interface
(Circuit diagram sheet 6)

Serial interface for controlling the Analyzer hardware		
IAICLK	Clock	Shift clock for the data ($\approx 1.7\text{MHz}$) the data bits are shifted with the positive edge
IAID0	Data in	serial data stream, MSB first
SD1[A]	Data out	to Analog Analyzer 1
IAIWR	Write	active 'Low', pulse width $\approx 200\text{ns}$ Data are transferred from the shift registers to the output <i>latches</i>
IAIRD	Read	active 'Low', pulse width $\approx 200\text{ns}$ The board identification (BOARD ID) of the boards (8 bits each) is inserted into the data stream

Serial data stream:

The data are shifted in blocks of 8 bits each with the rising clock edge. All Analog Analyzer modules are series-connected like in a long shift register. The data are read back to Digital Analyzer 1 via IAIDI.

Board	Bits ¹¹	Remark
Spare board, X23	0	currently not used
Analog Motherboard	48	Analyzer section
Analog Analyzer 1	68	
Analog Analyzer 2	68	
Data length	184	without spare board X23

The table also reflects the sequence of the boards in the data stream: the Analog Motherboard or the spare board X23 come first, the Analog Analyzer 2 comes last.

Since the entire data stream is always transmitted in blocks of 8 bits each, 184 bits are transferred in 23 blocks without spare board. The last bit of Analog Analyzer 2 is always the last bit of the complete data stream.

Board identification:

During the selftest of the UPD on switch-on, the board identifications of the boards are read in and checked. The order is from the bottom to the top according to the table. (→ Analyzer 2 comes first).

Data Multiplexer:

(ANA DATA MUX X23, circuit diagram sheet 6)

The multiplexer switches the data stream for the spare board which can be inserted into X23 (spare slot).

If no board is inserted, control line SD-OPT[A] is open and is pulled to 0 using pulldown resistor R606. The inserted board applies SD-OPT[A] to +5V.

SD-OPT[A]	Data stream
+5V	Board is inserted
0V	Data are not applied to the board

- Internal connection Generator to Analyzer

(Internal Connection Generator to Analyzer, circuit diagram sheets 4, 6)

From data register D605, driver D605 provides logically inverted control levels at *Open-Collector* outputs for the relays K401...K406, K408. Relay K407 is directly controlled from data register D605 via V601.

The analog signal connection to the generator permits the generator voltages to be measured without external cable connection (see Operating Manual, Configuration of the Analog Analyzers). Depending on the generator setting, the switching paths with the signal names BAL... or UNBAL... are used.

With the generator outputs switched off, the signal lines to the analyzer are grounded (K401, K402 or K405, K406 not energized).

Via K404, K408, the relay configuration enables switchable FLOAT/GND operation of the two test channels in *normal* input mode, the relays K401, K402 or K405, K406 representing a ground reference in the case of GND.

¹¹No. of bits including board identification

The switchable ground reference is also used for the cyclical offset voltage correction of the Analyzer boards, the test signals being deactivated and the inputs referred to ground (see OPTION Panel CAL ANL 'ZERO AUTO', 'ZERO ONCE' or, with earlier firmware, CALIBRATE 'AUTO', 'OFFSET').

- Monitor Output, analog level variation

(MONITOR FOR ANALYZER 1,2, circuit diagram sheet 6)

The level variation of the monitor outputs is effected via digital control of the 12-bit DACs D650 (Ch1-Out) and D660 (Ch2-Out). The multiplying D/A converters use the analog signal ACAMP[A1] or [A2] at the input VREF to provide a current at the output IOUT1, which is proportional to the set bit combination (setting code MO_ATTEN). Together with the opamp N650, N660 and the DAC-internal feedback resistors R_{FB} inverting output stages are formed.

The following applies to the voltage at the output of opamp N650, N660:

$$V_o = V_i * MO_ATTEN / 4096$$

Setting code		Attenuation
Hex	Decimal	dB
000	0	> 70, off
FFF	4095	0

- Backup for External Filters/Special Filters

(EXT. FILTER FOR ANALYZER 1,2, circuit diagram sheet 6)

In the case of the Analog Analyzer, external analog filters or internal special filters can be optionally connected into the signal path. Associated circuit groups and cable connectors to the UPD rear panel are currently not fitted (dashed marking in the circuit diagram).

- Phase comparator

(ANALYZER PHASE COMPARATOR, circuit diagram sheet 5)

As to the function in interaction with Analog Analyzer and Digital Analyzer 1, see explanation in section 6.1.1.5, page 6.5, Measurement of: frequency and phase.

Phase comparison: The digital signals from multiplexer D510 are compared in D501. Output D501/PC01 provides the exclusive-OR comparison, the signal of the edge comparison being provided at output D501/PC03.

Device D502 operates as phase modulator with the carrier frequency 6.144 MHz (CLKIN[A]) and the modulation signal $V_{pp} \approx 4V$, $f \approx 90Hz$ from the triangle generator with N520. The signals from the phase comparator output D502/PC03 and the triangle generator are applied to the VCO input of device D502. After feedback to the comparator input, the VCO output D502.4 provides the clock jitter signal JCLK with the center frequency 6.144 MHz. With this clock, the signal of the edge comparison from D501.15 (PC03) is edge-triggered and taken to D flip-flop D505-B and its output D505.9 PHASB. The 2nd part of D505-A is used as clock buffer.

7.2.7.2 Controlling the Analog Functions

Board identification 50 hex, bit length 48, absolute bit position 0..47 (with spare slot not fitted), relative bit position 0..47 (\equiv hardware function table), bit stream MSB first

Hardware function table: Analog Motherboard (Analyzer section)

device	BITS			function
	Pos.	Count	Bitvalue	
D606	0	1	1/0	Phase Measure: 0=Pos.180°, 1=pos.0° not connected
D606	1	7	—	
D605				GEN2-ANA Switch (Bal) GEN2-ANA Switch (Unbal) GEN-ANA Switch (Unbal) 0 = GEN2-ANA2 Switch or ANA2-GND GND/FLOAT Switch CH2 GEN1-ANA Switch (Bal) GEN1-ANA Switch (Unbal) GND/FLOAT Switch Ch1 GEN1-ANA1 Switch 0 = GEN2-ANA1 Switch or ANA1-GND
K401	.4	8	1=on	
K402	.5	9	1=on	
K403	.6	10	1=on	
K404	.7	11	1=GND	
K405	.14	12	1=on	
K406	.13	13	1=on	
K408	.12	14	1=GND	
K407	.11	15	1=on	
DAC8143/ D650	16..27	12		
DAC8143/ D660	28..39	12		
D680	40..47	8		Serial Out SD1[A] Board identification, incl. version is inserted into the data stream with the IAI RD pulse.

Bit 47 = MSB, end of Analog Motherboard (Analyzer section).

Continuation of bit stream in Analog Analyzer 1

7.2.7.3 Measuring Equipment

Measuring instrument	Specifications	R & S
Oscilloscope	Digital memory 4 channels, 100MHz	—
Voltmeter	VDC, VAC	URE 3

7.2.7.4 Testing and Troubleshooting

- Testing the Operating Voltages

DC measurement on flat cable W20B from the power supply or on the multipoint connectors of the boards.

Test values, see external interfaces

CAUTION: Note the correct ground reference of the different analyzer grounds:

- Testing the board identification (BOARD ID)

Each board of the Analog Analyzer contains a parallel-in/serial-out shift register in the serial data stream.

The byte at the parallel input of shift register D680 (coded with pull_up and pull_down resistors) is referred to as BOARD ID.

BOARD ID = 01010000B = 50H ¹²

The BOARD ID is inserted into the serial data stream with the IAIRD pulse and read in by Digital Analyzer 1 during the UPD program start only.

Signals for checking the board identifications: ¹

Signal	Motherboard	Analyzer 1	Analyzer 2
IAIRD	W31.8	= X22.A15	= X21.A15
IAICLK	W31.11	= X22.A13	= X21.A13
SD0	SD1[A], X22.C12	X22.C11	IAIDI, X21.C11

Test: Connect digital storage oscilloscope to the signal points.

Evaluate: See Analog Motherboard (generator section), page 7.175.

BOARD ID Analog Analyzer: See section 7.2.8.4, page 7.95.

- Testing the hardware control interface

Cause cyclical setting of the analyzer hardware, e.g. by means of the following setting:

Generator Panel	Analyzer Panel
Frequency sweep	RMS SEL
Auto Mode	Freq Mode: Gen Track

The control signals IAICLK, IAID0 and IAIWR are transmitted in cyclical sequence and can be traced with the oscilloscope on the serial device chain D610, D606, D605, D650, D660 and D680.

If the signals are okay and the data arrive at D680.9 SD[1], a faulty function may be due to an internal fault of the register devices or their peripheral devices.

- Testing the phase comparator circuit

(circuit diagram sheet 5)

UPD setting:

Generator Panel	Analyzer Panel
Function Sine	Frequency 2-channel
Frequency e.g. kHz	or Freq&Phase

Apply the generator signals to both analyzer inputs at the same time. Select the appropriate generator level and Analyzer level setting.

Signal multiplexer: In the case of pure frequency measurement, the squarewave signals FRISE[A1] and FRISE[A2] from Analog Analyzer 1 and 2 are connected further via multiplexer D510 and gates D500 to Digital Analyzer 1 for frequency measurement (signals FAMESS, FBMESS). Control lines PSEL-180/0 and PSEL-R/F are applied to logic 0.

¹²B = binary, H = hexadecimal

- Testing the monitor outputs
 - Set analyzer channels to Range FIX 3V and Monitor Out ON.
 - Apply input signal 3V, 1kHz to both inputs.
 - Measure the input voltage of D/A converters D650, D660 using AC voltmeter at X21.C20, X22.C20 (ACAMP [2], ACAMP [1])
 - Measure the output voltages at the monitor outputs with different attenuation setting in the Analyzer Panel

Attenuation	Ratio input/output
0 dB	0 dB \pm 0.05 dB
20 dB	20 dB \pm 0.1 dB
OFF	> 70 dB

Testing the control signals of the D/A converters:

Trace the load pulse (active H) at D650.5,9 and D660.5,9, clock and data strobe at SRI, SRO of the devices using an oscilloscope.

7.2.7.5 External Interfaces

Cable to front panel (W800, from Analog Analyzer 1, 2)						
name	Signal description	≡	source dest.	range	connector	comment
BAL2[A2]	at XLR 2 Pin2			0..35V RMS, ±35V DC 2Hz...300kHz	X800.2	bal. input channel 2
BAL3[A2]	at XLR 2 Pin3				X800.3	
BAL2[A1]	at XLR 1 Pin2			0..35V RMS, ±35V DC 2Hz...300kHz	X800.7	bal. input channel 1
BAL3[A1]	at XLR 1 Pin3				X800.8	
GND n.c.	Ground Connector coding			0V	X800.4,6 X800.1,5	Cable shields

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Cable to rear panel (W802, W803 Monitor-Out/External filter)						
name	Signal description	≡	source dest.	range	connector	comment
MONITOR	[A1]	O		0...3.5V RMS 2Hz...300kHz	X802.1	Monitor Out BNC-Ch1 Rear reserved reserved
EXTFIL OUT	[A1]	O	n.c.		X802.4	
EXTFIL IN	[A1]		n.c.		X802.6	
GND n.c.	Shield Connector coding			0V	X802.2,5,7 X802.3	
MONITOR	[A2]	O		0...3.5V RMS 2Hz...300kHz	X803.1	Monitor Out BNC-Ch2 Rear reserved reserved
EXTFIL OUT	[A2]	O	n.c.		X803.4	
EXTFIL IN	[A2]		n.c.		X803.6	
GND n.c.	Shield Connector coding			0V	X803.3,5,7 X803.2	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

ANALOG ANALYZER 2 (X21, 64-contact VG strip)						
name	Signal description	≡	source dest.	range	connector	comment
BAL2[A2]	balanced		X800	0..35V RMS, ±35V DC 2Hz...300kHz	X21.C32	XLR-Input, Pin 2
BAL3[A2]	balanced			dito	X21.A32	XLR-Input, Pin 3
GEN2[A2]	Int. GEN-Connect		GEN	0...12V RMS Unbal, 0...24V RMS Bal	X21.C27	Signal from Gene- rator
GEN3[A2]	Int. GEN-Connect		GEN	dito.	X21.A27	reserved for extension
EXTFIL[A2]	from external filter			0...3.5V AC	X21.A22	
Test outputs						
FRISE[A2]	1. Freq Rising	O		0/5V, 2Hz...300kHz	X21.A16	Freq./Phase
FFALL[A2]	2. DC-f Convert	O		0/5V, 5kHz...15kHz	--	DC measurement
ACAMP[A2]	Freq. Falling	O		0/5V, 2Hz...300kHz	X21.C14	Freq./Phase
ANALOG[A]	Input Ranging Out	O		0...3.5V AC	X21.C20	to Monitor MothB
	Function Out	O	X600.2	0...3.5V AC	X21.A18, X2.B17	RMS-Level-, Notch-, d2-LP-Out
Operating voltages						
-	Analog ground	O		Float/Gnd reference	X21.A24,25	Analog
GND[A2]	Analog ground			reference floating	X21.AC29	
-18V[A2]				-18V±1V	X21.C23	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
+18V[A2] +6V[A2] GND -15V +15V +5V	Ground			+18V±1V	X21.C24	Floating Potential X21.A1,17,21,23,26,28 X21.C22,26,28 X21.AC19,30,31; X21.C15, X2.B13 X21.C16, X2.A2 X21.C17 5V
				+6V±0.2V	X21.C25	
				0V		
				-15V±0.75V		
				+15V±0.75V		
				+5V±0.15V		
Digital control signals						
IAICLK WR[A] LOAD[A] SD2[A] IAIDI PK-INTR[A2]	Clock signal Write Load ser. data Ser. data Pk-Interrupt	 O O	DigAna1 (=W31.12) DigAna1	TTL HCT logic level HCT HCT HCT 0/5V	X21.A13 X21.C13 X21.A14 X21.C11 X21.C18	+Edge active H-pulse, L-pulse (=X22.C11) Monitor control
AD converter signals						
ADS11[A2] ADS10[A2] ADS9[A2] ADS8[A2] ADS7[A2] ADS6[A2] ADS5[A2] ADS4[A2] ADS3[A2] ADS2[A2] ADS1[A2] ADS0[A2] EOC[A2] SOC[A]	Bit11(MSB) Bit10 Bit9 Bit8 Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0 (LSB) End of Conv. Start of Conv.	O O O O O O O O O O O O O 	DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna2 DigAna1	TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL TTL HCT level	X21.C1 X21.A2 X21.C2 X21.A3 X21.C3 X21.A4 X21.C4 X21.A5 X21.C5 X21.A6 X21.C6 X21.A7 X21.C7 X21.A8	(=W35.33) (=W35.32) (=W35.31) (=W35.30) (=W35.29) (=W35.28) (=W35.27) (=W35.26) (=W35.25) (=W35.24) (=W35.23) (=W35.22) (=W35.21) Pulse (=W31.20) Puls 163ns
L/R[A] CATP[A] SCLK[A] CDATA[A2] CLKIN[A]	Left/Right Reset Clock 3.072MHz Ser. Data Out Operating clock	 O 	DigAna1 DigAna1 DigAna1 DigAna2 DigAna1	HCT level HCT level HCT level TTL L:<1V, H:>4V ..144MHz	X21.C8 X21.A9 X21.C9 X21.A10 X21.A11	(=W31.17) Frame 48kHz (=W31.18) Sync. Reset (=W31.15, W35.15) (=W35.16) 64-Bit/Conv (=W31.14)
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

ANALOG ANALYZER 1 (X22, 64-contact VG strip)						
name	Signal description	≡	source dest.	range	connector	comment
BAL2[A1] BAL3[A1] GEN2[A1] GEN3[A1] ANALOG[A] EXTFIL[A1]	balanced balanced Int. GEN-Connect Int. GEN-Connect to adjacent channel from external filter	 O 	X800 GEN GEN ADC Ch2	0..35V RMS, ±35V DC 2Hz...300kHz dito 0...12V RMS Unbal, 0...24V RMS Bal dito. 0...3.5V AC 0...3.5V AC	X22.C32 X22.A32 X22.C27 X22.A27 X22.A20 X22.A22	XLR-Input, Pin 2 XLR-Input, Pin 3 Signal from Generator reserved for extension
- continued -						

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
Test outputs						
FRISE[A1]	1. Freq Rising	O		0/5V, 2Hz...300kHz	X22.A16	Freq./Phase
	2. DC-f Convert	O		0/5V, 5kHz...15kHz	--	DC measurement
FFALL[A1]	Freq. Falling	O		0/5V, 2Hz...300kHz	X22.C14	Freq./Phase
ACAMP[A1]	Input Ranging Out	O		0...3.5V AC	X22.C20	to Monitor MothB
n.c.	Function Out	O		0...3.5V AC	X22.A18	RMS-Level-, Notch-, d2-LP-Out
Operating voltages						
-	Analog ground	O		Float/Gnd reference	X22.A24,25	
GND[A1]	Analog ground	I		Reference floating	X22.AC29	
-18V[A1]		I		-18V±1V	X22.C23	Analog
+18V[A1]		I		+18V±1V	X22.C24	Floating
+6V[A1]		I		+6V±0.2V	X22.C25	Potential
GND	Ground			0V	X22.A1,17,21,23,26,28 X22.C22,26,28 X22.AC19,30,31;	
-15V		I		-15V±0.75V	X22.C15, X2.B13	
+15V		I		+15V±0.75V	X22.C16, X2.A2	
+5V		I		+5V±0.15V	X22.C17	5V
Digital Control signals						
IAICLK	Clock signal	I	DigAna1	TTL	X22.A13	+edge active
WR[A]	Write	I		HCT logic level	X22.C13	H-pulse,
LOAD[A]	Load	I		HCT	X22.A14	L-pulse
SD1[A]	Ser. data	I		HCT	X22.C12	from AnaMoth
PK-INTR[A1]	Pk-Interrupt	U	DigAna1	0/5V	X22.C18	Monitor control
AD converter signals						
ADS11[A1]	Bit11(MSB)	U	DigAna1	TTL	X22.C1	(=W31.33)
ADS10[A1]	Bit10	O	DigAna1	TTL	X22.A2	(=W31.32)
ADS9[A1]	Bit9	O	DigAna1	TTL	X22.C2	(=W31.31)
ADS8[A1]	Bit8	O	DigAna1	TTL	X22.A3	(=W31.30)
ADS7[A1]	Bit7	O	DigAna1	TTL	X22.C3	(=W31.29)
ADS6[A1]	Bit6	O	DigAna1	TTL	X22.A4	(=W31.28)
ADS5[A1]	Bit5	O	DigAna1	TTL	X22.C4	(=W31.27)
ADS4[A1]	Bit4	O	DigAna1	TTL	X22.A5	(=W31.26)
ADS3[A1]	Bit3	O	DigAna1	TTL	X22.C5	(=W31.25)
ADS2[A1]	Bit2	O	DigAna1	TTL	X22.A6	(=W31.24)
ADS1[A1]	Bit1	O	DigAna1	TTL	X22.C6	(=W31.23)
ADS0[A1]	Bit0 (LSB)	O	DigAna1	TTL	X22.A7	(=W31.22)
EOC[A1]	End of Conv.	O	DigAna1	TTL	X22.C7	(=W31.21) Pulse
SOC[A]	Start of Conv.	I	DigAna1	HCT level	X22.A8	(=W31.20) Pulse pulse 163ns
L/R[A]	Left/Right	I	DigAna1	HCT level	X22.C8	(=W31.17) Frame 48kHz
CATP[A]	Reset	I	DigAna1	HCT level	X22.A9	(=W31.18) Sync. Reset
SCLK[A]	Clock 3.072MHz	I	DigAna1	HCT level	X22.C9	(=W31.15)
CDATA[A1]	Ser. Data Out	O	DigAna1	TTL	X22.A10	(=W31.16) 64-Bit/Conv
CLKIN[A]	Operating clock	I	DigAna1	L:<1V, H:>4V 6.144MHz	X22.A11	(=W31.14)
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

Spare slot (Analyzer section)						
(X23, 64-contact VG strip)						
name	Signal description	=	source dest.	range	connector	comment
Analog signals						
SPECFIL[A2]	to special filter	O	channel 2	0...3.5V AC, 2Hz...300kHz	X23.A1	reserved for extension
SPECFIL[A1]	to special filter	O	channel 1	0...3.5V AC, 2Hz...300kHz	X23.C1	reserved for extension
EXTFIL[A2]	from special filter	O	channel 2	0...3.5V AC, 2Hz...300kHz	X23.C3	reserved for extension
EXTFIL[A1]	from special filter	O	channel 1	0...3.5V AC, 2Hz...300kHz	X23.A3	reserved for extension
Digital control signals						
OPT[A]	ti ANA DATA MUX	O		0/5V	X23.B4	Board identification
IAIRD	Read	I	DigAna1	TTL	X23.A5	L-pulse
WR[A]	Write	I	AnaMoth	HCT logic level	X23.B5	H-pulse
IAIDO	Ser. data	I	DigAna1	TTL	X23.A6	
IAICLK	Clock signal	I	DigAna1	TTL	X23.A7	+edge active
SD-OPT[A]	Ser. data	O	AnaMoth	TTL	X23.B6	with spare board
Operating voltages						
GND	Ground, Chassis reference			0V	X23.B1, A2, B2, C2, B3, A4, C4 X23.A8, B8, C8	
-15V		I		-15V±0.75V	X23.B7	
+15V		I		+15V±0.75V	X23.C7	
+5V		I		+5V±0.15V	X23.C6	Digital
+6V		I		+6V±0.2V	X23.C5	
Explanation: =: I:Input, O:Output, B:Bidirectional, P:Power						

Cable to Digital Analyzer 1						
(W31, 34-contact, from Analog Analyzer 1, 2)						
name	Signal description	=	source dest.	range	connector	comment
GND	ground			0V	W31.1,34	
Test outputs						
FAMESS	1. Freq Rising Ch1	O		0/5V, 2Hz...300kHz	W31.3	Freq./Phase
	2. DC-f Convert Ch1	O		0/5V, 5kHz...15kHz	"	DC measurement
FBMESS	Freq Rising Ch2	O		HCT, 2Hz...300kHz	W31.5	Freq./Phase
	2. DC-f Convert Ch2	O		HCT, 5kHz...15kHz	"	DC measurement
PHASA	XOR comparison Ch1-2	O		HCT	W31.7	Phase
PHASB	Phase signal Ch1-2	O		HCT	W31.19	Phase
LDFREQ	Freq Low Dist Gen	O	DigAna 1	0/5V, 10Hz...110kHz	W31.6	for Freq measurement
Digital Control signals						
IAICLK	Clock signal	I	DigAna1	TTL	W31.11	+edge active
IAIWR	Write n	I	DigAna1	TTL	W31.9	L-pulse,
IAIRD	Read	I	DigAna1	TTL	W31.8	L-pulse
IAIDO	Ser. data	I	DigAna1	TTL	W31.10	
IAIDI	Ser. data	O	DigAna1	HCT	W31.12	Board ID
PK-INTR[A1]	Pk-Interrupt	O	AnlgAna1	0/5V	W31.2	Monitor control
PK-INTR[A2]	Pk-Interrupt	O	AnlgAna2	0/5V	W31.4	Monitor control
PSEL-R/F	Phase Rise/Fall	I	DigAna1	HCT	W31.13	to phase logic
AD converter signals						
ADS11[A1]	Bit11(MSB)	O	DigAna1	TTL	W31.33	(=X22.C1)
ADS10[A1]	Bit10	O	DigAna1	TTL	W31.32	(=X22.A2)
- continued -						

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
ADS9[A1]	Bit9	O	DigAna1	TTL	W31.31	(=X22.C2)
ADS8[A1]	Bit8	O	DigAna1	TTL	W31.30	(=X22.A3)
ADS7[A1]	Bit7	O	DigAna1	TTL	W31.29	(=X22.C3)
ADS6[A1]	Bit6	O	DigAna1	TTL	W31.28	(=X22.A4)
ADS5[A1]	Bit5	O	DigAna1	TTL	W31.27	(=X22.C4)
ADS4[A1]	Bit4	O	DigAna1	TTL	W31.26	(=X22.A5)
ADS3[A1]	Bit3	O	DigAna1	TTL	W31.25	(=X22.C5)
ADS2[A1]	Bit2	O	DigAna1	TTL	W31.24	(=X22.A6)
ADS1[A1]	Bit1	O	DigAna1	TTL	W31.23	(=X22.C6)
ADS0[A1]	Bit0 (LSB)	O	DigAna1	TTL	W31.22	(=X22.A7)
EOC[A1]	End of Conv.	O	DigAna1	TTL	W31.21	(=X22.C7) Pulse
SOC[A]	Start of Conv.	I	DigAna1	HCT level	W31.20	(=X22.A8) Pulse 163ns
L/R[A]	Left/Right	I	DigAna1	HCT level	W31.17	(=X22.C8) Frame 48kHz
CATP[A]	Reset	I	DigAna1	HCT level	W31.18	(=X22.A9) Sync. Reset
SCLK[A]	Clock 3.072MHz	I	DigAna1	HCT level	W31.15	(=X22.C9)
CDATA[A1]	Ser. Data Out	O	DigAna1	TTL	W31.16	(=X22.A10) 64-Bit/Conv
CLKIN[A]	Operating clock	I	DigAna1	L:<1V, H:>4V 6.144MHz	W31.14	(=X22.A11)

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Cable to Digital Analyzer 2 (W35, 34-contact, from Analog Analyzer 2, Option UPD-B3 Highspeed)						
name	Signal description	≡	source dest.	range	connector	comment
GND	Ground			0V	W35.1,34	
AD converter signals						
ADS11[A2]	Bit11(MSB)	O	DigAna2	TTL	W35.33	(=X21.C1)
ADS10[A2]	Bit10	O	DigAna2	TTL	W35.32	(=X21.A2)
ADS9[A2]	Bit9	O	DigAna2	TTL	W35.31	(=X21.C2)
ADS8[A2]	Bit8	O	DigAna2	TTL	W35.30	(=X21.A3)
ADS7[A2]	Bit7	O	DigAna2	TTL	W35.29	(=X21.C3)
ADS6[A2]	Bit6	O	DigAna2	TTL	W35.28	(=X21.A4)
ADS5[A2]	Bit5	O	DigAna2	TTL	W35.27	(=X21.C4)
ADS4[A2]	Bit4	O	DigAna2	TTL	W35.26	(=X21.A5)
ADS3[A2]	Bit3	O	DigAna2	TTL	W35.25	(=X21.C5)
ADS2[A2]	Bit2	O	DigAna2	TTL	W35.24	(=X21.A6)
ADS1[A2]	Bit1	O	DigAna2	TTL	W35.23	(=X21.C6)
ADS0[A2]	Bit0 (LSB)	O	DigAna2	TTL	W35.22	(=X21.A7)
EOC[A2]	End of Conv.	O	DigAna2	TTL	W35.21	(=X21.C7) Pulse
L/R[A]	Left/Right	I	DigAna1	HCT level	W35.17	(=X21.C8) Frame 48kHz
SCLK[A]	Clock 3.072MHz	I	DigAna1	HCT level	W35.15	(=X21.C9)
CDATA[A2]	Ser. Data Out	O	DigAna2	TTL	W35.16	(=X21.A10) 64-Bit/Conv
CLKIN[A]	Operating clock	I	DigAna1	L:<1V, H:>4V 6.144MHz	W35.14	(=X21.A11)

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.2.8 Analog Analyzer 1 and 2

Circuit diagram	1030.9102.01 S
Component location plan	1030.9102
Parts list	1030.9102.01 SA

Circuit diagram overview	
Sheet:	Contents
1/10:	Block diagram
2/10:	Input branching, input voltage divider
3/10:	Input protection, input buffer, input amplifier
4/10:	Range divider, range amplifier, buffer stage, Peak Control, DC-f-Converter
5/10:	Frequency Comparator
6/10:	d2-lowpass 1 kHz, notch correction filter, function switchover
7/10:	Notch filter
8/10:	Relay control, serial control interface/register
9/10:	serial control interface/register, level converter, board identification
10/10:	Pin assignment

7.2.8.1 Function

Each channel of the Analog Analyzer boards receives the balanced input signal from the XLR connector via the Analog Motherboard and multipoint connector X1, whereas the unbalanced input signal is taken from the BNC connector via a coaxial cable directly to SMB connector X200. The input section of the Analog Analyzer is isolated from the chassis, the computer and other boards and is operated from an extra current supply of the analog power supply.

- Input circuit

In the isolated input circuit, the test signals from the input connectors are first processed with respect to level via input divider, input amplifier 20 dB or buffer stage 0 dB, range attenuator pad 0/5 dB and range amplifier 0/5/10/20 dB. (see level tables for balanced and unbalanced input mode at the end of this section).

- Balanced input

The input signal (BAL2 and 3) arrives at the symmetrically designed network, which contains resistors that can be cut in via relays for the different input impedances 20k Ω , 600 Ω , 300 Ω and USER DEF. If the balanced input is cut off, the selected input impedance is maintained at the input via the relays K225, K230, K235 or K240.

The AC/DC coupling to the input divider and the balanced amplifier stages can be switched over via relay K250. Coupling capacitors C250, C251 are matched in order to achieve high unbalance rejection of the test input at low frequencies. The input voltage divider with resistors R260 .. R267 (input impedance 2*100 k Ω) has symmetrical taps for 10 and 20 dB and is capacitively compensated. It divides the input signal in the level range from 6V..35V.

In the input mode Input GEN (K235 ON), the generator signal is connected via the Analog Motherboard to the inputs (GEN2 and GEN3). Only the balanced input divider acts as input impedance with 2*100k Ω .

- Unbalanced input

The input signal (UNBAL HI and LO) is taken via relay K200 and the AC/DC input coupling with K205/C205 to the high-impedance $1M\Omega$ input voltage divider with resistors R206...R208. The voltage divider features capacitively compensated stages of 20 and 40 dB for the level range from 6V...300V. The adjustment for 20dB is performed using trimmer C 211, for 40dB using trimmer C217 at 20kHz in each case (previous coarse adjustment of 40-dB stage with a capacitor parallel to C215).

The outer conductor reference of the input is floating and can optionally be connected to the chassis via the relay in the Analog Motherboard (GROUND/FLOAT switchover).

- Input protection

The input amplifiers and buffer stages are protected against excessive input voltage by means of biased protection diodes (V315, V316 or V375, V376). For current limitation, the two bridges consisting of V303...V306 or V363...V366 are used, switching off the input signal automatically when the peak value of the input alternating current exceeds the value of the direct current in the cross path.

For transmitting the input signal without distortions in normal operation, two diode bridges are adjusted capacitively via the outputs of buffer stages N330, N390 and capacitors C315, C316 or C375, C376. Thus, no differential AC voltage is applied to the diode bridges as long as there is no current limitation.

- Input amplifier and level processing

For the measurement range stages above 300mV, the FET buffer stages with 0-dB amplification are used, for more sensitive measurement ranges, the FET operational amplifiers N345, N350 with 20-dB amplification are cut in.

Further level division and amplification in 5-dB steps is then effected by a range divider 0/5dB (R400, R402 or R421, R419) and a range amplifier with 0/5/10/20dB (N405, N425) in symmetrical design.

Table: Range amplification

Relay	Gain			
	0dB	5dB	10 dB	20dB
K410	●	○	○	○
K415	○	●	○	○
K420	○	○	○	●
● On ○ Off				

The signal at the output of range amplifier N405, N425 can then be further processed. The following buffer stage with transformer permits subtraction with a high common-mode rejection as well as transition from the floating input section to the circuit groups referred to the chassis.

- DC measuring path

After passing the DC-coupled input and range level setting, the test voltage is taken via differential amplifier (N410, test point P400.1, FRQIN) to a voltage/frequency converter (DC/f converter D470) for recording the DC component. Because of the unipolar way of operation, a positive reference voltage is superimposed on the DC/f converter for the bipolar DC measurement at the input (V467, $V_{ref} = +2.5V$). From the input DC voltage, the converter provides

a frequency-proportional squarewave signal DCF at the output for evaluation in the frequency counter (see also section 6.1.1.6, page 6.6).

- Comparator for frequency/phase measurement

For frequency measurement in counter mode, the signals are applied to level comparators at the output of the range level setting after subtraction in N410 and passing of a 500-kHz lowpass N500. .N504. The latter use threshold values, derived from two detectors for +PK/2 and -PK/2, to produce squarewave control signals for frequency/phase measurement via flip-flop stages N500. The control signals are taken via optocouplers (U465-A,B) to the phase comparator logic on the Analog Motherboard and to the frequency counter on the Digital Analyzer Board 1.

The falling edge of the signal FMESS at U465.6 corresponds to the rising test signal edge. It triggers the frequency counter for frequency measurement and is used for phase comparison with the other Analyzer channel. The falling edge of the signal PHIMESS at U465.7 corresponds to the falling test signal edge. It is used for phase comparison with the other analyzer channel (see also section 6.1.1.5, page 6.5).

- Monitoring the dynamic range

A peak detector circuit is used for monitoring the dynamic range of the signal levels at the output of the range level setting (N405.6 ,N425.6). A circuit for +PK and -PK is provided with diode rectifier, charging capacitor, reset circuit and operational amplifier. The detector circuit forms the greatest magnitude from the differential level and the common-mode dynamic levels. Via a programmable comparator threshold (PEAK CMP1 and 2), an interrupt signal is generated for the AT at the output if specified level limits are exceeded.

- Buffer stage

The active transformer stage (T1, N440, N415, N435) forms the difference of the signal at the output of range amplifier N405, N425 with high common-mode rejection. At the same time, the transition is made from the floating input section to the circuit groups referred to the chassis.

It acts as an inverter with the gain factor 1. The high unbalance rejection according to DIN 45405 is obtained by means of the balanced input circuit, the balanced supply via resistors R407, R427 and the balun T1 operated as current transformer with double potential shielding.

The chopper amplifier N415 connected up as integrator stabilizes the degenerative operational amplifier N440. The amplifier configuration N435 causes a frequency-dependent feedback of the output voltage of N440 to base impedance R430 of the secondary transformer winding. After adjustment using R435, the distortion factor of the stage is reduced to minimum at low frequencies.

- Function branching

The test signal is further processed in function groups for the different types of measurement:

- Measuring path for the functions level measurement, FFT, Wow& Flutter

The signal is taken via the joint LEV directly to the function switch with N608, D606 (D606-A = On) and is available at X600, ANALOG OUT in inverted form for further processing in the ADC board.

- Measuring path analog notch filter for the functions RMS, THD, THD+N, MOD DIST
The analog notch filter is automatically cut in by the DSP test routine according to the value of the signal distortions to be measured (see also section 6.1.1, page 6.1). With a later UPD software version, it can also be manually cut into the measuring path in the modes RMS level and FFT with a post-amplification of 0, 12 or 30 dB.

It is designed according to the principle of the *state variable filter* and consists of two circuit groups:

- * The first filter section (circuit diagram sheet 7) contains a frequency-tunable bandpass with fixed quality Q1 (N705 ... N707). It is tuned to the fundamental of the input signal. The output signal at N706.6 mainly contains the fundamental with a phase shift of 180° with respect to the input. By addition with the input signal via R715, R717 and the inverting amplifier N708, the fundamental is subtracted. The residual signal is amplified by 0, 12 or 30 dB via N708 according to the negative feedback which can be set by means of analog switch D706-C, D. The fundamental is suppressed by more than 30 dB compared with the original signal (output N708.6 X700, NOTCH10UT). Depending on the frequency tuning of the bandpass, the magnitude of the gain deviates slightly from the ideal value 1. For correction, the resistors R706, R708 in conjunction with analog switch D706-A,B are used.
- * Like the first section, the second filter section (NOTCH CORR. FILTER, circuit diagram sheet 6) contains a frequency-tunable bandpass with fixed quality Q2 (N604 ... N607) and is also tuned to the fundamental of the input signal. The output signal at N606.6 (X602) mainly contains the fundamental **without phase shift** and is added to the output of notch filter section 1 via the resistors R609, R619 in the ratio 4,75/11. The NOTCH CORR. FILTER corrects the passband attenuation of the notch filter in the range of the harmonics d2, d3 in order for a high measuring accuracy to be achieved with THD, THD+N measurements.
- * The corrected signal of the two filter paths is taken via the function switch with N608, D606 (D606-C = On) and is available at X600 ANALOG OUT in inverted form for further processing in the ADC board.
- * Notch filter frequency tuning

In both filter paths, the tuning is effected in the same way via fixed capacitors and binary-coded resistor networks via presetting by means of analog switches. In filter path 1, fine tuning is performed by D/A converter D700, D701.

The total notch frequency range 10Hz to 110kHz is subdivided into 5 partial frequency ranges by use of appropriate capacitors.

Table: Notch frequency ranges

Range ¹³	Frequency	Capacity C_i	f_{max} nom.
4	10Hz...70Hz	C4 = 680.39nF	F4 = 75,4Hz
3	68Hz...470Hz	C3 = 100.39nF	F3 = 511Hz
2	430Hz...3260Hz	C2 = 15.39nF	F2 = 3333.3Hz
1	3kHz...22.8kHz	C1 = 2190pF	F1 = 23.42kHz
0	20kHz...110kHz	C0 = 390pF	F0 = 131.54kHz

The actual values of the maximum frequencies are determined by individual calibration (see section Calibration, page 7.12).

The frequency tuning in each partial range is performed with 5 binary-coded resistors

¹³UPD-internal setting

for the most significant bits and a 12-bit D/A converter for the least significant bits. The 12-bit D/A converter determines the fine resolution of the notch frequency. Formula for calculating the notch frequency:

$$f_{notch} = \frac{D}{2^{17}} * \frac{1}{2 * \Pi * C_i * R0/2}$$

with f in Hz, C in F

$R0 = 6205\Omega$ corresponds to the greatest value R724, R725 of the R - networks + analog switch ON resistor

Binary setting code D with given nominal frequency from the measurement with PFC, DSP routine or specification for the appropriate partial ranges:

$$Binarycode = BIN \left(2^{17} * \frac{f_{nom.}}{f_{cal}} \right)$$

Value range: $0 \dots 2^{17} - 1$

The most significant 5 bits for the resistors are output to the filter hardware in *normal* position, the least significant 12 bits ($4096 - D_{low}$) for the D/A converters D700, D701 in inverted form.

The frequency setting of the two notch filter sections is made parallel to the hardware via the same binary code (circuit diagram sheet 9).

D/A converter for fine frequency tuning:

The multiplying 12-bit DAC D700 and D701 use the analog signal at the input VREF to provide a current at the output IOU1, which is proportional to the set bit combination (setting code D_{low}). Together with the opamp N702, N703 and the DAC-internal feedback resistors R_{FB} , inverting output stages are formed.

The following applies to the voltage at the output of opamps N702, N703:

$$V_o = V_i * \left(1 - \frac{D_{low}}{4096} \right)$$

The two signals are fed into the R-C filter stages via resistors R722, R723 according to the binary values.

- Measuring path d2 lowpass for the function DFD-d2

The analog lowpass filter is automatically cut in by the DSP test routine depending on the value of the signal distortions to be measured (see also section 6.1.1, page 6.1 and circuit diagram sheet 6, D2 LOWPASS 1kHz). The lowpass with N600, N601 is an active Cauer filter for attenuation of the difference tone carrier signals above 3.5kHz. The residual output signal at N601.6 LPOUT is taken via the function switch with N608, D606 (D606-B = On) and is available at X600 ANALOG OUT with a 30-dB postamplification for further processing in the ADC board.

All analog functions can be controlled by the AT processor via relays or integrated analog switches via level comparators and latches (see also hardware function table, function 'Serial hardware control interface' in section 7.2.7.1, page 7.75 and circuit diagrams sheet 8, 9).

7.2.8.2 Controlling the Analog Functions

When the UPD is switched on, the analyzer boards are identified by the program by means of their plug-in location and configuration.

- Analog Analyzer 1 with ADC Board:
Board identification 69H, corresponds to Analyzer Board Version 0.01
(see OPTION Panel, modified hardware with D606, circuit diagram sheet 6).
Board identification 68H, earlier Analyzer Board Version 0.00
Bit length = 68, bit stream MSB first,
absolute bit position 48 ... 115,
relative bit position 0 ... 67 (\equiv hardware function table)
- Analog Analyzer 2 without/**with** ADC Board: (with Option UPD-B3 **with** ADC Board)
Board identification 61/**69H**, Analyzer Board Version 0.01,
Board identification 60/**68H**, earlier Board Version 0.00
Bit length = 68, bit stream MSB first

absolute bit position 116 ... 183,
relative bit position 0 ... 67 (\equiv hardware function table),

Hardware function table: Analog Analyzer with ADC board

device	BITS				function
	Pos.	Count	Bitvalue		
D800					
(K200)	.4	0	1	1	1=on,0=BAL or GEN or OFF
(K205)	.5	1	1	1	1=DC-Coupl., 0=AC-Coupl.
(K215)	.6	2	1	1	1=40dB, 0=20dB
(K220)	.7	3	1	1	1=BAL or GEN, 0=UNBAL
(K225)	.14	4	1		1=on, 0=UNBAL or OFF or GEN
(K230)	.13	5	1		1=BAL300Ω or 600Ω
			1		0=BAL20kΩ or USER
(K235)	.12	6	1	1	1=GEN
			1		0=BAL or UNBAL or OFF
	.11	7	1	1	Range high/low 5dB, 10dB
D800	.11				linked with D802.14 PEAK_CMP2
D801					
(K240)	.4	8	1	1	1=BAL 300Ω
			1		0=BAL 600Ω or 20kΩ or USER
(K250)	.5	9	1	1	1=DC-Coupl., 0=AC-Coupl.
(K255)	.6	10	1	1	1=BAL USER
			1		0=BAL 300Ω or 600Ω or 20kΩ
(K265, K430)	.7	11	1	1	1=UNBAL, 0=BAL
(K260)	.14	12	1	1	1=20dB, 0=10dB
(K300)	.13	13	1	1	1=0dB, 0=20 or 40dB
(K345, /K400)	.12	14	1	1	1=20dB, 0=0dB
(K360)	.11	15	1	1	1=0dB, 0=10 or 20dB
D802					
(K405)	.4	16	1	1	1=ATT 5dB, 0=ATT 0dB,
(K410)	.5	17	1	3	0=AMP 5dB, 1=AMP 0dB,
(K415)	.6	18	1		2=AMP 10dB, 4=AMP 20dB
(K420)	.7	19	1		
	.14	20	1	1	Range high/low 5dB, 10dB
D802	.14				linked with D800.11 PEAK_CMP1
(D500, 501)	.13	21	1	1	1=FREQ, 0=DC-MEAS

- continued -

- continued -				
device	BITS			function
	Pos.	Count	Bitvalue	
(N455, V505) .12	22	1	1	0=RESET, 1=MEAS
(N455, V506) .11	23	1	1	0=LOW FRQ, 1=NORMAL
D700, 701 DAC8143	24...35	12		Notch filter frequency part. range fine 12-Bit-DAC, lower bit 0...11 (inverted) of 17 Pos.24: Bit 0= LSB, 1=on Pos.35: Bit 11=MSB, 1=on
D900 N0,W0 .4	36	5		Notch filter frequency Partial range coarse higher bit 12...16 of 17 Pos.36: Bit 12= LSB, 1=on Pos.40: Bit 16= MSB, 1=on
N1,W1 .5	37			
N2,W2 .6	38			
N3,W3 .7	39			
N4,W4 .14	40			
D900 N5,F0 .13	41	4		5 partial frequ. ranges 0=Range 0 (high Freq) 1=Range 1, 2=Range 2
N6,F1 .12	42			
N7,F2 .11	43			
D930 V0,F3 .4	44			8=Range 4 (low Freq)
D930 V1 .5	45	2		Function switch 0=Notchgain 30,01dB 1=Notchgain 0dB, 2=Notchgain 12,01dB
V2 (D706) .6	46			
V3 .7	47	3		5 (6 ¹⁴) =Function LEVEL 0dB 6 (5 ¹⁴) =d2-Meas LPOUT 30dB
V4 (D606) .14	48			
V5 .13	49			0 (3 ¹⁴) =Notch-Corr. Out no function
- .12	50	2		
- .11	51			
D950 .4	52	1		reserved for external filter no function
- .5	53	4		
- .6	54			
- .7	55			
- .14	56			
.13	57	1		1=Aliasfil. MB3, 0=MB2, ADC Board (MB2/3 = ANLG 100/300kHz)

- continued -

- continued -				
device	BITS			function
	Pos.	Count	Bitvalue	
D940	.12	58	1	1=AMP 30dB, 0=AMP 0dB, ADC Bd 1=same Ch, 0=other Ch, ADC Board Board identification (incl. version) is inserted into the data stream with the IAIRD pulse
	.11	59	1	
	.9	60..67	8	

Bit 67 = MSB, end of Analog Analyzer 1. Continuation of bit stream in Analog Analyzer 2 or Data return via Analog Motherboard (Analyzer section) to Digital Analyzer 1 (signal name IAIDI).

7.2.8.3 Measuring Equipment

Sinewave generator	SPN, AFG or AFGU
Digital multimeter	UDL 44 or UDS 5
AC voltmeter	URE 3
Oscilloscope	4-channel digital memory 100 MHz
Frequency counter	

7.2.8.4 Testing, Troubleshooting and Adjustment

- Testing the board identification (BOARD ID)

The byte at the parallel input of shift register D940 (coded with pull_up and pull_down resistors) is referred to as BOARD ID.

BOARD ID of Analog Analyzers 1 and 2:

Board	BOARD ID ¹⁵	
	HW version 0.00	HW version 0.01
Analyzer 1 with ADC Board	01101000B = 68H	01101001B = 69H
Analyzer 2 without ADC Board	01100000B = 60H	01100001B = 61H
Analyzer 2 with ADC Board ¹⁶	01101000B = 68H	01101001B = 69H

In the case of proper functioning of the board identification, the HW version is indicated in the OPTION panel under HARDWARE ANALOG (HW version 0.00 = earlier hardware version).

The BOARD ID is inserted into the serial data stream with the IAIRD pulse and read in by Digital Analyzer 1 during the program start only.

Testing: see Analog Motherboard, pages 7.79, 7.175

7.2.8.5 Disassembly and Assembly

- Remove upper instrument cover and screening cover (front right)
- Pull out the Analog Analyzer boards Ch1 and Ch2 using the levers and disconnect the coaxial connections at the bottom

¹⁴HW-Version 0.00 = earlier hardware version

¹⁵B = binary, H = hexadecimal

¹⁶with Option Highspeed UPD-B3

- For replacement, complete the new board with the ADC board, if necessary (see section 7.2.9, page 7.100) and install in the instrument. Make sure that the cable labelling of the channels is correct and the cables are **not** caught.
- Complete UPD

7.2.8.6 External Interfaces

Coaxial input connector (SMB connector)						
name	Signal description	≡	source dest.	range	connector	comment
UNBAL HI	unbalanced high	I	BNC input	0..300V RMS, 2Hz..300kHz, ±300V DC	X200	SMB, inner conductor
UNBAL LO	unbalanced low	I	BNC input	Reference, floating; 0..25V AC, ±50V DC	X200	SMB, outer conductor

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Motherboard connector (64-contact VG strip)						
name	Signal description	≡	source dest.	range	connector	comment
Test inputs						
BAL2	balanced	I		0..35V RMS, ±35V DC, 2Hz..300kHz	X1.C32	XLR-Input, Pin 2
BAL3	balanced	I		as before	X1.A32	XLR-Input, Pin 3
GEN2	Int. GEN-Connect	I	GEN	0..12V RMS Unbal, 0..24V RMS Bal	X1.C27	Signal from Generator
GEN3	Int. GEN-Connect	I	GEN	as before	X1.A27	to ADC Board
ANALOG IN	from adjacent channel	I		0..3.5V AC	X1.A20	
EXTFIL	from external filter	I		0..3.5V AC	X1.A22	reserved for extension
Test outputs						
FMESS	1.: Freq Rising 2.: DC-f Convert	O		0/5V, 2Hz..300kHz	X1.A16	Freq/Phase DC measurement
PHI MESS	Freq Falling	O		0/5V, 2Hz..300kHz	X1.C14	Freq/Phase
ACAMP	Input Ranging Out	O		0..3.5V AC	X1.C20	to Monitor MB
ANLG OUT	Function Out	O	X600.2	0..3.5V AC	X1.A18, X2.B17	RMS-Level-, Notch-, d2-LP-Out
Supply voltage						
GND A[1]	Analog ground	I		Reference, float.	X1.A24, 25, AC29	Analog Floating Potential
-18V[1]		I		-18V±1V	X1.C23	
+18V[1]		I		+18V±1V	X1.C24	
+6V[1]		I		+6V±0.2V	X1.C25	
GND	Ground	I		0V	X1.A1,17,21,23,26,28 X1.C22,26,28 X1.AC19,30,31	
-15V		I		-15V±0.75V	X1.C15, X2.B13	
+15V		I		+15V±0.75V	X1.C16, X2.A2	
+5V		I		+5V±0.15V	X1.C17	5V Digital
Digital control signals						
IAICK	Clock signal	I		TTL	X1.A13	+edge active Board identification
IAIRD	Read	I		TTL	X1.A15	
WR	Write	I		HCT logic level	X1.C13	H-pulse, L-pulse Ser. data Ser. data Monitor control
LOAD	Load	I			X1.A14	
SDI	Data input	I			X1.C12	
SDO	Data output	O			X1.C11	
PK INTR	Pk-Interrupt	O		0/5V 5V: Input Over	X1.C18	
A/D converter signals						

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
ADS11	Bit11(MSB)	O		TTL	X1.C1	(=X2.B1)
ADS10	Bit10	O		TTL	X1.A2	(=X2.A2)
ADS9	Bit9	O		TTL	X1.C2	(=X2.B2)
ADS8	Bit8	O		TTL	X1.A3	(=X2.A3)
ADS7	Bit7	O		TTL	X1.C3	(=X2.B3)
ADS6	Bit6	O		TTL	X1.A4	(=X2.A4)
ADS5	Bit5	O		TTL	X1.C4	(=X2.B4)
ADS4	Bit4	O		TTL	X1.A5	(=X2.A5)
ADS3	Bit3	O		TTL	X1.C5	(=X2.B5)
ADS2	Bit2	O		TTL	X1.A6	(=X2.A6)
ADS1	Bit1	O		TTL	X1.C6	(=X2.B6)
ADS0	Bit0 (LSB)	O		TTL	X1.A7	(=X2.A7)
EOC	End of Conversion	O		TTL	X1.C7	(=X2.B7) Pulse
SOC	Start of Conversion	I		HCT level	X1.A8	(=X2.A8) Pulse 163ns
L/R	Left/Right	I		HCT level	X1.C8	(=X2.A9) Frame 48kHz
CATP	Reset	I		HCT level	X1.A9	(=X2.B8) Sync. Reset
SCLK	Clock 3.072MHz	I		HCT level	X1.C9	(=X2.A10)
CDATA	Serial Data Out	O		TTL	X1.A10	(=X2.B9)
CLKIN	Operating clock	I	DigAna	L:<1V, H:>4V 6.144MHz	X1.A11	64-Bit/Conversion (=X2.B10)

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

ADC Board multipoint connector (40-contact multipoint connector)						
name	Signal description	≡	source dest.	range	connector	comment
Supply voltage ADC Board						
GND	Ground, ref. to chassis			0V	X2.A1, AB11, X2.AB16,18	
-15V		O		-15V±0.75V	X2.B13	
+15V		O		+15V±0.75V	X2.AB14	
+5V		O		+5V±0.15V	X2.B15	5V Digital
Digital control signals						
ALIAS MB2/3	MB2/3 selection	O		HC level	X2.A12	H: ANLG 300kHz L: ANLG 100kHz
AMP0/30	0/30dB selection	O		HCT level	X2.B12	H: 30dB-Amplif. L: 0dB-Amplif.
SELCHA	Channel selection	O		HCT level	X2.A13	H: Adjacent channel
ADCBID	Board ID	I	ADC Board	0/5V	X2.A15	L: Own channel 5V: with ADC Board
A/D converter signals						
ADS11	Bit11(MSB)	I	ADC Board	TTL	X2.B1	(=X1.C1)
ADS10	Bit10	I	ADC Board	TTL	X2.A2	(=X1.A2)
ADS9	Bit9	I	ADC Board	TTL	X2.B2	(=X1.C2)
ADS8	Bit8	I	ADC Board	TTL	X2.A3	(=X2.A3)
ADS7	Bit7	I	ADC Board	TTL	X2.B3	(=X1.C3)
ADS6	Bit6	I	ADC Board	TTL	X2.A4	(=X1.A4)
ADS5	Bit5	I	ADC Board	TTL	X2.B4	(=X1.C4)
ADS4	Bit4	I	ADC Board	TTL	X2.A5	(=X1.A5)
ADS3	Bit3	I	ADC Board	TTL	X2.B5	(=X1.C5)

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
ADS2	Bit2	I	ADC Board	TTL	X2.A6	(=X1.A6)
ADS1	Bit1	I	ADC Board	TTL	X2.B6	(=X1.C6)
ADS0	Bit0 (LSB)	I	ADC Board	TTL	X2.A7	(=X1.A7)
EOC	End of Conversion	I	ADC Board	TTL	X2.B7	(=X1.C7) Pulse
SOC	Start of Conversion	O	DigAna 1	HCT level	X2.A8	(=X1.A8) Pulse 163ns
L/R	Left/Right	O	DigAna 1	HCT level	X2.A9	(=X1.C8) Frame 48kHz
CATP	Reset	O	DigAna 1	HCT level	X2.B8	(=X1.A9) Sync. Reset
SCLK	Clock 3.072MHz	O	DigAna 1	HCT level	X2.A10	(=X1.C9)
CDATA	Serial Data Out	I	ADC Board	TTL	X2.B9	(=X1.A10) 64-Bit/Conversion
CLKIN	Operating clock	O	DigAna 1	L:<1V, H:>4V 6.144MHz	X2.B10	(=X1.A11)
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

7.2.9 ADC Board

Circuit diagram	1030.9260.01 S
Component location plan	1030.9260
Parts list	1030.9260.01 SA

Circuit diagram overview	
Sheet:	Contents
1/4:	Block diagram
2/4:	Channel selection/attenuation, 30-dB amplifier
3/4:	Aliasing filter ANLG 100/300 kHz/switchover, amplifier 9dB
4/4:	Aliasing filter ANLG 22 kHz, ADC ANLG 22 kHz, ADC ANLG 100/300 kHz, pin assignment

7.2.9.1 Function

The ADC Board is inserted as a subassembly in the Analog Analyzer Ch1/Ch2 ¹⁷.

It contains an input multiplexer with inverting amplifier, an additional 30-dB post-amplifier for the instruments ANLG 100/300 kHz, two A/D converters and associated aliasing lowpass filters for the 3 analog instruments ANLG 22, 100, 300kHz.

- Channel selection

A signal is selected from the two analog inputs ANALOG-OUT, ANALOG-IN via the input multiplexer N100 and attenuated by 6 dB in the operational amplifier N105. In Analog Analyzer CH1, the signal ANALOG-OUT comes from its own channel, whereas the signal ANALOG-IN is derived from channel 2 in the basic UPD model. If UPD-B3 is fitted, only the signals from ANALOG-OUT are passed on for both channels.

- 30-dB amplifier

The post-amplifier N115 is used to increase the sensitivity in the level ranges 1...10mV with the instruments ANLG 100/300 kHz and is cut in via analog switches N110, N120.

- Aliasing filter and ADC for ANLG 22 kHz

The signal at X101 is applied to a 1-stage lowpass R300, C308. In conjunction with the amplifier N300 and its frequency-dependent circuitry, it constitutes the analog aliasing lowpass for the audio ADC D300. The 3-dB cutoff frequency of the lowpass is about 150kHz. N300 is simultaneously used as buffer amplifier for the high input capacitances C301, C302 at the L/R inputs of the ADC. The buffer stage delivers the same signal to the L/R inputs (test points X303).

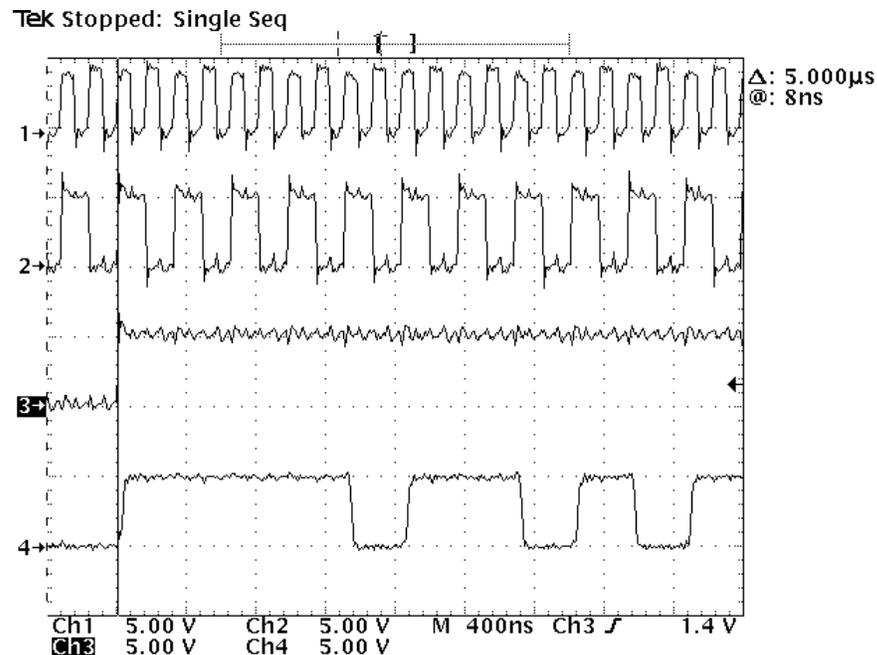
The delta-sigma A/D converter D300 operates with an internal sampling rate of 3.072 MHz (SCLK) and 64-fold oversampling and achieves a resolution of 18 bits for the internal stereo channels L, R. The output data rate is 48 kHz, corresponding to the *FRAME* frequency at the L/R connector of D300. When the UPD is switched on, the control line CATP is used to perform a reset for the ADC that is synchronous with the 6.144-MHz operating clock CLKIN. With CATP = logic H (+5V), the ADC is switched off if it is not used (instruments ANLG 100/300 kHz).

The data traffic is handled via the serial interface SCLK, L/R, CDATA controlled by the Digital Analyzer via the Analog Motherboard. After reading out the converted data of the left and

¹⁷in the case of Ch2 only with the Option Highspeed UPD-B3

right ADC channel with 18 bits each, the two data words are added in the DSP. The result is an increased resolution of 19 bits.

Oscilloscope with ADC signal traces:



Trace 1: CLKIN, Trace 2: SCLK, Trace 3: L/R, Trace 4: CDATA

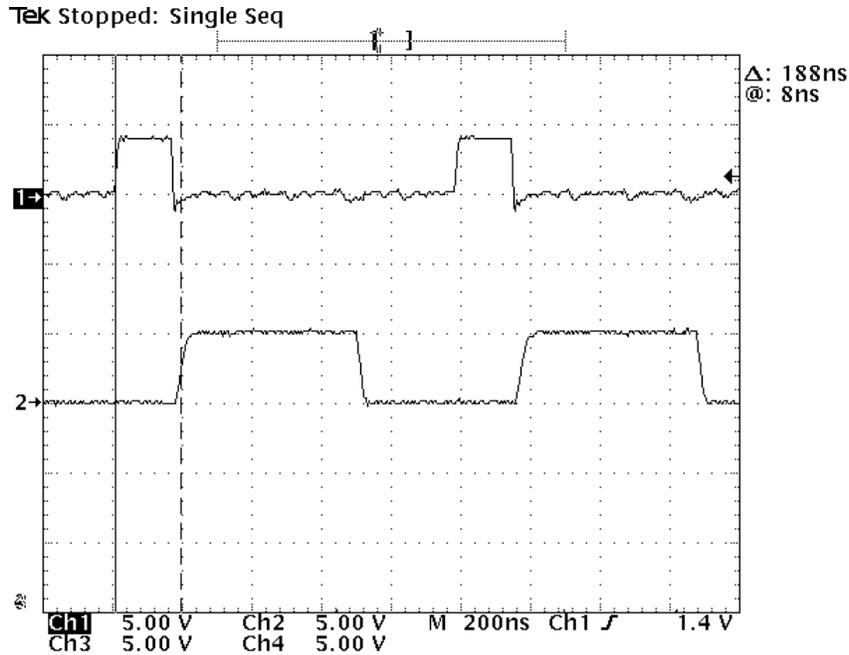
- Aliasing filter and switchover to ANLG 100/300 kHz
The aliasing filters MB2 and MB3 cause a steep-edged band limiting of the analog signals ahead of the fast A/D converter for the instruments ANLG 100kHz and 300kHz. The 7th-order lowpass filters are designed in FDNR structure and feature a very low ripple in the passband up to the cutoff frequency of 100 kHz or 300 kHz. The frequency response is adjusted at 20 kHz using the trimmers C215, C216. The stopbands are specified with 70-dB attenuation for $f_s > 241$ kHz for ANLG 100 kHz and $f_s > 700$ kHz for ANLG 300 kHz.

Both lowpass filters feature a transmission loss of 6 dB and are provided with an output buffer N230, N270 each. Depending on the selected analog instrument, the associated filter is connected via control line ALIAS MB2/3 and analog switch N275 to driver amplifier N200 (9.5-dB gain) to the A/D converter D350.

- ADC for ANLG 100/300 kHz
For A/D conversion in the instruments ANLG 100 kHz and 300 kHz the 12-bit ADC D350 is used. The signal is sampled with the clock of the start/conversion signals SOC of the conversion. The clock is generated in Digital Analyzer 1 - it is 341.33 kHz for ANLG 100 kHz and 1024 kHz for ANLG 300 kHz. When the ADC is inactive (e. g. with ANLG 22 kHz), the conversion clock remains deactivated.

The rising edge of the SOC pulse starts the A/D conversion. The ready signal EOC from D350 signals the correct end of a conversion cycle with the rising edge and provides an interrupt to the DSP in the Digital Analyzer 1 or 2, causing it to read the 12-bit data word from the ADC D350 in parallel.

Oscilloscope with ADC signal traces (for 1024kHz):



Trace 1: SOC, Trace 2: EOC

Cursor —: starting conversion, Cursor - - - -: End of previous conversion

7.2.9.2 Disassembly and Assembly

- Remove Analog Analyzer Ch1 or Ch2, respectively (see section 7.2.8.5, page 7.95)
- Unscrew the smaller screening cover on the component side
- Remove the 2 screws at the rear
- Pull out the ADC board towards the top making sure not to bend the connector pins
- Install new board and complete the module

7.2.9.3 External Interfaces

Connector to Analog Analyzer (40-contact pin strip)						
name	Signal description		source dest.	range	connector	comment
Test inputs						
ANALG OUT	Function Out			0...3.5V AC	X3.17	Own channel
ANALOG IN	Function Out			0...3.5V AC	X2.19	Adjacent channel
Control signals						
ALIAS MB2/3	MB2/3-selection			HCT level	X2.12	H: MB3 300kHz L: MB2 100kHz
AMP0/30dB	0/30dB selection			HCT level	X3.12	H: 30dB-Amplif. L: 0dB-Amplif.
- continued -						

- continued -							
name	Signal description	≡	source dest.	range	connector	comment	
SELCHA	Channel selection	I		HCT level	X2.13	H: Adjacent channel	
5V	ADC board ID	O		0/5V	X3.15	L: Own channel with ADC-Bd	
AD converter signals							
ADS11	Bit11(MSB)	O		TTL	X3.1	12-Bit DAC	
ADS10	Bit10	O		TTL	X2.2		
ADS9	Bit9	O		TTL	X3.2		
ADS8	Bit8	O		TTL	X2.3		
ADS7	Bit7	O		TTL	X3.3		
ADS6	Bit6	O		TTL	X2.4		
ADS5	Bit5	O		TTL	X3.4		
ADS4	Bit4	O		TTL	X2.5		
ADS3	Bit3	O		TTL	X3.5		
ADS2	Bit2	O		TTL	X2.6		
ADS1	Bit1	O		TTL	X3.6		
ADS0	Bit0 (LSB)	O		TTL	X2.7		
EOC	End of Conv.	O		TTL	X3.7		Pulse Pulse 163ns
SOC	Start of Conv.	I		HCT level	X2.8		
L/R	Left/Right	I		HCT level	X2.9	Frame 48kHz	
CATP	Reset	I		HCT level	X3.8	Sync. Reset	
SCLK	Ser. Data Clk	I		HCT level	X2.10	3.072MHz	
CDATA	Ser. Data Out	O		TTL	X3.9	64-Bit/Conversion	
CLKIN	Operating clock	I		L:<1V, H:>4V	X3.10	6.144MHz	
Supply voltage							
GND[D]	Ground			0V	X2.1,11	Digital	
-15V		I		-15V±0.75V	X3.11	5V Digital	
+15V		I		+15V±0.75V	X3.13		
+5V		I		+5V±0.15V	X2.14,X3.14		
GND[A]	Analog ground			0V	X3.15		
					X2.16,18,20		
					X3.16,18,20		
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power							

7.3 Analog-Generator

7.3.1 Overview

7.3.1.1 Signal Generation

In its basic version, the Analog Generator consists of the two modules DAC Board and Output Circuit. This basic version is referred to as universal generator.

- DAC Board:
 - Signal generation with D/A converter and lowpass filter
 - Squarewave generation
- Output Circuit:
 - Level setting
 - Balanced and unbalanced output stage
 - Channel switching
 - Impedances

With the Option UPD-B1 Low Distortion Generator installed:

- SINE, MODDIST and DFD with better S/N ratio
- DIM signal can be generated

7.3.1.2 Differences between the 25-kHz and 110-kHz Generators

In the basic generator version, all signals are generated on the DAC board.

Depending on the selected generator (ANLG 25 kHz or ANLG 110 kHz), the clock frequency of the signal D/A converter is set and the associated lowpass filter cut in:

Generator	Converter clock	Lowpass	Signal frequency
ANLG 25 kHz	96 kHz	25 kHz	2 Hz to 25 kHz
ANLG 110 kHz	384 kHz	110 kHz	2 Hz to 110 kHz

If the Low Distortion Oscillator is installed and switched on, the sinewave signal is generated in this module and applied to the Output Circuit instead of the signal from the DAC Board. Irrespective of the generator selected (25 kHz or 110 kHz), the same circuit parts are always used, i.e. there is only one Low Distortion Oscillator for both generators.

Further signal processing on the Output Circuit is always the same.

For generation of two-tone signals (DFD, MODDIST or DIM) with the Low Dist Generator, the two signal components (one from the DAC Board, the other one from the Low Dist Gen) are added in the Output Circuit by means of the SIGNAL ADDER circuit. The D/A converter and the lowpass filter on the DAC board are configured according to the generator selected.

For further signal processing, additional circuits for filtering the signal are used on the DAC Board and Output Circuit, and an additional circuit for level setting is cut in on the Low Dist Generator (see next section Level Tables).

7.3.1.3 Level Tables

The following tables can be used to check the generation of the various signals on the various modules.

The voltage and frequency values indicated apply to a calibrated Analog Generator. Without calibration, all voltages and the frequency of the Low Dist Generator may deviate from the nominal value by the permissible tolerance of the respective calibration factor. (Tolerances see section Adjustment and Calibration, page 7.123 pp.)

1. Signal generation without Low Distortion Generator

Level table for Universal Generator: Sinewave and two-tone signals						
Module	Test points		V_{pk}	SINE	DFD	MODDIST
	Gen 25	Gen 110		V_{rms}	V_{rms}	V_{rms} (4:1)
DAC Board	X30	X30	2.87	2.03	1.43	1.67
	P32	P42	2.87	2.03	1.43	1.67
	X34	X44	2.87	2.03	1.43	1.67
	P34	P44	3.48	2.46	1.74	2.03
	P35	P45	3.48	2.46	1.74	2.03
Output Circuit	X300		3.48	2.46	1.75	2.03
	X301		3.00	2.12	1.50	1.74
	X402		6.00	4.24	3.00	3.48
	X700, 701		6.00	4.24	3.00	3.48
	X800, 801		1.50	1.06	0.75	0.87
Generator setting			Instrument Channel(s)	ANLG 25kHz and 110kHz 1		
			Output Impedance	UNBAL 15Ω		
			Function	SINE		
			Low Dist	OFF		
			Frequency	1.000kHz		
			Voltage	3.000Vpp		
			Function	DFD		
			Low Dist	OFF		
			Mean Freq	14.000kHz		
			Diff Freq	800Hz		
			Voltage	3.000Vpp		
			Function	MODDIST		
			Low Dist	OFF		
			Upper Freq	7.000kHz		
			Lower Freq	400Hz		
			Total Volt	3.0000 Vpp		
			Volt LF:UF	4:1		

Tolerance SINE ±1% max, ±0.25% typ
 DFD, MODDIST ±5% max, ±2% typ

DFD signal: The HP DIFF on the Output Circuit is cut in

Level table for Universal Generator: Squarewave signal		
Module	Test point	Signal
DAC Board	X50	$2.46V_{rms}$ 2kHz Sine
	N500.7	$5V_{pp}$ 2kHz Square
	X54	$5V_{pp}$ 1kHz ∴
	X55	$5V_{pp}$ ∴ ∴
	N502.1	$4.75V_{pp}$ ∴
	N502.7	$5.3V_{pp}$
Output Circuit	X300	$5.3V_{pp}$ ($=2.6V_{rms}$)
	X301	$2V_{rms}$
	X402	$4V_{rms}$
	X700, 701	$4V_{rms}$
	X800, 801	$1V_{rms}$
	Generator setting:	

Tolerance $\pm 7.5\%$ max to X300
 $\pm 5\%$ max, $\pm 1\%$ typ from X301

2. SINE with Low Distortion Generator

The signal from the Low Distortion Generator is applied to the Level CONTROL circuit on the Output Circuit instead of the signal from the DAC Board.

Level table for SINE with Low Distortion Generator		
Module	Test point	Voltage (V_{rms})
Low Dist Gen	P30, P31, P34	2.70
	X2	2.70
	P21	2.64
Output Circuit	X300	$2.64V_{rms}$
	X301	$2.00V_{rms}$
	X402	$4.00V_{rms}$
	X700, 701	$4.00V_{rms}$
	X800, 801	$1.00V_{rms}$
Generator setting:		Instrument ANLG 110kHz Channel(s) 1 Output UNBAL Impedance 15Ω Function SINE Low Dist ON Frequency 1.000kHz Settling FAST Voltage 1.000V

Tolerance $\pm 6.5\%$ max, $\pm 3\%$ typ to X300
 $\pm 1\%$ max, $\pm 0.25\%$ typ from X301

3. MODDIST with Low Distortion Generator

The sinewave signal from the DAC board passes a lowpass filter in order to improve the S/N ratio in the vicinity of the higher-frequency signal coming from the Low Dist Generator.

Signal from	Frequency range	Filter	Level setting in	Signal Adder
Dac Board	30Hz ... 500Hz	LP SMPTE	SIGNAL DAC	0dB
Low Dist	4kHz ... 110kHz	—	IMD ATTEN	-6dB

Level table for MODDIST with Low Distortion Generator		
Module	Test point	Signals
DAC Board	X30	$1.62V_{rms}$ 400Hz
	P32	$1.62V_{rms}$
	X34	$1.62V_{rms}$
	P34	$1.97V_{rms}$
	P35	$1.97V_{rms}$
	X60	$1.97V_{rms}$
	P61	$1.96V_{rms}$
Low Dist Gen	X2	$2.70V_{rms}$ 7.00kHz
	P21	$0.98V_{rms}$
Output Circuit	X202	$1.96V_{rms}$ 400Hz Sine
	X200	$0.98V_{rms}$ 7.00kHz Sine
	X300	$2.03V_{rms}$ $3.48V_{pk}$ MODDIST
	X301	$1.74V_{rms}$
	X402	$3.48V_{rms}$
	X700, 701	$3.48V_{rms}$
X800, 801	$0.87V_{rms}$	
Generator setting:		Instrument ANLG 25kHz
		Channel(s) 1
		Output UNBAL
		Impedance 15Ω
		Function MODDIST
		Low Dist ON
		Upper Freq 7.000kHz
		Lower Freq 400Hz
		Settling FAST
		Total Volt 3.0000 Vpp
		Volt LF:UF 4:1

Tolerance DAC Board $\pm 1\%$ max, $\pm 0.25\%$ typ to X60
 $\pm 5\%$ max, $\pm 3\%$ typ to X202
 Low Dist $\pm 6.5\%$ max, $\pm 3\%$ typ to X200
 MODDIST $\pm 5\%$ max, $\pm 2\%$ typ from X301

In the case of the MODDIST signal, the level of the single components at the input of the Output Circuit also depends on the set voltage ratio LF:RF. The peak value at X300 after the adder on the Output Circuit is always the same: 3.48 V.

Volt LF:RF	X202	X200	Voltage at X300	
	V_{rms}	V_{rms}	V_{pk}	V_{rms}
1:1	1.23	2.46	3.48	1.74
2:1	1.64	1.64	3.48	1.83
4:1	1.96	0.98	3.48	2.02
10:1	2.24	0.45	3.48	2.26
Tolerance: $\pm 5\%$ max., $\pm 2\%$ typ.				

4. DFD with Low Distortion Generator

The sinewave signal from the DAC board passes a highpass filter to improve the S/N ratio with DFD d2. The Low Dist Gen provides the higher-frequency signal.

Signal from	Frequency range	Filter	Level setting in	Signal adder
Dac Board	5kHz ... 110kHz	HP DIFF	—	-6dB
Low Dist	5kHz ... 110kHz	—	IMD ATTEN	-6dB

The two single signals are of the same value, the level setting in IMD ATTEN is therefore ≈ 0 dB. The difference between the two frequencies is 80 Hz to 1 kHz.

Level table for DFD with Low Distortion Generator				
Module	Test point	Signals		
DAC Board	X30	2.03V _{rms}	13.6kHz	Sine
	P42	2.03V _{rms}	∴	∴
	X44	2.03V _{rms}	∴	
	P44	2.46V _{rms}		
	P45	2.46V _{rms}		
Low Dist Gen	X2	2.70V _{rms}	14.4kHz	Sine
	P21	2.46V _{rms}		
Output Circuit	X202	2.46V _{rms}	13.6kHz	Sine
	X200	2.46V _{rms}	14.4kHz	Sine
	N201.6	2.44V _{rms}	13.6kHz	Sine
	X300	1.74V _{rms}	3.48V _{pk}	DFD
	X301	1.50V _{rms}		
	X402	3.00V _{rms}		
	X700, 701	3.00V _{rms}		
	X800, 801	0.75V _{rms}		
Generator setting:		Instrument	ANLG 110kHz	
		Channel(s)	1	
		Output	UNBAL	
		Impedance	15Ω	
		Function	DFD	
		Low Dist	ON	
		Mean Freq	14.000kHz	
		Diff Freq	800Hz	
		Settling	PRECISION	
		Total Volt	3.0000 Vpp	

Tolerance	DAC Board	±1% max, ±0.25% typ	to X202
	Low Dist	±6.5% max, ±3% typ	to X200
	DFD	±5% max, ±2% typ	from X301

5. DIM (only with Low Distortion Generator)

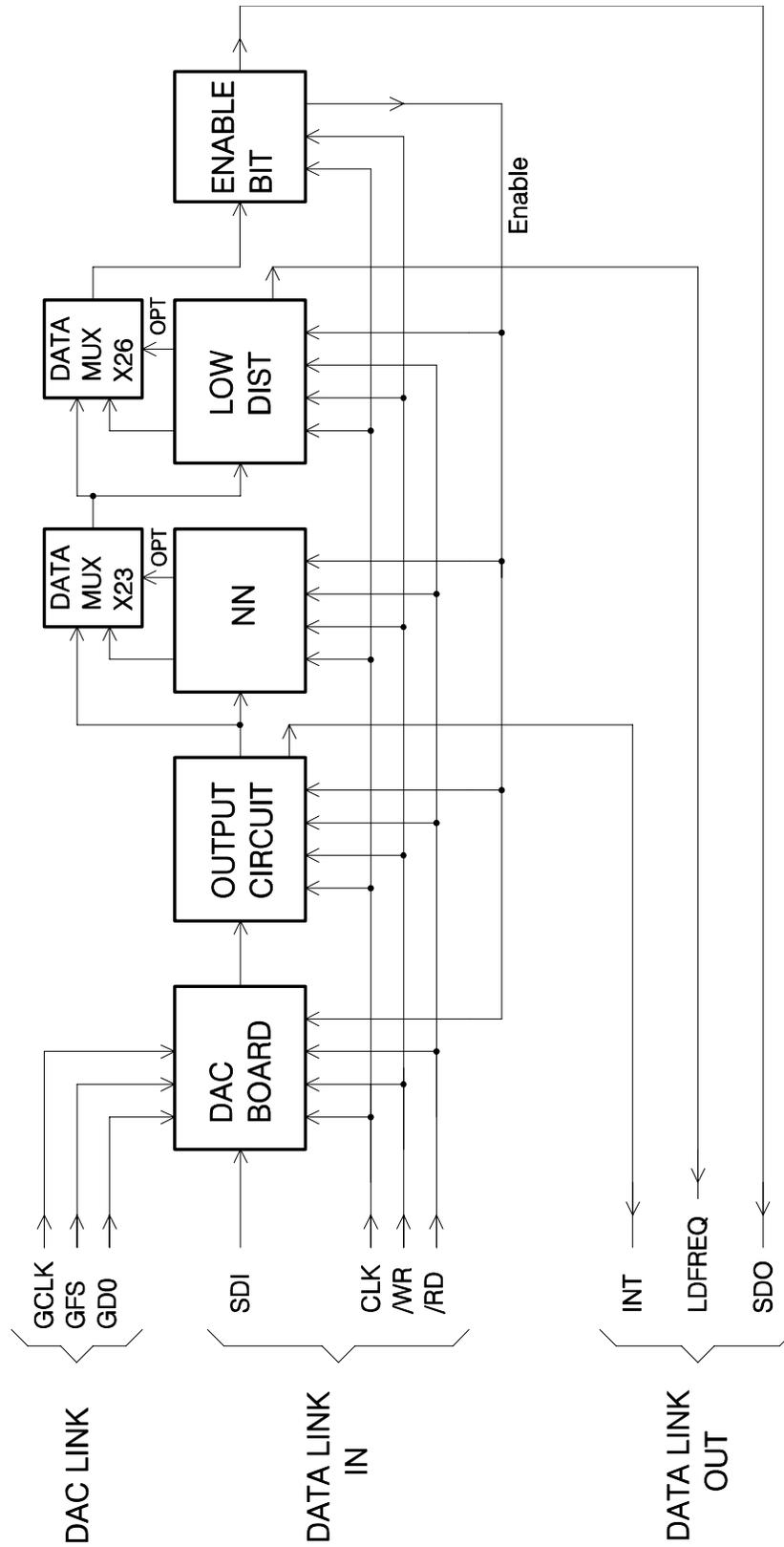
The DAC Board delivers the squarewave signal with the standard band limiting of 30 kHz or 100 kHz (LP DIM), the Low Dist Generator provides the higher-frequency sinewave signal.

Signal from	Frequency range	Filter	Level setting in	Signal adder
Dac Board	2.96kHz / 3.15kHz	LP DIM	—	0dB
Low Dist	14kHz / 15kHz	—	IMD ATTEN	-6dB

The amplitude ratio between squarewave and sinewave signal is permanently set to 4:1 according to the standard. The level setting in IMD ATTEN is ≈ -9.2dB.

Level table for DIM (only with Low Distortion Generator)		
Module	Test point	Signals
DAC Board	X30	2.03V _{rms} 6.30kHz Sine
	P32	2.03V _{rms} ∴ ∴
	X34	2.03V _{rms} ∴
	P35	2.46V _{rms}
	X50	2.46V _{rms} 6.30kHz Sine
	X60	2.58V _{rms} 3.15kHz Square
Low Dist Gen	X2	2.70V _{rms} 15.00kHz Sine
	P21	0.92V _{rms} 15.00kHz Sine
Output Circuit	X202	2.58V _{rms} 3.15kHz Square
	X200	0.92V _{rms} 15.0kHz Sine
	X300	2.62V _{rms} 3.30V _{pk} DIM
	X301	1.98V _{rms}
	X402	3.96V _{rms}
	X700, 701	3.96V _{rms}
	X800, 801	0.99V _{rms}
	Generator setting:	

Tolerance	DAC Board	±7.5% max	to X202
	Low Dist	±6.5% max, ±3% typ	to X200
	DIM	±5% max, ±2% typ	from X301



Ansteuerung des Analog Generators (Analog Generator Control)

7.3.1.4 Controlling the Analog Generator

The preceding block diagram shows controlling of the generator.

The Digital Generator is connected to the Analog Generator via the 16-contact flat cable W32, controlling it via two serial interfaces:

- DAC LINK: Control of the signal D/A converter
- DATA LINK: Setting of the analog functions

Due to the floating design of the entire generator, all data signals must be routed via an optocoupler. The modules DAC Board, Output Circuit and Low Dist are inserted in the Analog Motherboard, all the other circuit components are accommodated on the Motherboard itself.

7.3.1.5 Error Messages

1. Error in board ID

During the selftest after switching on of the UPD, the board IDs of all boards are checked.

The board ID is a version identification for the analog hardware, ensuring that the hardware and software version are always compatible.

(a) Reading in and testing of the board ID

- The entire shift register chain is filled with zeroes.
- With the \overline{RD} pulse, the board IDs of all generator boards are inserted into the data stream.
- The Digital Generator reads in the data stream.
The board IDs come in the following sequence:
 - Low Dist Generator (if fitted)
 - Output Circuit
 - DAC Board
- Evaluation
Only the first faulty board can be identified as faulty. All further boards will also be reported to be faulty even if they are okay.
All preceding boards have been identified correctly. No messages are issued in this case.

(b) Error in the universal generator (Low Dist Gen not fitted)

The following error messages may be caused:

- DAC Board: Error in board ID
Output Circuit has been identified correctly
Error: - in remaining data stream of Output Circuit:
(may be interrupted;
or SDO line is applied to 0 or 1)
- Faulty board ID in DAC Board
- Output Circuit: Error in board ID
DAC Board: Error in board ID
No analog generator boards detected

- Fault:
- Board ID of Output Circuit faulty
 - Error in data stream ahead of Output Circuit
Check data multiplexers X23 and X26 on the Analog Motherboard. The control line OPT[G] must be applied to 0, so that the data stream is through-connected.
Check ENABLE BIT circuit on the Analog Motherboard
 - Check optocoupler for SD0[D]

Testing of the read-in process for the board IDs is described with the Analog Motherboard Generator, see page 7.175.

After completion of the selftest, the following error messages appear (only if an Analog Generator was activated before switch-off and is switched on again now):

Error
DAC-Board not present;
hardware setting impossible
Press ENTER

(also for Output Circuit)

During further operation of the generator via the panel, no more error messages will be displayed.

Transmission of the bit stream for the Analog Generator, however, is faulty or missing. For troubleshooting on the Generator boards, however, the correct data stream must be sent for all installed boards. Therefore, all installed boards must be initialized, i.e. the software assumes them to be available then.

This procedure is to be performed in service mode as described in section Service Mode, page 7.166.

(c) Error with Low Dist Generator installed

The Low Dist Generator being an option (which need not necessarily be fitted), its absence or a faulty board ID cannot be detected as an error. In this case, the following error messages occur:

```
Output Circuit: Error in board ID
DAC Board: Error in board ID
No analog generator boards detected
```

In this case, the fault has to be located first:

- in the Universal Generator (DAC Board and Output Circuit)
- or in the Low Dist Generator

Perform the following test:

- Remove Low Dist Generator
- Switch on UPD: The selftest is executed
- Selftest ok: ⇒ Error in Low Dist Gen
- Selftest faulty: ⇒ Error in Universal Generator.
First eliminate this error, then reinstall the Low Dist Gen.

2. Error messages: Calibration data
 - The calibration factors in the files AGEN.CAL or LDG.CAL on the hard disk or in the CMOS RAM are faulty
 - The calibration factors in the files are out of tolerance

See section Adjustment and Calibration, page 7.118.

3. Error messages during calibration of Low Dist Gen

See section Adjustment and Calibration, page 7.128.

4. Error message: Option LOW DISTORTION is not installed

```
Option LOW DISTORTION is not installed!
Input will be switched to valid setting
Press ENTER
```

This error message always occurs if a function is selected in the generator panel with Low Dist Generator, and the latter is not installed or has not been identified by the software.

If the Low Dist Gen is installed and the selftest performed without faults, the following error will probably be involved:

Data multiplexer X26 on the Analog Motherboard is not switched correctly. The control line OPT[G] must be applied to +5 V.

7.3.1.6 Troubleshooting

- Fault during selftest: Error in board ID
 - Check the coding of the board IDs at the input of the boards (see circuit diagrams)
 - Check DATA LINK (see Analog Motherboard Generator)
 - Check the operating voltages (see Analog Motherboard Generator)
- The generator is not set correctly, e.g.
 - Frequency faulty with Low Dist Generator
 - Level faulty
 - Channel switching faulty
 -

The selftest has been performed without error messages for the generator, i.e. the boards have been identified correctly.

- Data lines, clock, \overline{RD} are okay, since the selftest would otherwise have signalled an error (Error in board ID
- Check the \overline{WR} pulse

- Check the ENABLE BIT circuit: `ENABLE[G]` must be 1

For checking the DATA LINK see Analog Motherboard Generator

If the DATA LINK is okay, the signals on the boards must be tested:

Generator setting	Instrument	ANLG 25kHz and 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	OFF
	Frequency	1.000kHz
	Voltage	1.000V

- GEN 25kHz ok, GEN 110kHz faulty
 - ⇒ Error in DAC Board: Lowpass 110kHz
- GEN 110kHz ok, GEN 25kHz faulty
 - ⇒ Error in DAC Board: Lowpass 110kHz
- If one of the two generators works, the Output Circuit is okay.
- Both generators faulty
 - Switch on Low Dist Generator
 - Signal okay: ⇒ Error in DAC Board
 - Signal faulty ⇒ Error in Output Circuit
- For further troubleshooting check the signal path
 1. Check the signal on the Low Dist Generator
 2. Check the signal at the output of the signal D/A converter on the DAC Board:
 - faulty: Check the DAC LINK from the Digital Generator to the DAC Board
 - okay: trace the signal further
 3. Trace the signal on the DAC Board and Output Circuit by way of the level tables.

Level tables for the entire generator see page 7.105 pp., for the Output Circuit see page 7.204 pp.

7.3.2 Module Replacement

The Analog Generator consists of the following boards:

A25	DAC Board	1030.9460.02	
A24	Output Circuit	1030.9290.02	
A26	Low Dist Generator	1031.2699.02	Option UPD-B1

These boards are accommodated behind the output connectors in the analog section of the UPD and are inserted in the Analog Motherboard (A10, 1030.9060.02).

For troubleshooting, the boards can be operated on adapter cards (included in Service Kit). After removing the shielding covers, the component and solder side are accessible for measurements. In this operating status, however, data integrity of the generator is not guaranteed!

CAUTION: None of the three boards of the Analog Generator can be replaced independently of the other ones without subsequent adjustment and calibration.

NOTE: Replacement of the Analog Motherboard (see page 7.5) does not affect the characteristics of the generator.

7.3.2.1 Disassembly and Assembly

- Pull the power plug of the UPD.
- Unscrew the feet on the rear of the instrument. (four Phillips screws).
- Slide the upper panelling slightly towards the rear and then lift off.
- Remove the cover of the analog section (on the right as viewed from the front).
- Unscrew the support from the middle partition (not necessary when replacing only the Output Circuit)
- Swivel the lever towards the top and pull out the board towards the top.
- For replacement proceed in the reverse order.

7.3.2.2 Adjustment and calibration after module replacement

Adjustment and calibration after module replacement			replaced module		
			Output Circuit	DAC Board	Low Dist
Adjustment	GEN 25kHz	LF	—	○	—
		FDNR	—	○	—
		RF	—	○	—
		Offset	●	●	—
	GEN 110kHz	LF	—	○	—
		FDNR	—	○	—
		RF	—	○	—
		Offset	●	●	—
	Low Dist Gen	RF	—	—	○
Calibration	Gen Anlg25 Level		●	●	—
	Gen Anlg110 Level		●	●	—
	Square Level		●	●	—
	LDG Sin Level		●	—	●
	LDG IMD Level		●	—	●
	LDG Frequency		—	—	●
execute ● check ○					

If the replaced modules are **not** pre-adjusted, the adjustment procedures marked by ○ must also be performed.

Effect of calibration factors

The following table indicates the module and the circuit part where the calibration factors are effective:

Calibration factor	Module	Circuit
Gen Anlg25 Level	DAC Board	Signal D/A converter
Gen Anlg110 Level	DAC Board	Signal D/A converter
Square Level	Output Circuit	LEVEL CONTROL
LDG Sine Level	Output Circuit	LEVEL CONTROL
LDG IMD Level	Low Dist Gen	IMD ATTEN
LDG Frequency	Low Dist Gen	INTEGRATOR 1 and 2

7.3.3 Adjustment and Calibration

7.3.3.1 General Information

- Preparing the Instrument
 - Connect external keyboard (for editing the files with the calibration data)
 - Remove upper panelling and cover of the analog section
 - All modules remain inside the UPD unless otherwise specified
 - Ambient temperature 23 ± 5 °C
 - Warmup time of the UPD:
 - 1 hour for adjustment and calibration of Universal Generator
 - 2 hours for calibration of Low Distortion Generator
- Universal generator
 - Calibration : Level accuracy
 - Adjustment: Frequency response, DC offset

The 25-kHz and 110-kHz generators can be adjusted and calibrated **independently of each other**.
- Low Distortion Generator
 - Calibration: Level accuracy, frequency accuracy
 - Adjustment: Frequency response

For calibration of the Low Distortion Generator, a calibration routine is available, which is executed automatically after it has been called up in the OPTIONS panel.
- Calibration factors

The calibration factors (abbreviated by CF in the following) are stored:

 - in files on the hard disk
 - C:\UPD\REF\AGEN.CAL for the Universal Generator
 - C:\UPD\REF\LDG.CAL for the Low Distortion Generator
 - in the CMOS-RAM on the Digital Generator

AGEN.CAL		
1.01308010	// CF_25	Gen Anlg25 Level
1.00762000	// CF_110	Gen Anlg110 Level
0.98201000	// CF_sqr	Square Level
LDG.CAL		
1.02923000	// CF_ldg_sin	Sin Level
0.99802000	// CF_ldg_imd	IMD Level
1.00510000	// CF_ldg_frq[0]	Freq Range 0 (at 50kHz)
0.99721000	// CF_ldg_frq[1]	Freq Range 1 (at 10kHz)
1.99320000	// CF_ldg_frq[2]	Freq Range 2 (at 1kHz)
1.00123400	// CF_ldg_frq[3]	Freq Range 3 (at 100Hz)

The sequence of the calibration factors in the files AGEN.CAL and LDG.CAL **must** be maintained.

When the UPD is started, the calibration data are read in and checked for compliance with the permissible tolerances during the selftest. When the tolerance is exceeded, an error message is displayed (see page 7.120).

If the generator is not calibrated, all calibration factors are $CF = 1.0000$. If the generator has already been calibrated, which will probably be the case, the files usually contain calibration data with $CF \neq 1$.

Except for the files with the calibration data, the file `AGEN_UN.CAL` containing all calibration factors $CF = 1.0000$ is also provided. Before recalibrating the universal generator completely, this file can be copied to `AGEN.CAL`:

⇒ the generator is thus not calibrated (all $CF=1.0000$).

As the Low Distortion Generator is calibrated automatically, there is no corresponding file `LDG_UN.CAL`. If an error occurs during calibration of the Low Dist Generator, (e.g. one or more calibration factors may be out of tolerance), `LDG.CAL` is not changed, but a new file `LDG_ER.CAL` is produced, containing all calibration factors - also the faulty ones. Knowledge of the faulty calibration factors permits rough error location.

- Recalibration of Universal Generator

- Quit UPD (Front panel: Key 'SYSTEM', Keyboard: <ctrl>F9)
- Change to directory `C:\UPD\REF`
- Copy `AGEN_UN.CAL` → `AGEN.CAL` (⇒ all CF → 1.0000)
If, e.g., only a particular calibration factor is to be redetermined, only this calibration factor can be set to 1.0000 by editing the file `AGEN.CAL`.
- Restart UPD
- Perform calibration measurements and calculate calibration factors:
 $CF = \text{nominal value} / \text{measured value}$
- Quit UPD
- Enter new calibration factors $CF(\text{new})$ in `AGEN.CAL`
- Restart UPD

NOTE: If, during the measurement, the old CF was $\neq 1$, it must be considered as follows: $CF(\text{new}) = CF(\text{old}) * \text{nominal value} / \text{measured value}$

- Recalibration of Low Distortion Generator

Calling the calibration routine:

Select 'LOW DIST' in the `OPTIONS` panel in line `CAL GEN`

7.3.3.2 Error Messages during the Selftest

When the UPD is started, the calibration data are read in and checked for compliance with the permissible tolerances during the selftest. In the case of faulty files or exceeding of the tolerance, the following error messages are produced:

- Cannot open calibration file AGEN.CAL
 CANCEL: Run Generator uncal, ENTER: Restore old AGEN.CAL from CMOS-RAM
 The file AGEN.CAL does not exist, or it contains too little or too many calibration factors CF
 CANCEL: Generator not calibrated, all CF = 1.0, AGEN.CAL unchanged
 All CF → 1
 The file AGEN.CAL is **not** changed
 The selftest is continued
 ENTER: If the CMOS RAM contains valid CF, the file AGEN.CAL is generated. It contains the previous CF from the CMOS RAM. The UPD may again be calibrated correctly.
 The selftest is continued.
 If the CMOS RAM does not contain any valid CF, the following error message is displayed:
 No valid calibration data in CMOS-RAM
 Generator not calibrated, all CF = 1.0, AGEN.CAL unchanged
 All CF → 1
 The file AGEN.CAL is **not** changed
 The selftest is continued
- Calibration data in File AGEN.CAL out of tolerance
 CANCEL: Run Generator uncal, ENTER: Restore old AGEN.CAL from CMOS-RAM
 One or more calibration factors are out of tolerance. The permissible tolerances are specified for the individual calibration measurements (see page 7.123 pp.)
 The further branching CANCEL/ENTER is the same as above.

Similar error messages are output with faulty file LDG.CAL

7.3.3.3 Measuring Equipment

Measuring instrument	Specifications	R & S
AC Voltmeter	5Hz ... 100kHz Accuracy 0.1%	–

If no AC voltmeter with sufficient accuracy is available, the necessary measuring accuracy of 0.1% can also be obtained via a reference measurement using an AC calibrator.

Calibration of the Low Distortion Generator does not require any measuring equipment, since it can be calibrated in an automatic calibration routine with reference to the universal generator. As a prerequisite, the universal generator must be calibrated and adjusted.

7.3.3.4 Adjustment of 25-kHz Generator

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	OFF
	Voltage	1.000V

The following adjustment procedures are to be performed:

- LF and FDNR adjustment

CAUTION: After the adjustment, the level must be recalibrated

The two adjustments are coupled and must therefore always be performed together:

Adjustment	Potentiometer	Effect
LF	R336	2 ... 100Hz
FDNR	C351	20Hz ... 2kHz

Operate the DAC board on adapter card, since C351 will not be accessible otherwise.

Adjustment		
UPD	Procedure	Tolerance
80Hz	Measure AC	→ reference
5Hz	Adjust to reference with R336	±0.1%
40Hz	Measure AC	→ reference
2kHz	Adjust to reference with C351	±0.05%
		→ reference
5Hz	Adjust to reference with R336	±0.05%

Plug the DAC board into the Motherboard again!

- RF adjustment

NOTE: The calibration is independent of this adjustment

Adjustment		
UPD	Procedure	Tolerance
2kHz	Measure AC	→ reference
20kHz	Adjust to reference with R344	±0.05%

- Offset adjustment

NOTE: The calibration is independent of this adjustment

Set generator: Voltage 6.0000V

Switch off level (using service function):

- Call the service mode in the OPTIONS panel by entering the correct password in the line 'SERVICE password ?'
- Set DAC VoltAC 0

Adjustment		
UPD	Procedure	Tolerance
	Measure DC Adjust to 0 V with R337	$\pm 0.5\text{mV}$

Reset GENERATOR panel in order to switch the level on again

7.3.3.5 Adjustment of 110-kHz Generator

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15 Ω
	Function	SINE
	Low Dist	OFF
	Voltage	1.000V

The following adjustments are to be performed:

- LF adjustment

NOTE: The calibration is independent of this adjustment

Adjustment		
UPD	Procedure	Tolerance
150Hz	Measure AC	→ reference
5Hz	Adjust to reference with R436	$\pm 0.05\%$

- FDNR adjustment

CAUTION: Following the adjustment, the level must be recalibrated.

Operate the DAC board on the adapter card, since C454 will otherwise not be accessible.

Adjustment		
UPD	Procedure	Tolerance
150Hz	Measure AC	→ reference
10kHz	Adjust to reference with C454	$\pm 0.05\%$

Reinsert the DAC board into the motherboard!

- RF adjustment

NOTE: The calibration is independent of this adjustment

Adjustment		
UPD	Procedure	Tolerance
10kHz	Measure AC	→ reference
100kHz	Adjust to reference with R444	$\pm 0.05\%$

- Offset adjustment

NOTE: The calibration is independent of this adjustment

Set the generator: Voltage 6.0000V

Switch off level (using the service function):

- Call service mode in the OPTIONS panel by entering the correct password in the line 'SERVICE password ?'
- Set DAC VoltAC 0

Adjustment		
UPD	Procedure	Tolerance
	Measure DC Adjust to 0 V using R437	±0.5mV

Reset the GENERATOR panel to switch the level on again

7.3.3.6 Calibration of 25-kHz and 110-kHz Generator

- Calibration of 25-kHz generator: Sinusoidal level

CAUTION: LF and FDNR adjustment must be performed

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	OFF
	Frequency	1.000kHz
	Voltage	1.000V

Measure AC → Vo(actual)

Calculate calibration factor: $CF_{25} = 1.0000V / V_o(\text{actual})$

permissible tolerance: $CF_{25} = 1 \pm 0.03$

- Calibration of 25-kHz generator: sinusoidal level

NOTE: independent of all other adjustment and calibration procedures

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SQUARE
	Frequency	1.000kHz
	Voltage	1.000V (rms)

Measure AC → Vo(actual)

Calculate calibration factor: $CF_{sqr} = 1.0000V / V_o(\text{actual})$

Permissible tolerance: $CF_{sqr} = 1 \pm 0.075$

- Analyzer setting

Instrument	ANLG 100kHz
Channel(s)	1
Ch1 Input	GEN 1
Ch1 Range	FIX: 1.0 V RMS
FREQ/PHASE	FREQ
Meas Time	FAST
Unit	Hz
FUNCTION	RMS & S/N
S/N	OFF
Meas Time	AUTO
Unit	V
Anlg Notch	OFF
Filter	OFF
POST FFT	OFF

- Calibration of sinusoidal level

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	ON
	Frequency	1.000kHz
	Settling	FAST
	Voltage	1.000V

Low Dist OFF: Measure AC → Vo(nom.)

Low Dist ON: Measure AC → Vo(actual)

Calculate calibration factor: $CF_ldg_sin = Vo(nom.) / Vo(actual)$

Permissible tolerance: $CF_ldg_sin = 1 \pm 0.065$

- Calibration of IMD level setting (IMD ATTEN)

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	OFF
	Frequency	7.000kHz
	Voltage	1.000V

Measure AC → Vo(nom.)

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	MODDIST
	Low Dist	ON
	Upper Freq	7.000kHz
	Lower Freq	200Hz
	Total Volt	1.4142V (rms)
	Volt LF:UF	1:1

Deactivate Lower Freq (DAC SIG) (using service function):

- Call service mode in the OPTIONS panel by entering the correct password in the line 'SERVICE password ?'
- Set DAC VoltAC 0

Measure AC → Vo(actual)

Calculate calibration factor: $CF = 1.0000V / V_o(\text{actual}) = CF_ldg_imd$

permissible tolerance: $CF = 1 \pm 0.065$

Reset GENERATOR panel to switch the level on again.

- Calibration of frequency accuracy

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	ON
	Frequency	f(nom.) acc. to table
	Settling	FAST
	Voltage	1.000V

Set nominal frequency → f(nom.)

Measure frequency → f(actual)

Calculate calibration factor: $CF = f(\text{nom.}) / f(\text{actual})$

Permissible tolerance: $CF = 1 \pm 0.02$

Frequency f(nom.)	Calibration factor CF
50kHz	CF_ldg_rg0
10kHz	CF_ldg_rg1
1kHz	CF_ldg_rg2
100Hz	CF_ldg_rg3

- Adjustment of frequency response (relative)

CAUTION: 110-kHz universal generator must be calibrated and adjusted
 The sinusoidal level of the Low Distortion Generator must be calibrated

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	OFF
	Frequency	100.00kHz
	Voltage	1.000V

Adjustment		
Low Dist	Procedure	Tolerance
OFF	Measure AC	→ ref.
ON	Adjust to reference with C500	±0.05%

- Adjustment of frequency response (absolute)

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	ON
	Frequency	1.000kHz
	Voltage	1.000V

Adjustment		
UPD	Procedure	Tolerance
1kHz	Measure AC	→ ref.
100kHz	Adjust to reference with C500	±0.05%

- Error messages with automatic calibration

1. Calibration setup not found,
calibration data unchanged.

The file CALLDG.SET in the SETUP directory with the setting data of generator and analyzer for the automatic calibration measurements of the LDG is faulty or not available.

2. Tolerance file not found or data invalid;
calibration data unchanged.

The file LDG.TOL in the REF directory with the tolerances of the calibration factors is faulty or not available.

3. Calibration Measurement failed,
calibration data unchanged.

Calibration measurement(s) faulty:

- Hardware error in the LDG
- Repeat calibration
- Check LDG (see function, testing and troubleshooting)
- The analyzer may also be faulty
- Perform the calibration manually

4. Calibration data out of tolerance;
calibration data unchanged.

See file LDG_ER.CAL in directory REF

One or more calibration factors are out of tolerance.

- Examine file LDG_ERR.CAL
- The faulty calibration factors permit to locate the error:
CF_frq ⇒ Check frequency setting
CF_imd ⇒ Check IMD level setting
CF_ldg ⇒ Check oscillator level

7.3.4 Performance Verification Universal Generator

7.3.4.1 Measuring Equipment and Auxiliary Means

Measuring instrument	Specifications	R & S
RMS voltmeter	2Hz ... 110kHz 0.1mV ... 30V $\pm 0.1\%$ 2Hz ... 20kHz $\pm 0.2\%$ 20kHz ... 110kHz Input impedance $> 1M\Omega$	—
Selective voltmeter	20Hz ... 20kHz 1 μ V sensitivity	UPD
Digital multimeter	Resistance measurement, $\pm 0.1\%$	UDS5
Frequency counter	2Hz ... 110kHz, ± 10 ppm	—
Oscilloscope	100MHz	—
Analyzer for THD+N	Inherent distortion < -105dB 25Hz ... 20kHz < -90dB 20kHz ... 25kHz < -85dB 25kHz ... 100kHz	UPD
Analyzer for intermodulation (DIN 45403, SMPTE)	Inherent distortion < -96dB Upper Freq 4kHz ... 20kHz < -80dB Upper Freq 20kHz ... 100kHz Lower Freq 30Hz ... 500Hz	UPD
Analyzer for differential tone d3 (DIN 45403)	Inherent distortion < -96dB Mean Freq 5kHz ... 20kHz < -75dB Mean Freq 20kHz ... 50kHz < -70dB Mean Freq 50kHz ... 100kHz Diff Freq 80Hz ... 1kHz	UPD
Differential-tone lowpass (LP DFD)	passive RC lowpass for DFD d2 measurement Attenuation 1dB at f = 300Hz Attenuation 2dB at f = 600Hz Attenuation 3dB at f = 750Hz Attenuation 4dB at f = 1kHz Attenuation > 30 dB for f > 5 kHz	—

Circuit diagram differential-tone lowpass: LP DFD

See Testing the Rated Specifications of the Low Distortion Generator, page 7.153.

7.3.4.2 Test procedure

1. SINE signal

Generator setting	Instrument	ANLG 25kHz and 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	OFF
	Frequency	see measurement
	Voltage	see measurement

- Level accuracy

The different analog generators - ANLG 25 kHz or 110 kHz, each with/without Low Distortion Generator - are all level-adjusted on the same module (Output Circuit). It is therefore sufficient to measure the level accuracy over the entire dynamic range for only one generator. The level accuracy of the other generators is only tested with one level then.

It is sufficient to check the two channels of the unbalanced output, since the same modules are used for the balanced output. The output COMTST is level-adjusted like UNBAL; it uses the balanced output channel and, therefore, need not be checked separately.

To avoid errors in measurement due to the noise of the measuring instrument, small levels must be measured with band limiting by means of lowpass filters or selectively (narrowband bandpass).

Instrument: RMS Voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
Readout in dBV
UPD setting and measurement according to the test report

Tolerance: Level accuracy $\pm 1.0\%$ ($= \pm 0.09\text{dB}$) over the entire level range
Frequency: 1kHz

- Frequency response

With the setting Output UNBAL, Channel(s) 2 = -1, the first output stage drives channel 1, the second channel 2. The two output stages are connected in series. If the frequency response of channel 2 lies within the tolerance, the same must apply to channel 1. Testing of channel 1 can then be performed for less test points or omitted completely. It is sufficient to measure the two channels of the unbalanced output since the same modules are used for the balanced output.

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to the output of UPD generator
Relative readout $\Delta\%$, the voltage measured at 1 kHz is the reference voltage

UPD setting and measurement according to test report

Generator	Measurement at:
ANLG 25kHz:	2.00V
ANLG 110kHz:	Impedance = 15 Ω : Voltage = 10/4/2/1/0.01 V Impedance = 5 Ω : Voltage = 0.5 / 0.25 Volt

Frequency	Frequency response
2Hz ... 20Hz	$\pm 1.0\%$
20Hz ... 20kHz	$\pm 0.5\%$
20kHz ... 110kHz	$\pm 1.0\%$

- Frequency accuracy

Since all the signals are calculated in the DSP, the frequency accuracy is the same for all signals and independent of frequency and level: Measurement only with sine: 1.00V, 1kHz

Instrument: Frequency counter

Measurement: Connect frequency counter to output of UPD generator
UPD setting and measurement according to test report

Tolerance: ± 50 ppm

- Inherent distortion THD+N

It is sufficient to measure the distortion on both channels of the unbalanced output, since the same modules are used for the balanced output.

If the balanced output is to be checked nevertheless, the balanced input of the UPD analyzer is to be used for this purpose.

With the setting Output UNBAL, Channel(s) 2 = -1, the first output stage drives channel 1, the second channel 2. The two output stages are connected in series. If the distortion on channel 2 is within the tolerance, the same must also apply to channel 1. Testing of channel 1 can then be performed with less test points or omitted completely.

Generator setting	Instrument	ANLG 25kHz and 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15 Ω
	Function	SINE
	Low Dist	OFF
	Frequency	see measurement
	Voltage	see measurement

Instrument: Analyzer for THD+N: UPD

Measurement: Connect UPD analyzer to output of generator
UPD setting and measurement according to test report

Tolerance: Generator ANLG 25kHz

Frequency	THD+N
25Hz ... 7kHz	< -92dB
7kHz ... 25kHz	< -87dB

Generator ANLG 110kHz

Frequency	THD+N
25Hz ... 7kHz	< -94dB
7kHz ... 20kHz	< -83dB
20kHz ... 30kHz	< -80dB
30kHz ... 75kHz	< -74dB
75kHz ... 100kHz	< -70dB

NOTE The inherent distortion of the analyzer can be neglected with this measurement

With the THD+N measurement, the bandwidth of the distortion meter must be limited depending on the generator frequency:

Frequency	Bandwidth	Measurement using analyzer
< 7kHz	22kHz	ANLG 22kHz
< 25kHz	100kHz	ANLG 100kHz
< 100kHz	300kHz	ANLG 300kHz

2. Squarewave signal

Generator setting	Instrument	ANLG 25kHz
Channel(s)	2	-1
Output	UNBAL	
Impedance	15Ω	
Function	SQUARE	
Frequency	see measurement	
Voltage	see measurement	

- Level accuracy

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
Measurement on channel 2
UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 5.0\%$, for all frequencies

- Frequency accuracy

Instrument: Frequency counter

Measurement: Connect frequency counter to output of UPD generator
UPD setting and measurement according to test report

Tolerance: $\pm 50\text{ppm}$

- Waveform

Instrument: Oscilloscope

Measurement: Connect oscilloscope to output of UPD generator
Check the waveform: overshoot, rise time 10% – 90%

3. MODDIST signal

Generator setting	Instrument	ANLG 25kHz and 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15 Ω
	Function	MODDIST
	Low Dist	OFF
	Upper Freq	4kHz ... 100kHz
	Lower Freq	30Hz ... 500Hz
	Total Volt	see measurement
	Volt LF:UF	see measurement

- Level accuracy

Since level accuracy and frequency response have already been measured for the SINE signal, one measurement with one level is enough.

Total Volt 1.000V

Volt UF:LF 10:1 ... 1:1

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
Relative readout $\Delta\%$, reference 1.000V
UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 5.0\%$, for all frequencies

- Inherent distortion MODDIST

Instrument: Analyzer for MODDIST: UPD

Measurement: Connect UPD analyzer to output of generator
UPD setting and measurement according to test report

Tolerance: Generator ANLG 25kHz

Upper Freq	MODDIST
4kHz ... 20kHz	< -82dB
20kHz ... 25kHz	< -80dB

Lower Freq: 30Hz ... 500Hz, Volt LF:UF 4:1

Generator ANLG 110kHz

Upper Freq	MODDIST
4kHz ... 25kHz	< -80dB
25kHz ... 100kHz	< -78dB

Lower Freq: 30Hz ... 500Hz, Volt LF:UF 4:1

NOTE: The inherent distortion of the analyzer can be neglected with this measurement

4. DFD signal

Generator setting	Instrument	ANLG 25kHz and 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15Ω
	Function	DFD
	Low Dist	OFF
	Mean Freq	5kHz ... 110kHz
	Diff Freq	80Hz ... 1kHz
	Total Volt	see measurement

- Level accuracy

Since level accuracy and frequency response have already been measured for the SINE signal, one measurement with one level is enough.

Mean Freq 5kHz ... 110kHz

Diff Freq 80Hz ... 1kHz

Total Volt 1.000V

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
Relative readout $\Delta\%$, reference 1.000V
UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 5.0\%$, for all frequencies

- Inherent distortion DFD d2

Instrument: Selective voltmeter: UPD

Measurement: Connect UPD analyzer to output of generator
 Cut in LP DFD
 selective RMS measurement at $f = \text{Diff Freq}$: $\rightarrow V_{meas}$ (in dB)
 - Bandwidth 3%, Frequency Mode FIX: Diff Freq
 - Readout in dB
 - The voltage set on the generator is the reference voltage
 Calculate measured value DFD d2:
 $V_{meas} + \text{attenuation of LP DFD (at } f=\text{Diff Freq}) - 3\text{dB}$
 further UPD setting and measurement according to test report

Tolerance: Generator ANLG 25kHz

Mean Freq	DFD d2
5kHz ... 20kHz	< -117dB
20kHz ... 24kHz	< -115dB

Diff Freq: 80Hz ... 1kHz

Generator ANLG 110kHz

Mean Freq	DFD d2
5kHz ... 20kHz	< -117dB
20kHz ... 100kHz	< -90dB

Diff Freq: 80Hz ... 1kHz

NOTE: The correction factor of -3dB for the calculation of the DFD d2 value results from the fact that, according to the standard, the measured value for DFD d2 is to be referred to twice the rms value of one of the two sinewave signals, this value being by 3 dB larger than the measured rms value of the total signal.

- Inherent distortion DFD d3

Instrument: Analyzer for DFD d3: UPD

Measurement: Connect UPD analyzer to output of generator
 UPD setting and measurement according to test report

Tolerance: Generator ANLG 25kHz

Mean Freq	DFD d3
5kHz ... 20kHz	< -85dB
20kHz ... 24kHz	< -75dB

Diff Freq: 80Hz ... 1kHz

Generator ANLG 110kHz

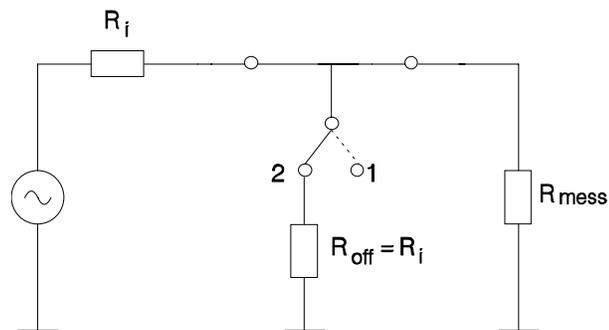
Mean Freq	DFD d3
5kHz ... 20kHz	< -85dB
20kHz ... 50kHz	< -75dB
50kHz ... 100kHz	< -70dB

Diff Freq: 80Hz ... 1kHz

CAUTION: For frequencies $<20\text{kHz}$, the inherent distortion of the analyzer can be neglected
 For frequencies $>20\text{kHz}$, the tolerance applies to loop measurement UPD generator with UPD analyzer and includes the inherent distortions of generator and analyzer

5. Impedance

The impedance R_{off} of the deactivated channel can be measured using an ohmmeter. The impedance R_i of the activated channel is calculated from the voltage division with a known resistance (e.g. resistance of deactivated channel). With a view to the measuring accuracy, the load must be approximately the same value as the impedance.



Generator setting	Instrument	ANLG 25kHz
	Channel(s)	see measurement
	Output	BAL and UNBAL
	Impedance	see measurement
	Function	SINE
	Low Dist	OFF
	Frequency	1kHz
	Voltage	see measurement

Instruments: Digital multimeter for resistance measurement
 RMS Voltmeter

Test setup: Connect digital multimeter to deactivated channel
 (Resistance measurement using four-wire technique)
 Connect RMS voltmeter to activated channel

Measurement: Measure resistance of deactivated channel using ohmmeter $\rightarrow R_{off}$
 RMS measurement on activated channel $\rightarrow V_1$
 Connect the two channels, RMS measurement $\rightarrow V_2$
 ($V_2 \approx 0.5 * V_1$)

Tolerance see test report

Calculate impedance according to the following formula:

$$R_i = \frac{1}{\frac{1}{R_{off}\left(\frac{V_1}{V_2} - 1\right)} - \frac{1}{R_{rms}}}$$

with R_{rms} = Impedance of RMS voltmeter
(can be neglected if $R_{rms} > 1000 * R_{off}$)

CAUTION: R_{off} must be measured directly on the output sockets of the UPD. To avoid errors in measurement due to line impedances, it is recommended to use the four-wire measurement technique. If possible, the connection of the two channels must be made with low impedance directly at the output sockets of the UPD.

6. Crosstalk

Crosstalk between the channels is independent of the generator selected (ANLG 25kHz or 110kHz, Low Dist ON or OFF) and of the impedance set.

Due to the high crosstalk of typ. 120dB, a very small voltage of a few μV only must be measured on the deactivated channel.

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	see measurement
	Output	BAL and UNBAL
	Impedance	15 Ω
	Function	SINE
	Low Dist	OFF
	Frequency	20kHz
	Voltage	see measurement

Instrument: Selective voltmeter (or spectrum analyzer or FFT analyzer)

Test setup: Connect selective voltmeter (e.g. UPD Analyzer) to the activated channel of the analog generator via a shielded cable

Measurement:

- UPD setting according to test report
- selective RMS measurement on deactivated channel
- Store measured value and switch to relative readout dB
- Switch generator to other channel
- selective RMS measurement on channel just deactivated
- the measured value is the crosstalk

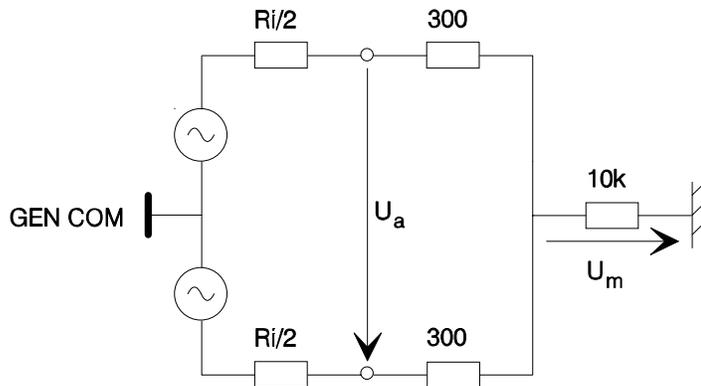
Tolerance: crosstalk < -117dB

7. Unbalance rejection

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	see measurement
	Output	BAL
	Impedance	see measurement
	Function	SINE
	Low Dist	OFF
	Frequency	see measurement
	Voltage	see measurement

Instrument: Selective voltmeter (or spectrum analyzer or FFT analyzer)

Test setup:



The two 300Ω resistors must be matched with an accuracy of $\pm 0.01\%$ to reach a limit of -100 dB. The absolute value is not important and should lie within the range $295\Omega \dots 305\Omega$.

Measurement: selective RMS measurement on activated channel $\rightarrow V_m$
 Relative readout dB
 The voltage V_o set on the generator is the reference
 The measured value is the unbalance

7.3.4.3 Test Report

measurement	min	act.	max	unit
SINUS				
SINUS Level Accuracy				
Generator	ANLG 25kHz			
Channel(s)	2 = -1			
Output	UNBAL			
Function	SINE			
Frequency	1kHz			
<i>measurement on ch. 1</i>				
Impedance	5Ω			
Voltage	21.58dBV	21.49	21.67	dBV
	20.00	19.91	20.09	
	15.00	14.91	15.09	
	12.00	11.91	12.09	
	8.00	7.91	8.09	
	7.00	6.91	7.09	
	6.00	5.91	6.09	
	5.00	4.91	5.09	
	4.00	3.91	4.09	
	3.00	2.91	3.09	
	2.00	1.91	2.09	
	1.00	0.91	1.09	
	0.00	-0.09	0.09	
	-1.00	-1.09	-0.91	
	-2.00	-2.09	-1.91	
	-3.00	-3.09	-2.91	
	-4.00	-4.09	-3.91	
	-5.00	-5.09	-4.91	
	-6.00	-6.09	-5.91	
	-7.00	-7.09	-6.91	
	-8.00	-8.09	-7.91	
	-10.00	-10.09	-9.91	
	-26.00	-26.09	-25.91	
	-40.00	-40.09	-39.91	
	-50.00	-50.09	-49.91	
	-60.00	-60.09	-59.91	
<i>measurement on ch. 2</i>				
Impedance	5Ω			
Voltage	21.58dBV	21.49	21.67	dBV
	10.00	9.91	10.09	

- continued -

measurement	min	act.	max	unit
0.00	-0.09		0.09	
-10.00	-10.09		-9.91	
-26.00	-26.09		-25.91	
-40.00	-40.09		-39.91	
-50.00	-50.09		-49.91	
-60.00	-60.09		-59.91	
<i>measurement on ch. 1</i>				
Impedance 15Ω				
Voltage 20.00dBV	19.91		20.09	dBV
2.00	1.91		2.09	
-6.00	-6.09		-5.91	
-12.00	-12.09		-11.91	
-26.00	-26.09		-25.91	
-40.00	-40.09		-39.91	
-48.00	-48.09		-47.91	
<i>measurement on ch. 2</i>				
Impedance 15Ω				
Voltage 20.00dBV	19.91		20.09	dBV
2.00	1.91		2.09	
-6.00	-6.09		-5.91	
-12.00	-12.09		-11.91	
-26.00	-26.09		-25.91	
-40.00	-40.09		-39.91	
-48.00	-48.09		-47.91	
Generator ANLG 110kHz				
Channel(s) 1				
Output UNBAL				
Impedance 15Ω				
Function SINE				
Frequency 1kHz				
Voltage 0.00dBV	-0.09		0.09	dBV
Generator ANLG 110kHz				
Channel(s) 2 = 1				
Output BAL				
Impedance 30Ω				
Function SINE				
Frequency 1kHz				
Voltage 0.00dBV				
<i>measurement on ch. 1</i>	-0.09		0.09	dBV
<i>measurement on ch. 2</i>	-0.09		0.09	dBV
SINUS Frequency Response				
Generator ANLG 25kHz				
Channel(s) 1				
Output UNBAL				
- continued -				

measurement		min	act.	max	unit
Impedance	15Ω				
Function	SINE				
Voltage	2.000V				
Frequency	2Hz	-1.0		1.0	%
	5	-1.0		1.0	
	10	-1.0		1.0	
	20	-0.5		0.5	
	200	-0.5		0.5	
	1kHz	0		0	
	5	-0.5		0.5	
	10	-0.5		0.5	
	15	-0.5		0.5	
	20	-0.5		0.5	
	25	-1.0		1.0	
Generator	ANLG 110kHz				
Channel(s)	2 = -1				
Output	UNBAL				
Impedance	15Ω				
Function	SINE				
<i>measurement on ch. 2</i>					
Voltage	2.000V				
Frequency	2Hz	-1.0		1.0	%
	5	-1.0		1.0	
	10	-1.0		1.0	
	20	-0.5		0.5	
	100	-0.5		0.5	
	1kHz	0		0	
	5	-0.5		0.5	
	10	-0.5		0.5	
	15	-0.5		0.5	
	20	-0.5		0.5	
	25	-1.0		1.0	
	50	-1.0		1.0	
	70	-1.0		1.0	
	90	-1.0		1.0	
	100	-1.0		1.0	
	110	-1.0		1.0	
<i>measurement on ch. 1</i>					
Voltage	2.000V				
Frequency	1kHz	0		0	%
	5	-0.5		0.5	
	10	-0.5		0.5	
	15	-0.5		0.5	
	20	-0.5		0.5	
	25	-1.0		1.0	
					- continued -

measurement	min	act.	max	unit
50	-1.0		1.0	
70	-1.0		1.0	
90	-1.0		1.0	
100	-1.0		1.0	
110	-1.0		1.0	
<i>measurement on ch. 2</i>				
Impedance 15Ω				
Voltage 10.000V				
Frequency 1kHz	0		0	%
10	-0.5		0.5	
20	-0.5		0.5	
50	-1.0		1.0	
75	-1.0		1.0	
100	-1.0		1.0	
<i>measurement on ch. 2</i>				
Impedance 15Ω				
Voltage 4.000V				
Frequency 1kHz	0		0	%
10	-0.5		0.5	
20	-0.5		0.5	
50	-1.0		1.0	
75	-1.0		1.0	
100	-1.0		1.0	
<i>measurement on ch. 1</i>				
Impedance 15Ω				
Voltage 1.000V				
Frequency 1kHz	0		0	%
10	-0.5		0.5	
20	-0.5		0.5	
50	-1.0		1.0	
75	-1.0		1.0	
100	-1.0		1.0	
<i>measurement on ch. 2</i>				
Impedance 15Ω				
Voltage 1.000V				
Frequency 1kHz	0		0	%
10	-0.5		0.5	
20	-0.5		0.5	
50	-1.0		1.0	
75	-1.0		1.0	
100	-1.0		1.0	
<i>measurement on ch. 1</i>				
Impedance 15Ω				
Voltage 10.0mV				
Frequency 1kHz	0		0	%

- continued -

measurement		min	act.	max	unit
	10	-0.5		0.5	
	20	-0.5		0.5	
	50	-1.0		1.0	
	75	-1.0		1.0	
	100	-1.0		1.0	
<i>measurement on ch. 2</i>					
Impedance	15Ω				
Voltage	10.0mV				
Frequency	1kHz	0		0	%
	10	-0.5		0.5	
	20	-0.5		0.5	
	50	-1.0		1.0	
	75	-1.0		1.0	
	100	-1.0		1.0	
<i>measurement on ch. 2</i>					
Impedance	5Ω				
Voltage	0.500V				
Frequency	1kHz	0		0	%
	10	-0.5		0.5	
	20	-0.5		0.5	
	50	-1.0		1.0	
	75	-1.0		1.0	
	100	-1.0		1.0	
<i>measurement on ch. 1</i>					
Impedance	5Ω				
Voltage	0.250V				
Frequency	1kHz	0		0	%
	10	-0.5		0.5	
	20	-0.5		0.5	
	50	-1.0		1.0	
	75	-1.0		1.0	
	100	-1.0		1.0	
<i>measurement on ch. 2</i>					
Impedance	5Ω				
Voltage	0.250V				
Frequency	1kHz	0		0	%
	10	-0.5		0.5	
	20	-0.5		0.5	
	50	-1.0		1.0	
	75	-1.0		1.0	
	100	-1.0		1.0	
SINUS Frequency Accuracy					
Generator	ANLG 25kHz				
Function	SINE				
Frequency	1000Hz	999.95		1000.05	Hz

- continued -

measurement		min	act.	max	unit
Generator	ANLG 110kHz				
Function	SINE				
Frequency	1000Hz	999.95		1000.05	Hz
SINUS Inherent Distortion THD+N					
Generator	ANLG 25kHz				
Channel(s)	2 = -1				
Output	UNBAL				
Impedance	15Ω				
Function	SINE				
Voltage	2.000V				
Frequency	25Hz			-92	dB
	100Hz			-92	dB
	1kHz			-92	dB
	7kHz			-92	dB
	10kHz			-87	dB
	20kHz			-87	dB
	25kHz			-87	dB
Generator	ANLG 110kHz				
Channel(s)	2 = -1				
Output	UNBAL				
Impedance	15Ω				
Function	SINE				
Voltage	2.000V				
Frequency	25Hz			-94	dB
	100Hz			-94	dB
	1kHz			-94	dB
	7kHz			-94	dB
	20kHz			-83	dB
	30kHz			-80	dB
	50kHz			-74	dB
	75kHz			-74	dB
	100kHz			-70	dB
Squarewave					
Squarewave Level Accuracy					
Frequency	1kHz				
Voltage	10V	9.5		10.5	V
	1V	0.95		1.05	
	0.1V	0.095		0.105	
Squarewave Frequency Response					
Voltage	1.000V				
Frequency	2Hz	0.95		1.05	V
	10	0.95		1.05	
- continued -					

measurement		min	act.	max	unit
100		0.95		1.05	
1kHz		0.95		1.05	
10		0.95		1.05	
Squarewave Frequency Accuracy					
Frequency	2Hz	1.9999		2.0001	Hz
	10Hz	9.9995		10.0005	
	100Hz	99.995		100.005	
	500Hz	499.975		500.025	
	1000Hz	999.95		1000.05	
	5.000kHz	4.99975		5.00025	kHz
	10.000kHz	9.9995		10.0005	
Squarewave Signal Shape					
Frequency	10.00kHz				
Voltage	10.00V				
<i>over swing</i>				0	%
<i>rise time</i>				2	μ s
MODDIST					
MODDIST Level Accuracy					
Generator	ANLG 25kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15 Ω				
Lower Freq	250Hz				
Volt LF:UF	4:1				
Total Volt	1.000V				
Upper Freq	4kHz	-5.0		+5.0	%
	10kHz	-5.0		+5.0	%
	20kHz	-5.0		+5.0	%
	25kHz	-5.0		+5.0	%
Generator	ANLG 110kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15 Ω				
Lower Freq	250Hz				
Volt LF:UF	4:1				
Total Volt	1.000V				
Upper Freq	4kHz	-5.0		+5.0	%
	20kHz	-5.0		+5.0	%
	50kHz	-5.0		+5.0	%
	100kHz	-5.0		+5.0	%
MODDIST Inherent Distortion					
Generator	ANLG 25kHz				

- continued -

measurement		min	act.	max	unit
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Lower Freq	250Hz				
Volt LF:UF	4:1				
Total Volt	3.000V				
Upper Freq	4kHz				
	:			-82	dB
	10kHz				
	:			-82	dB
	20kHz				
	:			-80	dB
	25kHz				
Generator	ANLG 110kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Lower Freq	250Hz				
Volt LF:UF	4:1				
Total Volt	3.000V				
Upper Freq	5kHz				
	:			-80	dB
	25kHz				
	:			-78	dB
	50kHz				
	:			-78	dB
	100kHz				
DFD					
DFD Level Accuracy					
Generator	ANLG 25kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Total Volt	1.000V				
Diff Freq	500Hz				
Mean Freq	5kHz	-5.0		+5.0	%
	10kHz	-5.0		+5.0	%
- continued -					

measurement		min	act.	max	unit
	20kHz	-5.0		+5.0	%
	25kHz	-5.0		+5.0	%
Generator	ANLG 110kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Total Volt	1.000V				
Diff Freq	500Hz				
Mean Freq	5kHz	-5.0		+5.0	%
	20kHz	-5.0		+5.0	%
	50kHz	-5.0		+5.0	%
	100kHz	-5.0		+5.0	%
DFD Inherent Distortion d2					
Generator	ANLG 25kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Total Volt	5.000V				
Diff Freq	500Hz				
Mean Freq	5kHz				
	⋮			-117	dB
	20kHz				
	⋮			-115	dB
	25kHz				
Generator	ANLG 110kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Total Volt	5.000V				
Diff Freq	500Hz				
Mean Freq	5kHz				
	⋮			-117	dB
	20kHz				
	⋮			-90	dB
	50kHz				
	⋮			-90	dB
	100kHz				
DFD Inherent Distortion d3					
Generator	ANLG 25kHz				

- continued -

measurement		min	act.	max	unit
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Total Volt	3.000V				
Diff Freq	500Hz				
Mean Freq	5kHz				
	⋮			-85	dB
	20kHz				
	⋮			-75	dB
	25kHz				
Generator	ANLG 110kHz				
Channel(s)	1				
Output	UNBAL				
Impedance	15Ω				
Total Volt	3.000V				
Diff Freq	500Hz				
Mean Freq	5kHz				
	⋮			-85	dB
	20kHz				
	⋮			-75	dB
	50kHz				
	⋮			-70	dB
	100kHz				
Output Impedance					
Output	UNBAL				
Channel(s)	OFF				
Impedance	15Ω				
measurement on ch.	R_{off}	14.7		15.3	Ω
1					
measurement on ch.	R_{off}	14.7		15.3	Ω
2					
Impedance	5Ω				
measurement on ch.	R_{off}	4.5		5.0	Ω
1					
measurement on ch.	R_{off}	4.5		5.0	Ω
2					
Output	UNBAL				
Channel(s)	2 = -1				
- continued -					

measurement		min	act.	max	unit
Impedance	15Ω				
<i>measurement on ch.</i>	R_i				
1					
Voltage	2V	14.7		15.3	Ω
	1V	14.7		15.3	Ω
	.25V	14.7		15.3	Ω
	25mV	14.7		15.3	Ω
	10mV	14.7		15.3	Ω
<i>measurement on ch.</i>	R_i				
2					
Voltage	2V	14.7		15.3	Ω
	1V	14.7		15.3	Ω
	.25V	14.7		15.3	Ω
	25mV	14.7		15.3	Ω
	10mV	14.7		15.3	Ω
Output	UNBAL				
Channel(s)	2 = -1				
Impedance	5Ω				
<i>measurement on ch.</i>	R_i				
1					
Voltage	0.5V	4.5		5.0	Ω
	0.2V	4.5		5.0	Ω
<i>measurement on ch.</i>	R_i				
2					
Voltage	0.5V	4.5		5.0	Ω
	0.2V	4.5		5.0	Ω
Output	BAL				
Channel(s)	OFF				
<i>measurement on ch.</i>	R_{off}				
1					
Impedance	10Ω	9.0		10.0	Ω
	30Ω	29.5		30.5	Ω
	200Ω	199		201	Ω
	600Ω	597		603	Ω
<i>measurement on ch.</i>	R_{off}				
2					
Impedance	10Ω	9.0		10.0	Ω
	30Ω	29.5		30.5	Ω
	200Ω	199		201	Ω
	600Ω	597		603	Ω
crosstalk					
Output	UNBAL				
Frequency	20kHz				
- continued -					

measurement		min	act.	max	unit
Voltage	10V				
<i>crosstalk</i>	channel 1 → 2			-117	dB
<i>crosstalk</i>	channel 2 → 1			-117	dB
Voltage	1V				
<i>crosstalk</i>	channel 1 → 2			-117	dB
<i>crosstalk</i>	channel 2 → 1			-117	dB
Output	BAL				
Frequency	20kHz				
Voltage	10V				
<i>crosstalk</i>	channel 1 → 2			-117	dB
<i>crosstalk</i>	channel 2 → 1			-117	dB
Voltage	1V				
<i>crosstalk</i>	channel 1 → 2			-117	dB
<i>crosstalk</i>	channel 2 → 1			-117	dB

Unbalanced Rejection

Channel(s)	1				
Voltage	10V				
Frequency	1kHz				
Impedance	10Ω			-80	dB
	30Ω			-80	dB
	200Ω			-80	dB
	600Ω			-80	dB
Frequency	20kHz				
Impedance	10Ω			-60	dB
	30Ω			-60	dB
	200Ω			-60	dB
	600Ω			-60	dB
Channel(s)	1				
Voltage	2V				
Frequency	1kHz				
Impedance	10Ω			-80	dB
	30Ω			-80	dB
	200Ω			-80	dB
	600Ω			-80	dB
Frequency	20kHz				
Impedance	10Ω			-60	dB
	30Ω			-60	dB
	200Ω			-60	dB
	600Ω			-60	dB
Channel(s)	1				
Voltage	10V				
Frequency	1kHz				

- continued -

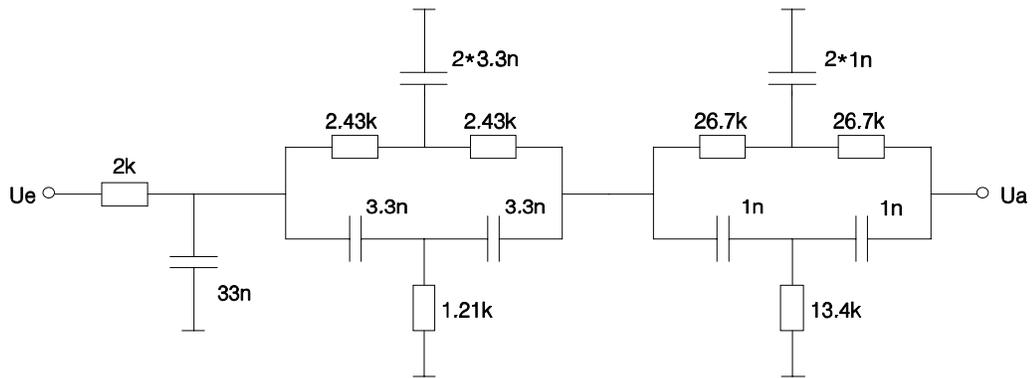
measurement		min	act.	max	unit
Impedance	10Ω			-80	dB
	30Ω			-80	dB
	200Ω			-80	dB
	600Ω			-80	dB
Frequency	20kHz				
Impedance	10Ω			-60	dB
	30Ω			-60	dB
	200Ω			-60	dB
	600Ω			-60	dB
Channel(s)	2				
Voltage	2V				
Frequency	1kHz				
Impedance	10Ω			-80	dB
	30Ω			-80	dB
	200Ω			-80	dB
	600Ω			-80	dB
Frequency	20kHz				
Impedance	10Ω			-60	dB
	30Ω			-60	dB
	200Ω			-60	dB
	600Ω			-60	dB

7.3.5 Performance Verification Low Distortion Generator

7.3.5.1 Measuring Equipment and Auxiliary Means

Measuring instrument	Specifications	R & S
RMS Voltmeter	10Hz ... 110kHz 0.1mV ... 30V ±0.1% 10Hz ... 20kHz ±0.2% 20kHz ... 110kHz Input impedance >1MΩ	—
Selective voltmeter	80Hz ... 1kHz 1μV sensitivity	UPD
Frequency counter	10Hz ... 110kHz, ±10ppm	—
Analyzer for THD	Inherent distortion < -96dB 10Hz ... 20Hz < -100dB 20Hz ... 100Hz < -110dB 100Hz ... 7kHz < -92dB 7kHz ... 50kHz < -86dB 50kHz ... 100kHz	UPD
Analyzer for THD+N THD+N	Inherent distortion < -105dB 25Hz ... 20kHz < -90dB 20kHz ... 25kHz < -85dB 25kHz ... 100kHz	UPD
Analyzer for intermodulation (DIN 45403, SMPTE)	Inherent distortion < -96dB Upper Freq 4kHz ... 20kHz < -80dB Upper Freq 20kHz ... 100kHz Lower Freq 30Hz ... 500Hz	UPD
Analyzer for differential tone d3 (DIN 45403)	Inherent distortion < -96dB Mean Freq 5kHz ... 20kHz < -75dB Mean Freq 20kHz ... 50kHz < -70dB Mean Freq 50kHz ... 100kHz Diff Freq 80Hz ... 1kHz Diff Freq 80Hz ... 1kHz	UPD
Analyzer for DIM (IEC 268-3)	Inherent distortion < -85dB	UPD
Differential-tone lowpass (LP DFD)	passive RC lowpass for DFD d2 measurement Attenuation 1dB at f = 300Hz Attenuation 2dB at f = 600Hz Attenuation 3dB at f = 750Hz Attenuation 4dB at f = 1kHz Attenuation >35dB for f > 5kHz	—
Intermodulation highpass (HP MODDIST)	passive RC highpass for MODDIST measurement Attenuation >40dB for f < 500Hz Attenuation <5dB for f > 4kHz	—

Circuit diagram of differential-tone lowpass LP DFD

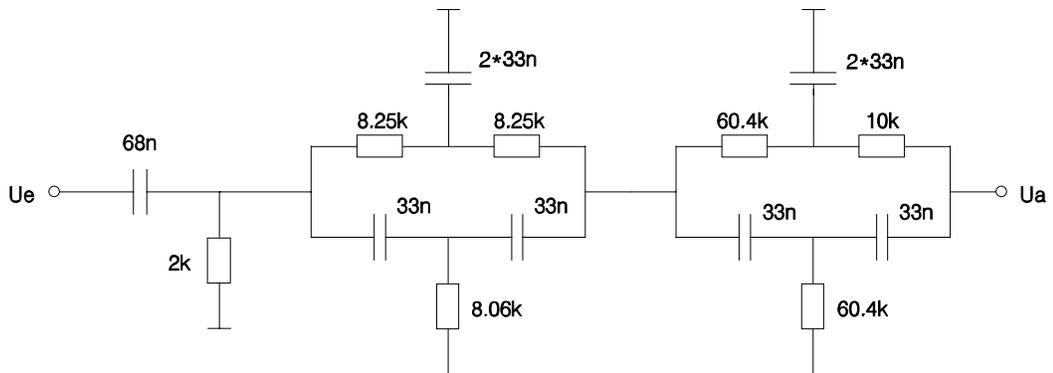


Components:

Resistors: Metal film resistors, 1% tolerance

Capacitors: Polypropylene, 1% tolerance

Circuit diagram of intermodulation highpass HP MODDIST



Components:

Resistors: Metal film resistors, 1% tolerance

Capacitors: Polypropylene, 1% tolerance

7.3.5.2 Test sequence

1. SINE Signal

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	ON
	Frequency	see measurement
	Settling	FAST
	Voltage	1.000V

- Level accuracy

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 1.0\%$

- Frequency response

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
Relative readout $\Delta\%$, the voltage measured at 1 kHz is the reference voltage
UPD setting and measurement according to test report

Tolerance:

Frequency	Frequency response
10Hz ... 20Hz	$\pm 1.0\%$
20Hz ... 20kHz	$\pm 0.5\%$
20kHz ... 110kHz	$\pm 1.0\%$

- Frequency accuracy

Instrument: Frequency counter

Measurement: Connect frequency counter to output of UPD generator
UPD setting and measurement according to test report

Tolerance: $\pm 0.5\%$, Settling FAST
 $\pm 0.1\%$, Settling PRECISION

• Inherent distortion THD and THD+N

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15Ω
	Function	SINE
	Low Dist	ON
	Frequency	see measurement
	Settling	FAST
	Voltage	see measurement

Instrument: Analyzer for THD and THD+N: UPD

Measurement: Connect UPD analyzer to output of generator
 Measurement on channel 1 and 2
 Measurement at several voltages, e.g.:
 Voltage = 10 / 4 / 2 / 1 Volt; Impedance = 15Ω

Tolerance:

Frequency	THD+N	THD	THD (with UPD-ANA)
10Hz	—	< -107dB	< -96dB
25Hz ...100Hz	< -105dB	< -113dB	< -100dB
100Hz ...7kHz	< -105dB	< -113dB	< -110dB
7kHz ...20kHz	< -90dB	< -107dB	< -100dB
20kHz ...50kHz	< -85dB	< -92dB	< -92dB
50kHz ...100kHz	< -85dB	< -86dB	< -86dB

CAUTION: The THD+N tolerance applies to the loop measurement UPD generator with UPD analyzer and includes inherent distortions of generator and analyzer

In the case of the THD+N measurement, the bandwidth of the distortion meter must be limited depending on the generator frequency:

Frequency	Bandwidth	measurement with analyzer
< 7kHz	22kHz	ANLG 22kHz
< 25kHz	100kHz	ANLG 100kHz
< 100kHz	300kHz	ANLG 300kHz

• Measurement procedures for THD of Low Distortion Generator

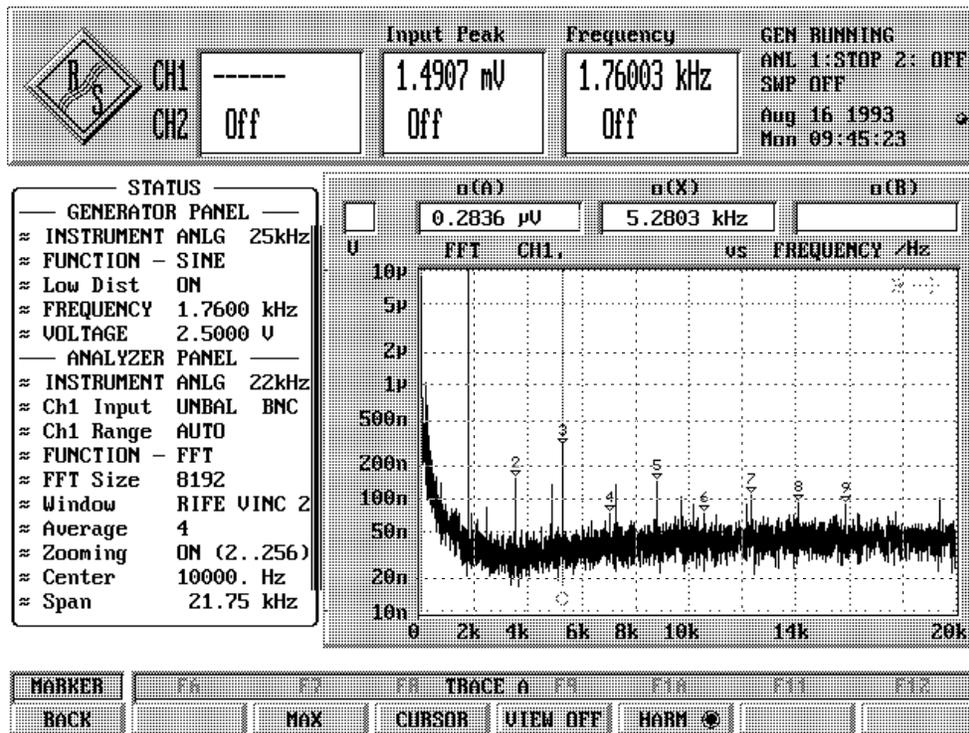
The inherent distortion of the generator is better than that of the analyzer and, therefore, cannot be directly tested using the UPD.

For measurement of the harmonics suppression, a passive notch filter is used, suppressing the fundamental by more than 60 dB and attenuating the harmonics by less than 10 dB. As a result of this, the dynamic range is increased by 50 dB from 100 dB to 150 dB (referred to the non-suppressed fundamental).

Procedure:

- Generator setting

Instrument	ANLG 25kHz
Channel(s)	1
Output	UNBAL
Impedance	15Ω
Function	SINE
Low Dist	ON
Frequency	f_1
Settling	FAST
Voltage	2.500V ($=U_1$)
- Analyzer setting according to the display



- Switch generator signal via notch filter to analyzer input
In order to obtain a suppression of the fundamental by more than 60 dB, it may be necessary to readjust the generator frequency f_1 slightly.
- Measure the voltage of every harmonic $n * f_1$ ($n = 2 \dots 5$) separately using the cursor ($\rightarrow V_{meas}$) and correct with the attenuation a_n of the notch filter (the attenuations a_n are specified with the notch filter circuit, see next page).
 \Rightarrow Voltage of nth harmonic:

$$V_n = V_{meas} * a_n$$

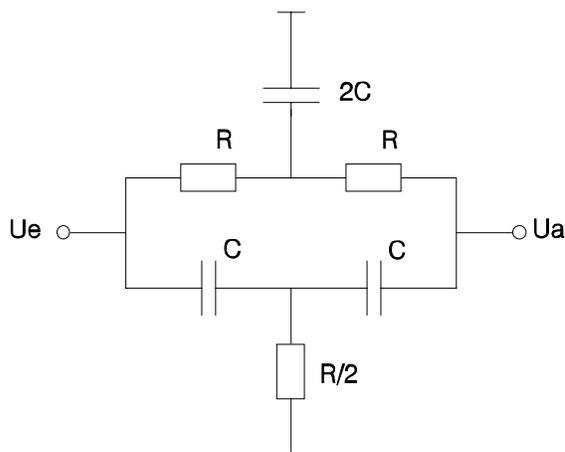
- Calculation of the THD value:
Squarelaw addition of the individual harmonics:

$$V_{THD} = \sqrt{\sum_{n=2}^5 V_n^2}$$

Reference to the fundamental:

$$THD \text{ (in dB)} = 20 * \log \frac{V_{THD}}{V_1}$$

Circuit diagram of notch filter for THD measurement



Components:

Resistors: Metal film resistors, 0.1% tolerance

Capacitors: Polypropylene, 1% tolerance

Notch frequency:

$$f_1 = \frac{1}{2\pi RC}$$

The attenuation of the notch filter for the harmonics must be taken into account with the THD measurement:

Frequency	Attenuation/dB	a_n
f_1	>60	—
$2 * f_1$	9.1	2.85
$3 * f_1$	5.1	1.80
$4 * f_1$	3.3	1.50
$5 * f_1$	2.3	1.30

2. MODDIST signal

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15Ω
	Function	MODDIST
	Low Dist	ON
	Upper Freq	4kHz ... 100kHz
	Lower Freq	30Hz ... 500Hz
	Total Volt	see measurement
	Volt LF:UF	see measurement

- Level accuracy

Total Volt 1.000V
 Volt UF:LF 10:1 ... 1:1

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
 Relative readout $\Delta\%$, reference 1.000V
 UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 5.0\%$, for all frequencies

- Inherent distortion MODDIST

Instrument: Analyzer for MODDIST: UPD
 external RC lowpass: HP MODDIST

Measurement: Connect UPD analyzer to output of generator
 Cut in HP MODDIST: the highpass eliminates the effect of the inherent distortions of the analyzer (attenuation in the passband does not affect the measurement)
 Measurement on channel 1 and 2
 Measurement with several voltages, e.g.:
 Total Volt = 10 / 5 / 3 / 1 V; impedance = 15Ω

<u>Tolerance:</u>	Upper Freq	MODDIST
	4kHz ... 20kHz	< -96dB
	20kHz ... 100kHz	< -80dB

Lower Freq: 200Hz ... 500Hz, Volt LF:UF 4:1

For Lower Freq 30Hz ... 200Hz, the inherent distortion is somewhat worse, since the measurement is made in the vicinity of the lower-frequency signal (see data sheet)

3. DFD signal

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15Ω
	Function	DFD
	Low Dist	ON
	Mean Freq	5kHz ... 110kHz
	Diff Freq	80Hz ... 1kHz
	Settling	PRECISION
	Total Volt	see measurement

• Level accuracy

Mean Freq 5kHz ... 110kHz
 Diff Freq 80Hz ... 1kHz
 Total Volt 1.000V

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
 Relative readout $\Delta\%$, reference 1.000V
 UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 5.0\%$, for all frequencies

• Inherent distortion DFD d2

Instrument: Selective voltmeter: UPD

Measurement: Connect UPD analyzer to output of generator
 Cut in LP DFD
 selective RMS measurement at $f = \text{Diff Freq}$: $\rightarrow V_{meas}$ (in dB)
 - Bandwidth 3%, Frequency Mode FIX: Diff Freq
 - Readout in dB
 - The voltage set on the generator is the reference
 Calculate measured value DFD d2:
 $V_{meas} + \text{attenuation of LP DFD (at } f = \text{Diff Freq)} - 3\text{dB}$
 further UPD setting and measurement according to test report
 Measurement on channel 1 and 2
 Measurement with several voltages, e.g.:
 Total Volt = 10 / 5 / 3 / 1 V; Impedance = 15Ω

Tolerance:

Mean Freq	DFD d2
5kHz ... 20kHz	< -120dB
20kHz ... 50kHz	< -100dB
50kHz ... 100kHz	< -90dB

Diff Freq: 80Hz ... 1kHz

• Inherent distortion DFD d3

Instrument: Analyzer for DFD d3: UPD

Measurement: on channel 2 (and 1)
Measurement with several voltages, e.g.:
Total Volt = 10 / 5 / 3 / 1 V; Impedance = 15 Ω

<u>Tolerance:</u>	Mean Freq	DFD d3
	5kHz ... 20kHz	< -96dB
	20kHz ... 50kHz	< -75dB
	50kHz ... 100kHz	< -70dB
	Diff Freq: 80Hz ... 1kHz	

CAUTION: The tolerance applies to loop measurement UPD generator with UPD analyzer and includes the inherent distortions of generator and analyzer

4. DIM signal

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	2 = -1
	Output	UNBAL
	Impedance	15 Ω
	Function	DIM
	Square/Sin	2.96/14kHz and 3.15/15kHz
	Bandwidth	30kHz and 100kHz
	Settling	FAST
	Total Volt	2.0000 Vpp

- Level accuracy

Instrument: RMS voltmeter

Measurement: Connect RMS voltmeter to output of UPD generator
Relative readout $\Delta\%$, reference 1.000V
UPD setting and measurement according to test report

Tolerance: Level accuracy $\pm 5.0\%$, for all frequencies

- Inherent distortion DIM

Instrument: analyzer for DIM: UPD

Measurement: Measurement on channel 1 and 2
with impedance 5 Ω and 15 Ω
with different voltages

Tolerance: DIM < -85dB

CAUTION: The tolerance applies to loop measurement UPD generator with UPD analyzer and includes the inherent distortions of generator and analyzer

7.3.5.3 Test Report

measurement	min	act.	max	unit
SINUS				
SINUS Level Accuracy				
Frequency 1kHz				
Voltage 1.0000V	.9900		1.0100	V
SINUS Frequency Response				
Voltage 1V				
Frequency 10Hz	-1.0		1.0	%
20	-0.5		0.5	
200	-0.5		0.5	
1kHz	0		0	
5	-0.5		0.5	
10	-0.5		0.5	
15	-0.5		0.5	
20	-0.5		0.5	
25	-1.0		1.0	
50	-1.0		1.0	
70	-1.0		1.0	
90	-1.0		1.0	
100	-1.0		1.0	
SINUS Frequency Accuracy				
Settling FAST				
Frequency 10Hz	9.95		10.05	Hz
100Hz	99.5		100.5	
200Hz	199		201	
1.000kHz	0.95		1.05	kHz
1.500kHz	1.4925		1.5075	kHz
2.000kHz	1.99		2.01	
10.000kHz	9.95		10.05	
20.000kHz	19.9		20.1	
50.000kHz	49.75		50.25	
110.000kHz	109.45		110.55	
Settling PRECISION				
Frequency 10Hz	9.99		10.01	Hz
100Hz	99.9		100.1	
200Hz	199.8		200.2	
1.000kHz	0.999		1.001	kHz
1.500kHz	1.4985		1.5015	kHz
2.000kHz	1.998		2.002	
10.000kHz	9.99		10.01	
- continued -				

measurement	min	act.	max	unit
20.000kHz	19.98		20.02	
50.000kHz	49.95		50.05	
110.000kHz	109.89		110.11	
SINUS Inherent Distortion THD				
Channel(s)	2 = -1			
Output	UNBAL			
Impedance	15Ω			
Function	SINE			
Voltage	3.000V			
Measurement with UPD-Analyzer				
Frequency	10Hz		-96	dB
	20Hz		-100	dB
	100Hz		-100	dB
	1kHz		-110	dB
	7kHz		-110	dB
	20kHz		-100	dB
	50kHz		-92	dB
	100kHz		-86	dB
SINUS Inherent Distortion THD+N				
Channel(s)	2 = -1			
Output	UNBAL			
Impedance	15Ω			
Function	SINE			
Voltage	3.000V			
Frequency	25Hz		-105	dB
	100Hz		-105	dB
	1kHz		-105	dB
	7kHz		-105	dB
	20kHz		-90	dB
	50kHz		-85	dB
	100kHz		-85	dB
MODDIST				
MODDIST Level Accuracy				
Upper Freq	7kHz			
Volt LF:UF	10:1			
Total Volt	1.000V			
Lower Freq	30Hz	-5.0	+5.0	%
	100Hz	-5.0	+5.0	%
	200Hz	-5.0	+5.0	%
	500Hz	-5.0	+5.0	%
Lower Freq	250Hz			
Volt LF:UF	4:1			
- continued -				

measurement		min	act.	max	unit
Total Volt	1.000V				
Upper Freq	4kHz	-5.0		+5.0	%
	10kHz	-5.0		+5.0	%
	20kHz	-5.0		+5.0	%
	50kHz	-5.0		+5.0	%
	100kHz	-5.0		+5.0	%
Lower Freq	250Hz				
Volt LF:UF	1:1				
Total Volt	1.000V				
Upper Freq	4kHz	-5.0		+5.0	%
	10kHz	-5.0		+5.0	%
	20kHz	-5.0		+5.0	%
	50kHz	-5.0		+5.0	%
	100kHz	-5.0		+5.0	%
MODDIST Inherent Distortion					
Volt LF:UF	4:1				
Total Volt	5.000V				
Lower Freq	300Hz				
Upper Freq	5kHz				
	⋮			-96	dB
	20kHz			-80	dB
	⋮			-80	dB
	50kHz			-80	dB
	⋮				
	100kHz				
DFD					
DFD Level Accuracy					
Total Volt	1.000V				
Diff Freq	500Hz				
Mean Freq	5kHz	-5.0		+5.0	%
	10kHz	-5.0		+5.0	%
	20kHz	-5.0		+5.0	%
	50kHz	-5.0		+5.0	%
	100kHz	-5.0		+5.0	%
DFD Inherent Distortion d2					
Total Volt	5.000V				
Diff Freq	500Hz				
Mean Freq	5kHz				
	⋮			-120	dB

- continued -

measurement		min	act.	max	unit
20kHz				-100	dB
⋮					
50kHz				-90	dB
⋮					
100kHz					
DFD Inherent Distortion d3					
Total Volt	5.000V				
Diff Freq	500Hz				
Mean Freq	5kHz				
⋮				-96	dB
20kHz					
⋮				-75	dB
50kHz					
⋮				-70	dB
100kHz					
DIM					
DIM Level Accuracy					
Total Volt	2Vpp				
Square/Sin	2.96/14kHz				
Bandwidth	30kHz	-5.0		+5.0	%
	100kHz	-5.0		+5.0	%
Total Volt	2Vpp				
Square/Sin	3.15/15kHz				
Bandwidth	30kHz	-5.0		+5.0	%
	100kHz	-5.0		+5.0	%
DIM Inherent Distortion					
Total Volt	2Vpp				
Square/Sin	2.96/14kHz				
Bandwidth	30kHz			-85	dB
	100kHz			-85	dB
Total Volt	2Vpp				
Square/Sin	3.15/15kHz				
Bandwidth	30kHz			-85	dB
	100kHz			-85	dB

7.3.6 Service Mode

For test purposes, it may be necessary to configure the hardware other than possible with the normal entries in the GENERATOR panel. For this purpose, however, no special functions for particular hardware settings have been implemented. However, bit groups of minimally 1 to maximally 16 bits can be varied in the serial data stream of the generator. A single bit, e.g., permits to switch a certain relay, the entire attenuator can be switched by 8 bits; 12 bits permit to set an offset DAC, 16 bits the frequency of the Low Dist Gen.

The module descriptions include tables for controlling the analog functions with information on position, number, value range and function of the bits.

All the possible settings of the service mode are also available in IEC-bus mode: see DIAGNOSTIC commands in the operating manual

- Calling the service mode

- Change to OPTIONS panel

- Enter password in the line 'SERVICE password ?':

After entering the correct password,

OPTIONS panel	SERVICE	password ok
	Diag State	OFF

- Activate service mode

Diag State ON

ON Activate service mode for all analog modules

UPD setup is stored

normal operation via the panels remains activated

NOTE: A new setting in the generator panel overwrites the entries made in service mode. The OPTIONS panel is changed and the actual setting of the hardware is displayed.

OFF Switch off service mode

The UPD is reset to the status valid before calling of the service mode

- After entering 'Diag State ON', further options appear in the OPTIONS panel:

OPTIONS panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	DAC
	Position	6
	Count(Bit)	0
	Bitvalue	1
	Execute	NO

- Setting the signal D/A converter

DAC VoltAC x Signal amplitude ($x * FS$) with $0 \leq x \leq 1$

DAC VoltDC y DC offset ($y * FS$) with $-1 \leq y \leq 1$

These two settings are performed at once

CAUTION: The D/A converter is overdriven (digitally), if $|y| + x > FS$

- Setting the analog hardware
 - Selecting the board

AGEN Board	DAC	→ Dac Board
	OUT	→ Output Circuit
	LOW DIST	→ Low Distortion Generator
	NONAME GEN	→ Spare slot X23 (currently not used)
 - Setting the bits

Position	Position of the first bit to be changed
Count(Bit)	Number of bits to be changed (maximally 16)
Bitvalue	new bits (decimal 0 to 65535)
 - Executing the setting

Execute	NO	nothing has happened
	YES	Send bit stream ⇒ Hardware is set
- Enable Bit

ON	Bit=1	normal operating status
OFF	Bit=0	Signal DAC is switched off (AND gate D200 on the motherboard disables the signals from the digital generator) The outputs of the generator are switched off with high-impedance.

This single bit also belongs to the data stream for the generator and is implemented by means of flip-flop D310 on the analog motherboard. The ENABLE line is routed from there to all modules of the analog generator. (see circuit diagram Analog Motherboard and description of the modules)

- Initializing the modules

One or more modules have been registered with `Error` in board ID and are therefore not addressed by the software.

For troubleshooting on the generator modules, however, the correct data stream must be sent for all installed boards. Therefore, all installed boards must be initialized: They are then considered to be available by the software.

- Initializing the DAC board

AGEN Board	Set DAC
Count(Bit)	Set ≠0
Bitvalue	Confirm
- Initializing the Output Circuit

AGEN Board	Set OUT
Count(Bit)	Set ≠0
Bitvalue	Confirm
- Initializing the Low Dist Gen
(only if the option is installed)

AGEN Board	Set LOW DIST
Count(Bit)	Set ≠0
Bitvalue	Confirm

CAUTION: Only the installed boards may be initialized. If a board is initialized unintentionally, this cannot be cancelled. In this case, the UPD must be restarted.

7.3.7 Analog Motherboard Generator

Circuit diagram	1030.9060.01 S
Component location plan	1030.9060
Parts list	1030.9060.01 SA

7.3.7.1 Function

The Analog Motherboard is not a purely passive module where only the operating voltages and the signals are distributed between the individual plug-in modules, but contains active circuits both for the generator and the analyzer.

The operating voltages for the generator and the analyzer are routed via cable connector W20B from the Analog Power Supply to the Analog Motherboard. The circuit parts in the power supply and the motherboard and thus the generator and analyzer ground are completely independent of each other.

In the circuit diagram of the motherboard, the signal names are marked to indicate where they belong to:

Marking	Module
[D]	Digital Generator
[G]	Analog Generator
[A]	Analog Analyzer
none	Analog or Digital Analyzer

The Digital Generator is connected to the Analog Generator via the 16-contact flat cable W32, controlling it via two serial interfaces (GENCONN). Due to the floating design of the entire generator, all data signals must be taken via optocoupler.

- Connection between Digital and Analog Generator (GENCONN, circuit diagram sheet 2)

Part of the signals on the Digital Generator are not referred to with the same signal names as on the Analog Motherboard.

The relationship is illustrated by the opposite table:

Generator	
Analog	Digital
\overline{RD}	IAIRD
SD0	IAIDI
CLK	IAICLK
SDI	IAIDO
\overline{WR}	IAIWR
INT	GENINT
GD1	GD1
GDO	GDO
GFS	GFSX
GCLK	GCLK

- Interface for the signal D/A converter
(DAC LINK, circuit diagram sheet 2)

Serial interface for controlling the 20-bit signal DAC		
GCLK	Clock	Shift clock for the data the data bits are shifted with the positive edge
GDO	Data	serial data stream MSB first, twos complement, 24 bits (the upper 4 bits are shifted)
GD1	Data	second data channel, currently not used
GFS	Frame Sync	active 'Low', pulse width >40ns occurs with the falling edge of the clock pulse for the LSB the falling edge triggers the conversion
Gen ANLG 25kHz		Frame Sync = 96kHz Clock = 24*96kHz = 2.304MHz
Gen ANLG 110kHz		Frame Sync = 384kHz Clock = 24*384kHz = 9.2164MHz

This interface is only activated by the signal ENABLE=1 and is therefore deactivated during the system start (ENABLE=0): all the four lines are applied to 0.

- Serial data interface
(DATA LINK IN and OUT, circuit diagram sheets 2 and 3)

All the modules of the Analog Generator are connected one after the other like in a long shift register.

Serial interface for controlling the generator hardware		
CLK	Clock	shift clock for the data ($\approx 1.7\text{MHz}$) The data bits are shifted with the positive edge
SDI	Data in	serial data stream, MSB first
SDO	Data out	
$\overline{\text{WR}}$	Write	active 'Low', pulse width $\approx 200\text{ns}$ Data are transferred from the shift registers into the latch
$\overline{\text{RD}}$	Read	active 'Low', pulse width $\approx 200\text{ns}$ The board identification of the modules (8 bits each) is inserted into the data stream
INT	Interrupt	static signal, signals overdriving of the generator output
LDFREQ		TTL signal with the frequency of the Low Dist Generator (to Digital Analyzer)

At the output of optocoupler U203-A, which transfers the $\overline{\text{WR}}$ strobe, a lowpass is used to suppress high-frequency spikes, thus improving the interference immunity of data transfer.

Serial data stream:

The data are shifted further in blocks of 8 bits each with the rising edge of the clock. The data line is referred to as SDI at the input, SDATA[G] between the modules and SDO at the output. Via SDO[D], the data are read back into the Digital Generator.

Module	Bit number	Remark
DAC Board	16	currently not used
Output Circuit	84	
X23	0	
Low Dist Gen	60	
Enable Bit	1	
Sum of the bits	101	without Low Dist Gen
	161	with Low Dist Gen

(Number of bits including the board identification ID)

The table simultaneously reflects the sequence of the modules in the data stream:

The Enable Bit is the first one, the DAC Board the last one.

Since the entire data stream is always sent in blocks of 8 bits each, 104 bits are transferred in 13 blocks (3 bits **before** the Enable Bit) without the Low Dist Gen, 168 bits in 21 blocks (7 bits **before** the Enable Bit) with the Low Dist Gen. The last bit of the DAC board is always the last bit of the entire data stream.

During the selftest after switching on of the UPD, the board IDs of the modules are read in and checked in this sequence.

- Data Multiplexer

(DATA MUX X23 and X26, circuit diagram sheet 2)

These multiplexers switch the data stream for the optional modules which can be inserted in X23 (spare slot) or X26 (UPD-B1, Low Distortion Generator).

Without module inserted, the respective control line OPT[G] is open and is pulled to 0 using a pulldown resistor. The inserted module applies OPT[G] to +5V.

OPT[G]	Data stream
+5V	Module is inserted
0V	Data are not applied to the module

- Enable circuit

(ENABLE BIT, circuit diagram sheet 2)

ON Bit=1 normal operating status

OFF Bit=0 Signal DAC is switched off, since the AND gate D200 disables the signals from the Digital Generator.

The outputs of the generator are deactivated with high impedance.

The ENABLE line is routed from D310-B to all modules of the Analog Generator (see circuit diagram Analog Motherboard and description of the modules).

During switching on, the comparator circuit with N304 resets the flip-flop D310-B (Enable=0). After loading of the UPD software, Enable=1 is set by the software.

The function of the reset circuit is described in greater detail in section 7.3.7.3 Testing and Troubleshooting (see page 7.174).

7.3.7.2 Measuring Instruments

Measuring instrument	Specifications	R & S
DC Voltmeter	0.5%	UDS5, URE2/3 or UPD
Oscilloscope	Digital memory 4 channels, 100 MHz	—

7.3.7.3 Testing and Troubleshooting

1. Testing the Operating Voltages

DC measurement on flat cable W20B from the power supply or on the multipoint connectors of the modules.

Test values see external interfaces

CAUTION:

Not the chassis, but the generator ground GND[G] is used as reference ground.

- W20B.25, 26, 39, 40
- Screen of a generator module
- Male connector GEN COM on the front panel

2. Testing GENCONN

- Testing +5V[D]

DC measurement at W32.10 and .14: $+5V \pm 0.25V$

- Testing DAC LINK

Generator setting | Instrument ANLG 25kHz |

GCLK = 2.304 MHz

GFS = 96 kHz, T = 10.417 μs , pulse width 434ns

GDO transition 0 \leftrightarrow 1 with falling GCLK edge

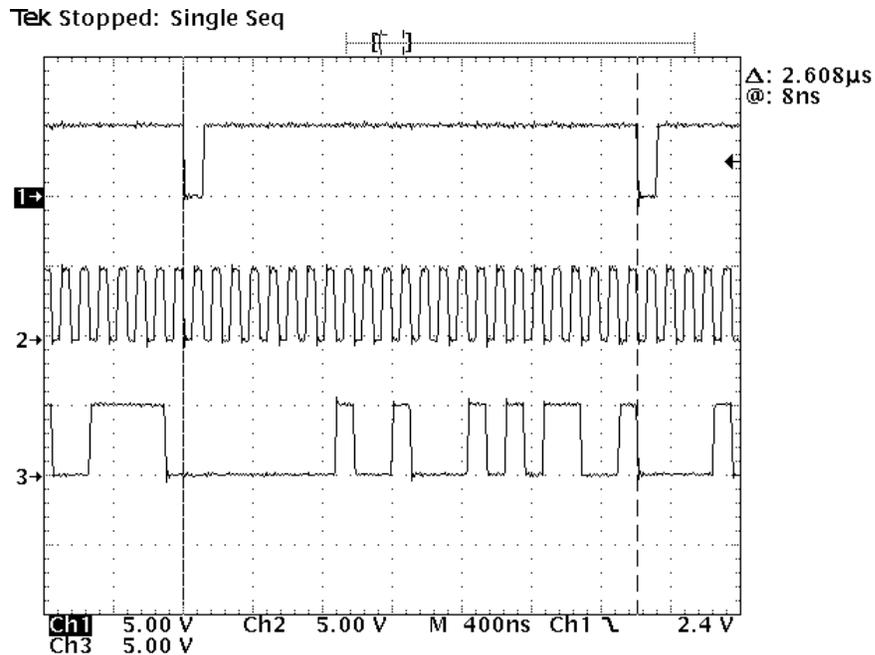
Generator setting | Instrument ANLG 110 kHz |

GCLK = 9.216 MHz

GFS = 384kHz, T = 2.604 μs , pulse width 108.5ns

GDO transition 0 \leftrightarrow 1 with falling GCLK edge

Trace the signals from the Digital Generator to the DAC Board using an oscilloscope.



DAC LINK, Generator ANLG110kHz

Trace1: GFS, X25 C16

Trace2: GCLK, X25 A16

Trace3: GD0, X25 A14

The signals are measured on multipoint connector X25 of the DAC board. The falling edge of Frame Sync (start of D/A conversion) occurs synchronously with the falling edge of the last clock pulse with which the LSB is transferred. The data are permanently being changed.

- Testing of DATA LINK

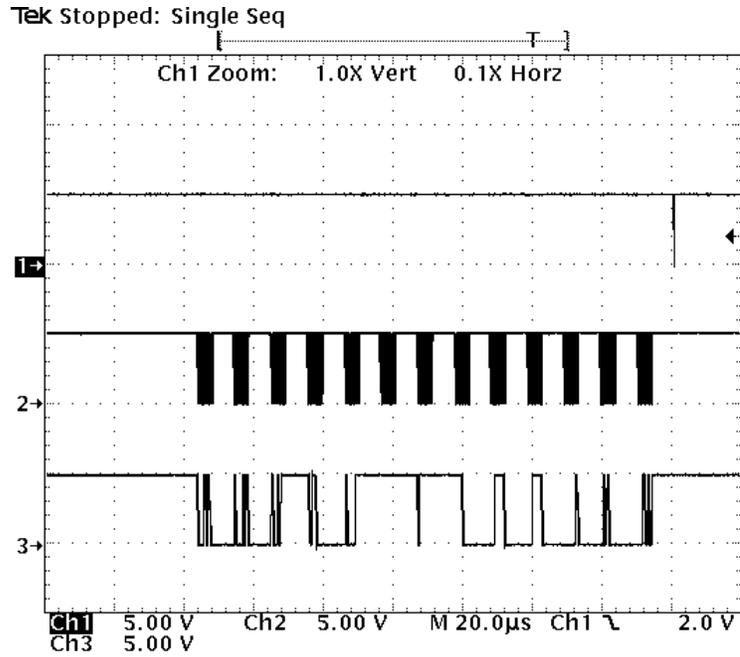
Generator setting:

- Function SINE
- Set level sweep ⇒ the hardware is set cyclically

Trace the signals CLK, SDI, \overline{WR} from the Digital Generator to the Generator Board using an oscilloscope.

Compared with the SDI line, the data signals on the SDATA lines are shifted to the right by the number of the bits of all preceding boards.

The \overline{WR} pulse is distorted at the input of gate D201.9 with a time constant of $562\Omega * 22pF \approx 12ns$.



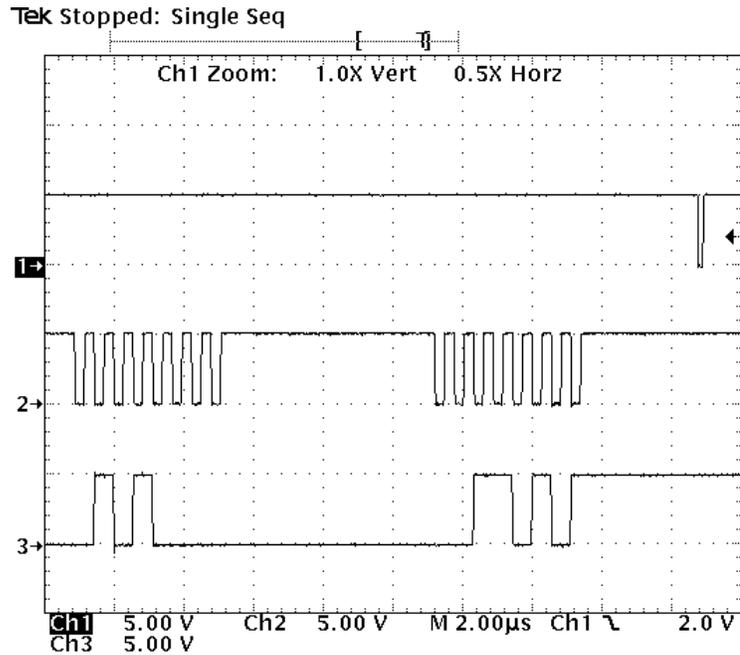
DATA LINK, transfer of the data stream in 13 blocks (Low Dist is not installed)

Trace1: \overline{WR}

Trace2: CLK

Trace3: SDI

The next illustration shows an expanded view of the transmission of the last two bytes before the \overline{WR} pulse.



These last two bytes in the entire data stream contain the 16 bits for the DAC Board:

- The last but one (left) byte is the board ID: 01010000 = 50H
- The last (right) byte is the contents of latch D201: 00110101

3. Testing the optocoupler interfaces

- Function

The input of each optocoupler is not directly driven with TTL level by a gate, but via a diode resistor circuit.

$V_i = H \approx 5V$ The diode BAS32 is reverse-biased. The input diode of the optocoupler is operated with a low current of ≈ 0.25 mA. The output transistor is high impedance and pulled to +5 V via a resistor:
 $V_o = H$

$V_i = L \approx 0V$ A current of ≈ 6 mA is flowing through the input diode of the optocoupler. The output transistor is low-impedance: $V_o = L$

The optocoupler interface is non-inverting. The delay time from the input to the output amounts to ≈ 40 ns, the maximum transmission frequency is about 20 MHz. The operating point at the input of the optocoupler is at ≈ 3.6 V. The current control causes only a small voltage deviation of about 100 mV and prevents capacitive coupling from the input referred to the chassis to the floating generator ground. Subsequent ACT gates (D200), D201) decouple the outputs of optocouplers U200 to U203, improve the slope and ensure the required driver power for controlling the analog modules.

- Testing

Trace the signal before and after the optocoupler using an oscilloscope:

TTL level, non-inverting, ≈ 40 ns delay time

CAUTION: Note the ground:

GND[G] Analog Generator, e.g. screen of a module

GND[G] Digital Generator, chassis

4. Testing the Enable Circuit (ENABLE BIT)

The enable bit of the serial data stream is stored in flip-flop D310 on the motherboard and taken via the ENABLE[G] line to all modules of the Analog Generator. During the start of the system, the comparator circuit with N304 resets flip-flop D310-B: Enable=0.

The DAC LINK is disabled with D200, undefined switch-on states are avoided on the analog boards, all generator outputs are high impedance.

After loading the UPD software, all analog boards are initialized and Enable=1 is set.

- Function of the reset circuit:

N304-A,-B are comparators with open-collector output. The comparator N304-A compares the +5-V operating voltage with the fixed reference of ≈ 1.2 V (forward voltage of the diodes) via a resistive voltage divider. While the operating voltage is built up, the output of N304-A remains low-impedance first and short-circuits capacitor C306. N304-B holds the $\overline{\text{Reset}}$ input of flip-flop D310-B at 0. The flip-flop is reset, ENABLE[G]=0.

If the +5-V operating voltage exceeds a threshold of ≈ 4 V, N304-A switches, the output becomes high-impedance, C306 is charged via R309. After ≈ 1.5 ms, this voltage exceeds the diode reference of 1.2 V, the output of N304-B is high-impedance. The $\overline{\text{Reset}}$ input

is set to 1, D310-B now operates as D flip-flop and the ENABLE[G] line can be set to 0 or 1 by the software.

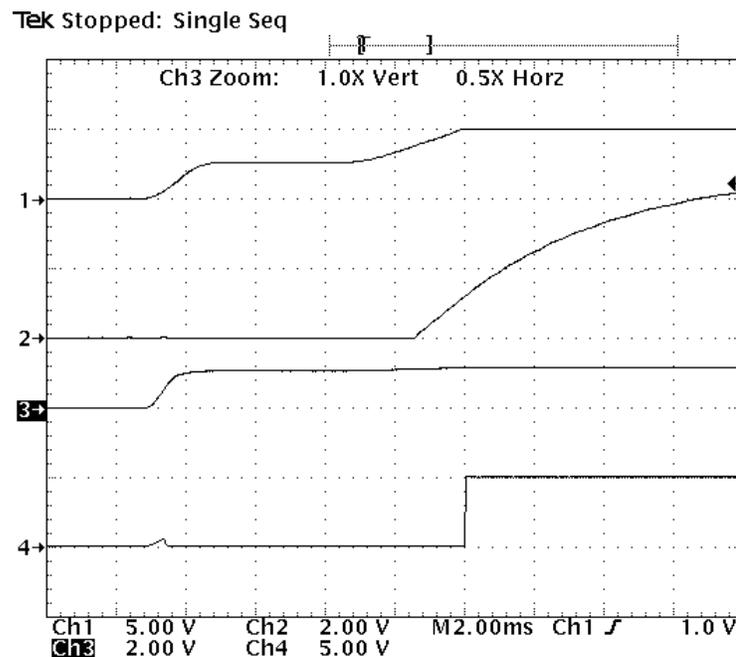
- Testing:

Connect the digital storage oscilloscope:

Trace1: +5V Operating voltage
 Trace2: N304.5 Charging characteristic of C306
 Trace3: N304.2 Diode reference 1.2 V
 Trace4: D310.13 $\overline{\text{Reset}}$ input

Switch the UPD off and on again

Compare the signal traces with the following illustration



5. Testing the board identification (BOARD ID)

Each module of the Analog Generator contains a parallel-in/serial-out shift register in the serial data stream. The byte at the parallel input of the shift register is coded with pull_up and pull_down resistors and designated as BOARD ID.

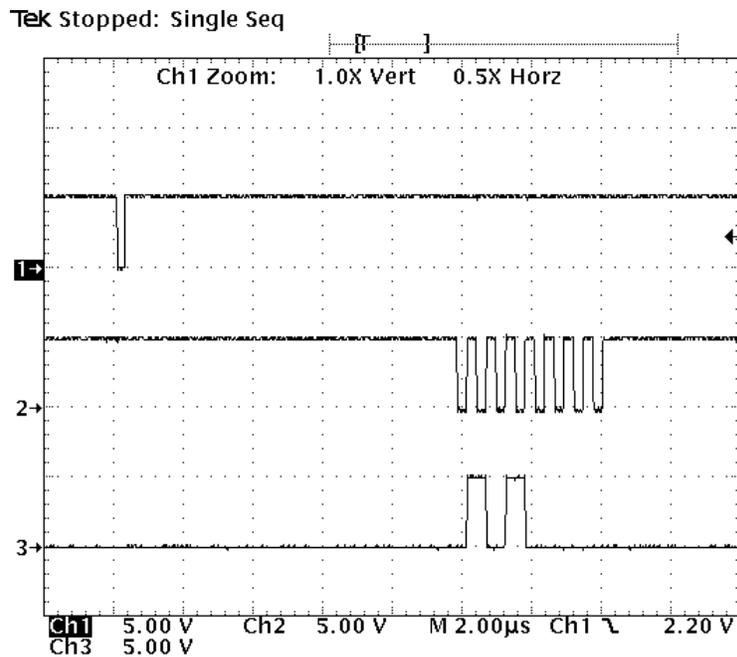
During system startup of the UPD, the BOARD ID is inserted into the serial data stream with the $\overline{\text{RD}}$ pulse, read in by the Digital Generator and checked during the selftest.

The signals $\overline{\text{RD}}$, CLK and SD0 are easily accessible on the modules at the following test points:

Signal	Dac Board	Output Circuit	Low Dist
$\overline{\text{RD}}$	X2.3	X105.3	X3.3
CLK	X2.4	X105.4	X3.4
SD0	X2.6	X105.6	X3.6

Connect digital storage oscilloscope with 10:1 probes to: $\overline{\text{RD}}$, CLK, SD0

- Quit UPD (<ctrl>F9)
- Trigger oscilloscope with single trigger on \overline{RD} signal
- Restart UPD (enter UPD)
- The data on the SD0 line change $\approx 20\text{ns}$ after the positive CLK edge and are valid during the negative edge. The BOARD ID appears with the first 8 CLK pulses after the \overline{RD} pulse (MSB first).
- The following illustration shows the signal traces for the DAC board.



Trace1: \overline{RD}

Trace2: CLK

Trace3: SD0, measured on DAC board

In the case of the other modules, \overline{RD} and CLK are the same, the data on SD0 correspond to the respective BOARD ID, see table:

Board	BOARD ID
Dac Board	01010000B = 50H
Output Circuit	01001000B = 48H
Low Dist Gen	01011000B = 58H

With each generator setting, the board IDs are also transferred in the data stream.

7.3.7.4 External Interfaces

Analog Motherboard						
name	Signal description	=	source dest.	range	connector	comment
Operating voltages generator, cable W20B, (circuit diagram sheet 7)						
-24V[G]	Output stage / Low Dist		P.supply	-24±1.2V < 250mA	W20B.29,30	
+24V[G]	Output stage		P.supply	24±1.2V < 250mA	W20B.27,28	
-15V[G]	Analog		P.supply	-15±0.75V < 315mA	W20B.31,32	
+15V[G]	Analog		P.supply	15±0.75V < 315mA	W20B.33,34	
+6V[G]	Relay		P.supply	6±0.2V < 840mA	W20B.35,36	
+5V[G]	Logic		P.supply	5±0.15V < 190mA	W20B.37,38	
GND[G]	Ground Gen				W20B.25,26,39,40	
Connection Digital Generator → Analog Generator, GENCONN, cable W32						
CLK [D]	Clock		all boards	TTL, 1 ... 3 MHz	W32.4	No interrupt Interrupt GEN 25kHz / 110kHz GEN 25kHz / 110kHz
SDI [D]	Data in		DacBoard	TTL	W32.5	
SDO [D]	Data out	O	EnableBit	TTL	W32.3	
/WR [D]	Write Data		all boards	TTL	W32.6	
/RD [D]	Read (Board ID)		all boards	TTL	W32.2	
INT [D]		O	OutCirc	TTL High TTL Low	W32.7	
GCLK[D]	Clock		DacB/X23	TTL 2.304MHz / 9.216MHz	W32.15	
GFS [D]	Frame Sync		DacB/X23	TTL 96kHz / 384kHz	W32.13	
GD0 [D]	Data in		DacBoard	TTL	W32.11	
GD1 [D]	Data in		X23	TTL	W32.9	
+5V [D]					W32.10,14	
GND [D]					W32.8,12,16	
N.C.					W32.1	
Shielded cables to front panel						
BAL 1-2	Channel1		OutCirc		X801.11	XLR, pin2
BAL 1-3	Bal (XLR)		OutCirc		X801.13	XLR, pin3
BAL 2-2	Channel2		OutCirc		X801.4	XLR, pin2
BAL 2-3	Bal (XLR)		OutCirc		X801.6	XLR, pin3
UNBAL 1 HI	Channel1		OutCirc		X801.8	Inner conductor
UNBAL 1 LO	Unbal (BNC)		OutCirc		X801.9	Outer conductor
UNBAL 2 HI	Channel2		OutCirc		X801.1	Inner conductor
UNBAL 2 LO	Unbal (BNC)		OutCirc		X801.2	Outer conductor
GND	Ground Gen				X801.15	
Ground	Chassis				X801.5,12	
DAC Board X25						
Output signal of DAC Board						
DAC SIG			OutCirc	2.50V ... 0.25V 2Hz ... 110kHz	X25.A1	
Serial data interface, DATA LINK						
CLK	Clock	O	DigGen	HCMOS, 1 ... 3 MHz	X25.A11	
SDI	Data in	O	DigGen	HCMOS	X25.C11	
SDATA	Data out		OutCirc	TTL	X25.A9	
/WR	Write Data	O	DigGen	HCMOS	X25.C10	
/RD	Read (Board ID)	O	DigGen	HCMOS	X25.A10	
ENABLE		O	DigGen	HCMOS	X25.C9	
Serial interface for the signal D/A converter, DAC LINK						
GCLK	Clock	O	DigGen	HCMOS	X25.A16	GEN

- continued -

- continued -						
name	Signal description		source dest.	range	connector	comment
GFS	Frame Sync	O	DigGen	2.304MHz / 9.216MHz HCMOS	X25.C16	25kHz / 110kHz GEN
GD0	Data in	O	DigGen	96kHz / 384kHz HCMOS	X25.A14	25kHz / 110kHz
Operating voltages						
-15V		O		$-15 \pm 0.75V < 200mA$	X25.A.C4	
+15V		O		$15 \pm 0.75V < 200mA$	X25.A.C5	
+6V		O		$6 \pm 0.2V < 80mA$	X25.A.C6	
+5V		O		$5 \pm 0.15V < 10mA$	X25.A.C7	
GND	Ground Gen				X25.C1	
N.C.					X25.A.C 2,3,8,12,13,15	
					X25.C14	
Output Circuit						
Input signals of the Output Circuit						
LOW DIST		O	LowDist	2.85V ... 0.25V 10Hz ... 110kHz Sine	X24.A31	
DAC SIG		O	DacBoard	2.50V ... 0.25V 2Hz ... 110kHz	X24.C31	
Output signals (Value range see data sheet)						
BAL 1-2	Channel1	I	Front panel		X24.C10	XLR, pin2
BAL 1-3	Bal (XLR)	I	Front panel		X24.A10	XLR, pin3
BAL 2-2	Channel2	I	Front panel		X24.C2	XLR, pin2
BAL 2-3	Bal (XLR)	I	Front panel		X24.A2	XLR, pin3
UNBAL 1 HI	Channel1	I	Front panel		X24.A8	Inner conductor
UNBAL 1 LO	Unbal (BNC)	I	Front panel		X24.C8	Outer conductor
UNBAL 2 HI	Channel2	I	Front panel		X24.A4	Inner conductor
UNBAL 2 LO	Unbal (BNC)	I	Front panel		X24.C4	Outer conductor
Serial data interface, DATA LINK						
CLK	Clock	O	DigGen	HCMOS, 1 ... 3 MHz	X24.A25	
SDATA	Data	O	DacBoard	HCMOS	X24.C25	
SDATA	Data	I	X23/Mux	TTL	X24.A23	
/WR	Write Data	O	DigGen	HCMOS	X24.C24	
/RD	Read (Board ID)	O	DigGen	HCMOS	X24.A24	
ENABLE		O	DigGen	HCMOS	X24.C23	
External signal (not used)						
EXT OUT		I	MothB X23	2.5V / 2Hz...110kHz	X24.C28	
EXT IN		O	MothB X23	2.5V / 2Hz...110kHz	X24.A28	
Overload Interrupt						
INT		I	DigGen	> +10V < -10V	X24.A22	no interrupt Interrupt
Operating voltages						
-24V		O		$-24 \pm 1.2V < 250mA$	X24.A14,C14	
+24V		O		$-24 \pm 1.2V < 250mA$	X24.A15,C15	
-15V		O		$-15 \pm 0.75V < 80mA$	X24.A17,C17	
+15V		O		$15 \pm 0.75V < 80mA$	X24.A18,C18	
+6V		O		$6 \pm 0.2V < 700mA$	X24.A20,C20	
+5V		O		$5 \pm 0.15V < 40mA$	X24.A21,C21	
GND	Ground Gen				X24.A.C 1,3,5,7,9,11, 12,13,16	
					X24.A.C 19,26,27,29,30, 32	
Ground	chassis				X24.C 22	
					X24.A.C 6	
Low Distortion Generator						
- continued -						

- continued -						
name	Signal description	⇒	source dest.	range	connector	comment
Output signals of Low Distortion Generator						
LOW DIST	Sine	O	OutCirc	2.85V ... 0.25V 10Hz ... 110kHz	X26.A16	
LDFREQ		O	DigAna	Sine L: 10Hz ... 110kHz L: 3 ... 8mA H: 0 ... 0.5mA (Voltage ≈ 3.6V)	X26.A1	
Serial data interface, DATA LINK						
CLK	Clock	O	DigGen	HCMOS, 1 ... 3 MHz	X26.A6	
SDATA	Data	O	Mux X23	HCMOS	X26.C6	
SDATA	Data	I	Mux X26	TTL	X26.A4	
/WR	Write Data	O	DigGen	HCMOS	X26.C5	
/RD	Read (Board ID)	O	DigGen	HCMOS	X26.A5	
ENABLE		O	DigGen	HCMOS	X26.C4	
+5V(OPT)	to Data Mux X26	E		5±0.15V	X26.A7	
Operating voltages						
-24V		O		-24±1.2V < 15mA	X26.A8,C8	
-15V		O		-15±0.75V < 150mA	X26.A9,C9	
+15V		O		15±0.75V < 100mA	X26.A10,C10	
+6V		O		6±0.2V < 35mA	X26.A11,C11	
+5V		O		5±0.15V < 10mA	X26.A12,C12	
GND	Ground Gen				X26.C 1,7,16 X26.A,C 2,3,13,14,15	
spare slot X23 (Generator)						
Signal from/to Output Circuit						
EXT	from X23	I	OutCirc	2.5V / 2Hz...110kHz	X23.C14	
EXT	to X23	O	OutCirc	2.5V / 2Hz...110kHz	X23.B14	
Serial data interface, DATA LINK						
CLK	Clock	O	DigGen	HCMOS, 1 ... 3 MHz	X23.B12	
SDI	Data	O	Mux X23	HCMOS	X23.C10	
SDO	Data	I	Mux X23	TTL	X23.B10	
/WR	Write Data	O	DigGen	HCMOS	X23.B11	
/RD	Read (Board ID)	O	DigGen	HCMOS	X23.A11	
ENABLE		O	DigGen	HCMOS	X23.A10	
+5V(OPT)	to Data Mux X23	I		5±0.15V	X23.B12	
Serial interface for a signal D/A converter, DAC LINK						
GCLK	Clock	O	DigGen	HCMOS 2.304MHz / 9.216MHz	X23.B16	GEN 25kHz / 110kHz
GFS	Frame Sync	O	DigGen	HCMOS	X23.C16	GEN 25kHz / 110kHz
GD1	Data in	O	DigGen	HCMOS 96kHz / 384kHz	X23.A16	
Operating voltages						
-15V		O		-15±0.75V	X23.C13	
+15V		O		15±0.75V	X23.C12	
+6V		O		6±0.2V	X23.C11	
+5V		O		5±0.15V	X23.A14	
GND	Ground Gen				X23.C1 X23.A,B,C 9,15 X23.A,B 13	
Explanation: ⇒: I:Input, O:Output, B:Bidirectional, P:Power						

Since all the signal names are associated with the Analog Generator, the designation [G] has been omitted. The designation is only indicated for GENCONN and the connection W20 B to the power supply (for differentiation from the analyzer voltages).

In contrast to the interface description of the remaining modules, the following applies to the item ⇒ Source/destination in the case of the motherboard:

I: Input to the motherboard: Where does the signal go to

O: Output from the motherboard: Where does the signal come from

7.3.8 DAC Board

Circuit diagram	1030.9460.01 S
Component location plan	1030.9460
Parts list	1030.9460.01 SA

7.3.8.1 Function

All signals (except for the squarewave signal) are generated by a 20-bit audio D/A converter (D204), which is controlled by the Digital Generator via a serial interface. The signals are transferred from the Digital Generator via the 16-contact flat cable W32 to the Analog Motherboard.

- DAC LINK

Serial interface for controlling the 20-bit signal DAC		
GCLK	Clock	Shift clock for the data the data bits are shifted with the positive edge
GDO	Data	Serial data stream MSB first, twos complement, 24 bits (the most significant 4 bits are shifted)
GFS	Frame Sync	active 'Low', pulse width >40ns comes with the falling edge of the clock pulse for the LSB the falling edge starts the conversion
Gen ANLG 25kHz		Frame Sync = 96kHz Clock = 24*96kHz = 2.304MHz
Gen ANLG 110kHz		Frame Sync = 384kHz Clock = 24*384kHz = 9.2164MHz

- Signal DAC

(SIGNAL DAC, circuit diagram sheet 2)

As output signal, the DAC provides a current to ground. The opamp N202, operated as inverter, generates a virtual ground at the output of the DAC. The current I from the DAC flows via the feedback resistor R_{fb} (R_{fb} is about $3k\Omega$ and is installed in the DAC) and generates the signal voltage V_o at the output of the opamp.

Fullscale (FS): $I(\pm FS) = \pm 1mA \Rightarrow V_o(\pm FS) = \pm 3V$

The DAC is operated with only about 0.95FS, therefore the voltage applied to X30 is $\approx 2V_{rms}$ with a sinewave signal.

- 25-kHz Lowpass

(LOWPASS 25 kHz, circuit diagram sheet 3)

An active 9th-order lowpass (N300...303) suppresses the clock of the signal D/A converter (96 kHz) by more than 110 dB. This lowpass is implemented as FDNR filter (Frequency Dependent Negative Resistor) and acts as an elliptical 9th-order LC lowpass filter terminated on both sides. At its output (N332.3), the signal is attenuated by 6 dB in the passband. Opamp N332 raises the level by 6 dB again.

At the output P32, the bias currents of the bipolar opamps generate a large DC offset of a few 100 mV, which is suppressed by a 1st-order highpass filter (C339, R335, N333). In

conjunction with the 1st-order lowpass filter (C330, R326, N330), this highpass constitutes a diplexer. The transfer frequency is about 5.4 Hz. An additional 3rd-order lowpass (N331 and R330, R331, C336) also suppresses the clock of the signal D/A converter in the lowpass path.

In order to avoid frequency response errors, the signals from the highpass and lowpass path of the diplexer are applied via identical resistors to inverter N334 and thus added. A current for correction of the remaining offset is applied there via R338.

The following circuit is a 2nd-order Chebishev lowpass, correcting the $\sin(x)/x$ frequency response caused by the D/A conversion: 3-dB amplification at ≈ 50 kHz, 0 dB at ≈ 75 kHz.

The voltage at P35 is $\approx 2.5V_{rms}$ with a sinewave signal.

- 110-kHz lowpass

(LOWPASS 110 kHz, circuit diagram sheet 4)

Same as 25-kHz lowpass, except for:

- Clock of the signal D/A converter is 384 kHz
- Additional lowpass is simpler (only R430, R431, C436)
- The $\sin(x)/x$ correction is implemented as bandpass filter.
(Resonance at ≈ 320 kHz with ≈ 6 -dB amplification)

- Squarewave generation

(SQUARE, circuit diagram sheet 5)

The squarewave signal from the 25-kHz lowpass is taken via jumper X50 and relay K22 to comparator N500 \rightarrow squarewave with HCMOS level. The frequency of this squarewave is divided by 2 in flip-flop D500-A, producing an excellent symmetry of the squarewave (even harmonic is very low, typ. -80 dB). The operating voltage of the flip-flop determining the amplitude of the squarewave, the comparator and the flip-flop are provided with their own +5-V supply (N501). The output signals Q and \bar{Q} are combined in differential amplifier N502-A: the DC component is eliminated, amplitude $4.75V_{pp}$.

N502-B: Inverter: $g = -1.115$
switchable band limiting with D501
(for DIM signals 30 kHz or 100 kHz, for squarewave ≈ 400 kHz)

The amplitude of the squarewave (at N502.7 or P61) is about 2.65 V

- MODDIST lowpass

(LP SMPTE, circuit diagram sheet 6)

This lowpass is only used if the generator generates a MODDIST signal and the Low Distortion Generator is switched on. The DAC Board then provides the AF noise signal and the lowpass ensures a high noise suppression in the vicinity of the wanted RF signal from the Low Distortion Generator.

4th-order Chebishev lowpass filter

Passband: < 700 Hz, max. ± 0.3 dB ripple

Stop band: > 4 kHz, 50 dB attenuation

7.3.8.2 Controlling the Analog Functions

device	BITS			function
	Pos.	Count	Bitvalue	
Latch D201 K21, K20	0	2	0 1 2 3	not useful, but permissible Lowpass 25 kHz on Lowpass 110 kHz off not useful, but permissible
K22	2	1	0/1	Square circuit off/on
D500-A	3	1	0/1	Square signal off/on
D501	4	2	0 1 2 3	not used Bandwidth 100 kHz (DIM) Bandwidth 30 kHz (DIM) Bandwidth >300kHz (square)
K23	6	1	0/1	LP SMPTE off/on
	7	1	x	not assigned
D202	8	8	50H	Board identification BOARD ID is inserted into the data stream with the \overline{RD} pulse

7.3.8.3 Measuring Instruments

Measuring instr.	Specifications	R & S
Sinewave generator	2Hz...300kHz	AFG, AFGU or ADS
DC voltmeter	0.5%	UDS5, URE2/3 or UPD
AC voltmeter	2Hz...110kHz	URE3
Oscilloscope	—	—
Frequency counter	50ppm	UPD

7.3.8.4 Testing and Troubleshooting

1. Testing the jumpers

X30.1 - .2
 X31, X34
 X41, X44
 X50.1 - .2
 X54.1 - .2
 X55
 X60.1 - .2

2. Testing the operating and reference voltages

Test point	Nom. value	Tolerance
X21.1	+5V	± 0.15V
.2	+15V	± 0.75V
.3	-15V	± 0.75V
.4	+6V	± 0.20V
P20	+12V	± 0.60V
P21	-12V	± 0.60V
P50	+5V	± 0.25V
X22.1	+6.2V	± 0.31V
X22.1	-6.2V	± 0.31V

3. Testing the board identification (BOARD ID)

The byte at the parallel input of shift register D202 (coded with pull_up and _down resistors) is referred to as BOARD ID.

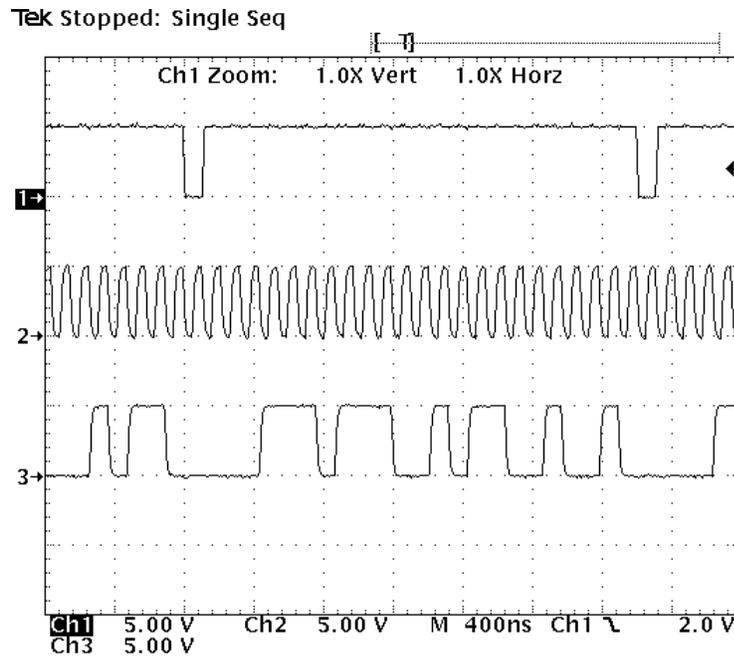
BOARD ID = 01010000B = 50H

The BOARD ID is inserted into the serial data stream with the \overline{RD} pulse and read in by the Digital Generator during the system start of the UPD only.

Testing see Analog Motherboard (page 7.175)

4. Testing SIGNAL DAC

The following illustration shows the digital signals applied to the serial input of the D/A converter:



DAC LINK, recorded with generator ANLG 110kHz

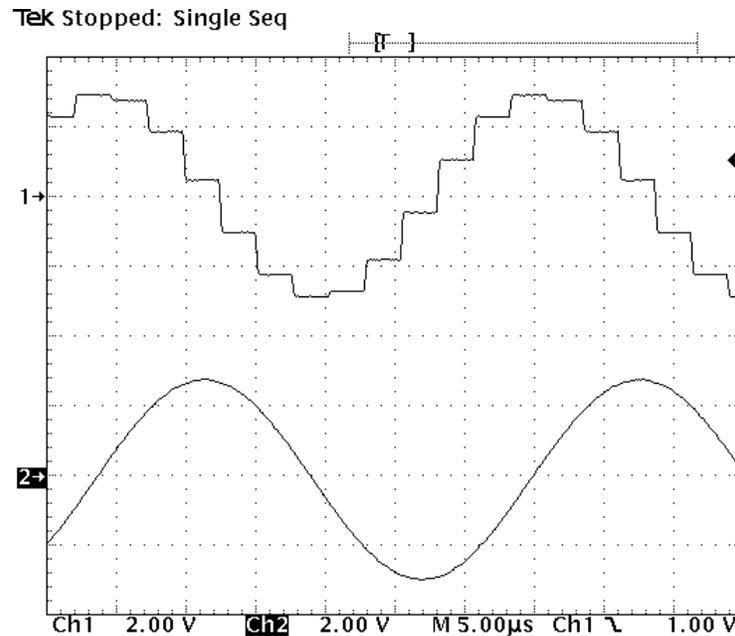
Trace1: GFS, D204.6

Trace2: GCLK, D204.5

Trace3: GD0, D204.7

The signals are directly measured on D/A converter D204. The clock signal and the data signal are somewhat distorted by the series resistors. The falling edge of the Frame Sync GFS starts the D/A conversion and occurs synchronously with the falling edge of the last clock pulse with which the LSB is transferred. The data change permanently.

The next illustration shows the signals at output X30 of the D/A converter and at output P42 of the following reconstruction lowpass:



- Trace1: Signal at X30
 Signal frequency 32 kHz
 Generator ANLG 110kHz (sampling frequency 384 kHz)
 The stair-case waveform produced by the D/A conversion can easily be seen
 The duration of one step is $1/384k Hz = 2.604\mu s$
- Trace2: Signal at P42
 The lowpass suppresses the clock frequency of the D/A converter
 A low DC offset of about -100 mV can be seen

5. Testing LOWPASS 25kHz

- Testing the frequency response adjustment
 - Record frequency response at P35 from 2 Hz to 25 kHz, the voltage at 2 kHz is the reference
 - Typical characteristic of the frequency response: from 2 Hz to 20 kHz completely flat ($\pm 0.15\%$) above 20kHz slightly falling by 0.25%
 - Falling or rising between 2 Hz and 20 Hz
 ⇒ LF adjustment (with R336) faulty
 - Staircase between 20 Hz and 2 kHz
 ⇒ FDNR adjustment (with C351) faulty
 - Falling or rising at 20 kHz
 ⇒ RF adjustment (with R344) faulty
 - The adjustment is described in section Adjustment and Calibration, page 7.121.

- Testing the adjustment range of the trimmers

Generator setting	Instrument	ANLG 25kHz
	Function	SINE
	Frequency	see measurement

Test point: P61 or X1.A1 (Signal output)

Measurement: Turn trimmer from minimum to maximum, measure voltage

- C351: Voltage change > 2.5%, measurement at 1 kHz
- R336: Voltage change > 8.0%, measurement at 10 Hz
- R344: Voltage change > 0.75%, measurement at 20 kHz

After testing set the trimmers approximately to center position!

- Testing DC offset

Generator setting | Instrument ANLG 110kHz |

⇒ The input of the 25-kHz lowpass is applied to ground.

DC measurement at P32: Tolerance: $-700mV < V_{dc} < 0V$, *typ* $-300mV$

- Testing the offset supply

Generator setting | Instrument ANLG 110kHz |

⇒ The input of the 25-kHz lowpass is applied to ground.

Test point: P61 or X1.A1 (signal output)

Use R337 to check the adjustment range: $-100mV < V_{dc} < +100mV$

then use R337 to adjust to $0 \pm 5mV$

- Testing the frequency response: lowpass 25kHz

Generator setting	Instrument	ANLG 25kHz
	Function	SINE
	Frequency	see measurement

- Remove jumper X30

- Feed in signal: Sine, 1 kHz, $2V_{rms}$: at X30.2 (ground applied to X30.3)

Measurement:

- Remove jumper X31

- AC at X30: → reference

- AC at P34: $1.68dB \pm 0.25dB$, → new reference

- Frequency response measurement by way of the following table

Frequency	AC at P34 (in dB)
1kHz ... 25kHz	0 ± 0.25
40kHz	< -21
50kHz	< -54
60kHz	< -80
> 70kHz	< -100

The measurements can be performed using the UPD analyzer:

- selective RMS measurement, Freq Mode FIX
- Readout in dB.

- Testing the frequency response: additional lowpass

Generator setting	Instrument	ANLG 25kHz
	Function	SINE
	Frequency	see measurement

- Remove jumper X30

- Feed in signal: Sine, 100 Hz, $2V_{rms}$: at X30.2 (ground at X30.3)

Measurement:

- AC at X30: → reference
- AC at P34: $1.68\text{dB} \pm 0.25\text{dB}$, → new reference
- Remove jumper X34
- Apply N332.3 to ground (to avoid crosstalk)
- Frequency response measurement by way of the following table

Frequency	AC at P34 (in dB)
100Hz	< -20
1kHz	< -40
10kHz	< -60
50kHz	< -108

The measurements can be performed using the UPD analyzer:

- selective RMS measurement, Freq Mode FIX
- Readout in dB.
- Testing the diplexer

Generator setting	Instrument	ANLG 25kHz
	Function	SINE
	Frequency	5.40 Hz

 - Measure voltage at P34 ($\approx 2.5V_{rms}$) → reference
 - Remove jumper X31: ⇒ -3dB at P34, reinsert jumper
 - Remove jumper X34: ⇒ -3dB at P34, reinsert jumper
- Frequency response $\sin(x)/x$ correction

Generator setting	Instrument	ANLG 25kHz
	Function	SINE
	Frequency	see measurement

Frequency = 1kHz

- Measure AC at P34: $\approx 2.50\text{V}$, → reference
- Measure AC at P35: $0\text{dB} \pm 0.25\text{dB}$

Frequency = 20kHz

- Measure AC at P34: $\approx 2.25\text{V}$, → reference
- Measure AC at P35: $1\text{dB} \pm 0.25\text{dB}$

6. Testing LOWPASS 110kHz

- Testing the frequency response adjustment
 - Record frequency response at P61 from 2 Hz to 110 kHz, the voltage at 15 kHz is the reference
 - Typical characteristic of the frequency response:
 - from 2 Hz to 20 kHz completely flat ($\pm 0.15\%$)
 - above 20 kHz slight ripple ($\pm 0.3\%$)
 - Falling or rising between 2 Hz and 20 Hz
 - ⇒ LF adjustment (with R436) faulty

- Staircase between 150 Hz and 15 kHz
⇒ FDNR adjustment (with C454) faulty
- Falling or rising at 100 kHz
⇒ RF adjustment (with R444) faulty
- The adjustment is described in section Adjustment and Calibration, page 7.122.
- Testing the adjustment range of the trimmers

Generator setting	Instrument	ANLG 110kHz
	Function	SINE
	Frequency	see measurement

Test point: P61 or X1.A1 (signal output)

Measurement: turn trimmer from minimum to maximum, measure voltage

- C454: Voltage change > 2.25%, measurement at 10 kHz
- R436: Voltage change > 8.0%, measurement at 10 Hz
- R444: Voltage change > 3.5%, measurement at 100 kHz

After testing, set the trimmers approximately to center position!

- Testing the DC offset

Generator setting	Instrument	ANLG 25kHz
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 ⇒ The input of the 110-kHz lowpass is applied to ground.
 DC measurement at P42: Tolerance: $-250mV < V_{dc} < 0V$, *typ* $-70mV$
- Testing the offset supply

Generator setting	Instrument	ANLG 25kHz
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 ⇒ The input of the 110-kHz lowpass is applied to ground.
 Test point: P61 or X1.A1 (signal output)
 Use R437 to check the adjustment range: $-100mV < V_{dc} < +100mV$
 then use R437 to adjust to $0 \pm 5mV$
- Testing the frequency response: 110-kHz lowpass

Generator setting	Instrument	ANLG 110kHz
	Function	SINE
	Frequency	see measurement

- Remove jumper X30
- Feed in signal: Sine, 1 kHz, $2V_{rms}$: at X30.2 (ground at X30.3)

Measurement:

- Remove jumper X41
- AC at X30: → reference
- AC at P44: $1.68dB \pm 0.25dB$, → new reference
- Frequency response measurement by way of the following table

Frequency	AC at P44 (in dB)
1kHz ... 25kHz	0 ± 0.25
25kHz ... 110kHz	0 ± 0.35
160kHz	< -20
180kHz	< -40
220kHz	< -80
$> 270kHz$	< -100

The measurements can be performed using the UPD analyzer:

- selective RMS measurement, Freq Mode FIX
- Readout in dBr.

- Testing the frequency response: additional lowpass

Generator setting	Instrument	ANLG 110kHz
	Function	SINE
	Frequency	see measurement

- Remove jumper X30
- Feed in signal: Sine, 100 Hz, $2V_{rms}$: at X30.2 (ground at X30.3)

Measurement:

- AC at X30: → reference
- AC at P44: $1.68\text{dB} \pm 0.25\text{dB}$, → new reference
- Remove jumper X44
- Apply N432.3 to ground (to avoid crosstalk)
- Frequency response measurement by way of the following table:

Frequency	AC at P34 (in dB)
100Hz	< -20
1kHz	< -40
10kHz	< -60
100kHz	< -90
200kHz	< -100

The measurements can be performed using the UPD analyzer:

- selective RMS measurement, Freq Mode FIX
- Readout in dBr.

- Testing the diplexer

Generator setting	Instrument	ANLG 110kHz
	Function	SINE
	Frequency	5.40 Hz

- Measure voltage at P44 ($\approx 2.5V_{rms}$) → reference
- Remove jumper X41: ⇒ -3dB at P44, reinsert jumper
- Remove jumper X44: ⇒ -3dB at P44, reinsert jumper

- Frequency response $\sin(x)/x$ correction

Generator setting	Instrument	ANLG 110kHz
	Function	SINE
	Frequency	see measurement

Frequency = 1kHz

- Measure AC at P44: $\approx 2.50\text{V}$, → reference
- Measure AC at P45: $0\text{dB} \pm 0.25\text{dB}$

Frequency = 100kHz

- Measure AC at P44: $\approx 2.25\text{V}$, → reference
- Measure AC at P45: $1\text{dB} \pm 0.25\text{dB}$

7. Testing the squarewave generation

•	Generator setting	Instrument	ANLG 25kHz
		Function	SQUARE
		Frequency	1kHz

• Testing the squarewave generation

The signals can be checked by way of the following table:

Test point	Signal
X50	$2.5V_{rms}$ 2kHz Sine
N500.7	$5V_{pk}$ 2kHz Square
X54	$5V_{pk}$ 1kHz ∴
X55	$5V_{pk}$ ∴
N502.1	$4.75V_{pp}$
N502.7	$5.30V_{pp}$
X60	$5.30V_{pp}$

• Testing the waveform at P60

Measurement using oscilloscope:

- no overshoots, symmetrical, free from DC

• Testing the DIM limit frequencies

–	Generator setting	Instrument	ANLG 25kHz
		Function	SQUARE
		Frequency	100Hz

– Switch over the DIM limit frequencies in service mode:
(see also controlling the analog functions)

OPTIONS Panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	DAC
	Position	4
	Count(Bit)	2
	Bitvalue	see table
	Execute	YES

– Testing the limit frequencies:

- Remove jumper X50
- Feed in signal: Sine, 100Hz, $2.5V_{rms}$: at X50.2 (ground at X50.3)
- Remove jumper X55
- Remove jumper X54 and insert on .2 .3
- Measure voltage at X60: Sine, ($\approx 1.3V_{rms}$), → reference
- further settings and measurement according to table:

Bit value	Frequency	⇒ Voltage at X60
2	30kHz	$-3dB \pm 0.5dB$
1	100kHz	$-3dB \pm 0.5dB$
3	300kHz	$-2dB \pm 1.0dB$
3	500kHz	$-5dB \pm 2.0dB$

8. Testing the LP SMPTE

- Generator setting

Instrument	ANLG 25kHz
Function	SINE
Frequency	100Hz
- Cut in the lowpass filter LP SMPTE in service mode:
(see also controlling the analog functions)

OPTIONS Panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	DAC
	Position	6
	Count(Bit)	1
	Bitvalue	1
	Execute	YES

- Testing the frequency response
 - Measure voltage at X60 ($\approx 2.5V_{rms}$) → reference
 - Measure voltage at P61:
 - Passband: < 700Hz, max ± 0.3 dB ripple
 - Stop band: > 4kHz, attenuation >40dB, typ. 50dB

7.3.8.5 External Interfaces

Motherboard connector X1						
name	Signal description	≡	source dest.	range	connector	comment
Output signal						
DAC SIG		O	OutCirc	2.50V ... 0.25V 2Hz ... 110kHz	X1.A1	
Serial data interface DATA LINK						
CLK.	Clock	I	DigGen	TTL, 1 ... 3 MHz	X1.A11	
SDI	Data in	I	DigGen	TTL	X1.C11	
SDO	Data out	O	OutCirc	HCMOS	X1.A9	
/WR.	Write Data	I	DigGen	TTL	X1.C10	
/RD.	Read (Board ID)	I	DigGen	TTL	X1.A10	
ENABLE		I	MothBoard	TTL	X1.C9	
Serial interface for the signal D/A converter DAC LINK						
GCLK	Clock	I	DigGen	TTL 2.304MHz / 9.216MHz	X1.A16	GEN 25kHz / 110kHz
GFS	Frame Sync	I	DigGen	TTL 96kHz / 384kHz	X1.C16	GEN 25kHz / 110kHz
GD0	Data in	I	DigGen	TTL	X1.A14	
Operating voltages						
-15V		I		-15±0.75V < 200mA	X1.A.C4	
+15V		I		15±0.75V < 200mA	X1.A.C5	
+6V		I		6±0.2V < 80mA	X1.A.C6	
+5V		I		5±0.15V < 10mA	X1.A.C7	
Ground					X1.C1 X1.A.C 2,3,8 X1.A.C 12,13,15	
N.C.					X1.C14	
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

7.3.9 Output Circuit

Circuit diagram	1030.9290.01 S
Component location plan	1030.9290
Parts list	1030.9290.01 SA

7.3.9.1 Function

The output signals of the DAC Board (referred to as DAC SIG in the following) and of the Low Distortion Generator (referred to as LOW DIST in the following) are taken to the Output Circuit via multipoint connector X1.

The signal is directly taken (via the relays K238, K236, K237, K239) to the LEVEL CONTROL circuit unless one of the following signals has been selected (see also section 6.1.4 Analog Signal Generation, page 6.12):

- DFD signal without Low Distortion Generator
→ HP DIFF cut in
- DFD signal with Low Distortion Generator
→ HP DIFF and SIGNAL ADDER cut in
- MODDIST signal with Low Distortion Generator
→ SIGNAL ADDER cut in
- DIM signal (only possible with Low Distortion Generator)
→ SIGNAL ADDER cut in

At the input of the LEVEL CONTROL circuit (X300), all signals are set such that they feature the same peak value of about 3.54 V ($\hat{=} 2.5V_{rms}$ with sine).

Exception: the squarewave signal is set to $V_{peak} = 2.65V$ (even with DIM signal).

- DFD highpass

(HP DIFF, circuit diagram sheet 2)

This highpass is only cut in with DFD signals, improving the signal-to-noise ratio of the DAC SIG signal for frequencies < 1 kHz from 100 dB to 130 dB.

3rd-order Chebishev highpass

Stop band: < 1 kHz, 30-dB attenuation

Passband: > 5 kHz, max ± 0.3 dB ripple

- Signal adder

(SIGNAL ADDER, circuit diagram sheet 2)

The signal adder is implemented using an operational amplifier (N200) connected up as inverting summing amplifier with two inputs. Using the relays K236 and K237, the two input signals DAC SIG and LOW DIST are either through-connected separately or added with N200.

In the case of addition:

The LOW DIST signal is applied via relay K237 and attenuated by 6 dB. The additional level setting required for the signals MODDIST and DIM is performed on the Low Distortion Generator by means of the IMD ATTEN circuit.

The DAC SIG signal is applied via relay K236.

With the DFD signal, K301 is open, the attenuation is 6 dB.

With the SMPTE or DIM signal, K301 is closed, the attenuation is 0 dB.

- Level setting

(LEVEL CONTROL, circuit diagram sheet 3)

The entire circuit acts like a multiplying D/A converter with 16-bit resolution. The maximum gain is 0 dB if K300 is closed. By opening relay K300, this maximum gain (referred to as N302_gain) can be switched from 0 dB to 7.722 dB.

The 16 bits No. 8 to 23 in the data stream of the Output Circuit (12 bits in the DAC D300, 4 bits in N301) are referred to as Level_bits: Level_Bits = 0...FFFFH (0...65535).

(see also controlling the analog functions, page 7.198).

The amplifier N302 is connected up as inverter:

Gain $|g| = R2 / R1 =: \text{Level_gain} * \text{N302_gain}$

R1 = Coupling resistor: R300, 301, ..., 309, D300, N300
2.5k Ω / Level_gain
(minimally 2.5k Ω , 16-bit resolution)

R2 = negative-feedback resistor:
R318 || R319 = 2.5k Ω or R319 = 6.19k Ω alone
 \Rightarrow additional gain N302_gain switchable with K300
N302_gain = R319 / 2.5k Ω = 2.4329 (7.722dB) or
N302_gain = R318 || R319 / 2.5k Ω = 1 (0dB)

The gain Level_gain is specified by:

Level_gain = (65535 - Level_bits) / 65536 = 0 ... 1

Except for the case that the attenuator is already set to the maximum attenuation of 84 dB, only the range between 0.25 and 1.0 (-12dB ... 0dB) is used for Level_gain.

Due to the extreme requirements placed on distortion factor and noise, the most significant 4 bits are implemented discretely: FETs V314 to V317 connect the associated binary-coded resistors R300 to R305 through. The bipolar transistors V310 to V313 pull the drains of the reverse-biased FETs to ground; therefore, they are not driven and are free from distortions.

- Offset DAC

(OFFSET DAC, circuit diagram, sheet 4)

- Offset DAC1 for output stage V1:

The 12 bits of the DAC D400 are referred to as Offset_dac1.

The voltage $V_{ref} = 6.2V$ ($\pm 5\%$) is applied to the input (pin 15) of the 12-bit DAC D400.

\Rightarrow Voltage at output of opamp N400-A: $-V_{ref} * \text{Offset_dac1}/4096$

Output of N400-B (P400):

$$V_o = 6.2 * 33.2 / 20 * (1 - 2 * Offset_dac1 / 4096) = 10.3V * (1 - 2 * Offset_dac1 / 4096)$$

$$Offset_dac1 = 0 \dots FFFH (0 \dots 4095) \Rightarrow V_o = -10.3V \dots + 10.3V$$

Via R407,408, a current is fed into the output stage V1, causing an offset of max. $\pm 200\text{mV}$ at its output (V1_OUT).

- Offset DAC2 for output stage V2:

D401, N401, P401

$$Offset_dac2 = 0 \dots FFFH (0 \dots 4095), \text{ feed-in into output stage V2}$$

- Overload Interrupt

(Circuit diagram, sheet 4)

N404, N403 Dual comparators, open-collector

Outputs connected as 'wired-or'

N402 Dual opamp

The two comparators are connected up as window comparators with thresholds of $\pm 0.3\text{ V}$.

If jumpers X400 and X401 are plugged in and the output stages V1 and V2 operate in normal mode, a voltage of about 0 V is applied to the inputs 2 and 5 of N404 and N403. All outputs are high-impedance: +15 V at the input N402.2, $\Rightarrow > 10\text{ V}$ at P402

If one of the output stages is overdriven (e.g. by a short-circuit at the output), the voltage at its inverting input increases to +0.7 V or -0.7 V (limitation to a diode voltage). At least one comparator becomes low-impedance: -15V at the input N402.2, $\Rightarrow < -10\text{ V}$ at P402

The signal at P402 is taken via multipoint connector X1 to optocoupler U305 on the Analog Motherbord and further to the Digital Generator, where the interrupt GENINT is accepted by the SERPA (D2A).

- Output amplifier

(OUTPUT AMPLIFIER, circuit diagram, sheets 4, 5, 6)

The two output amplifiers V1 and V2 are connected up as bridge output stage. The second amplifier inverts the signal of the first one, and the voltage **between** the two amplifiers is then applied to the output terminals as balanced signal.

V1 Inverter with switch-selectable gain (relay K302)

V1_gain 0dB or 6dB

V2 Inverter with $g = -1$

Input signal is the output signal of V1

$$V2_OUT = -V1_OUT$$

The two output amplifiers are operational amplifiers of discrete design. The inner circuits (on sheets 5 and 6) are identical.

Inner circuit: (described for V1 on sheet 5)

- Input stage V501, with emitter current source V500
- Current balancing circuit V504, 505
- Emitter follower V506 as impedance transformer
- Second voltage amplifier stage V507
- Complementary emitter followers V508, 509 drive the output stage V513, 514

- Current limiting with V510, 511, 512: $I_{max}(peak) \approx 190mA$
- Compensation: R503, C505, R521, R522, C507, C508, C513
- Output attenuator
(OUTPUT ATTENUATOR, circuit diagram sheet 7)
The two attenuators are completely identical and are switched over together. The output stage V1 supplies the upper attenuator, output SIG 3. The output stage V2 supplies the lower one, output SIG 4. Each attenuator consists of a 48-dB divider and a 12/24/36-dB ladder attenuator and can therefore be switched from 0 to 84 dB in 12-dB steps. Its source impedance can be switched between 5Ω and 15Ω .
 - Switchover of attenuation:
 - K101 switches between 0 and 48 dB
 - K102 switches between with/without ladder attenuator
 - K103,104,105 switch between 12, 24, 36dB
 - Source impedance 15Ω :
 - K106 and K107 are open
 - K101 to K105 switch the attenuator
 - Source impedance 5Ω :
 - without attenuation: K106 cuts in the 5Ω resistor
the 15Ω path is switched high-impedance
 - with attenuation: K106 is open
K101 to K105 switch the attenuator
K107 switches a load resistor to the 15Ω attenuator
⇒ Source impedance = 5Ω
⇒ **additional** attenuation: 10.2195dB
- Switchover of output
(CHANNEL 1 and 2, circuit diagram, sheets 8 and 9)
Except for bridges X800,801 and X900,901, the output stages with attenuators act like a balanced source with $2*5\Omega$ or $2*15\Omega$ source impedance. Both channels are also of symmetrical design and are completely identical except for relay K132 in channel 2, which changes the polarity of this channel.
 - Switching off the channel, switchover of Output COMTST
Output UNBAL or BAL:
The center tap is grounded via K110
K111 switches the channel to the attenuator or OFF
 - Output COMTST:
K111 is in the OFF position
K110 switches the channel on or off
 - Switching the resistor R804...R807
This switchover facility permits to match the resistance of the deactivated channel to the source impedance of the attenuator:
Channel ON: resistors are bridged by K112

Channel OFF: Attenuator $2*5\Omega$ resistors are short-circuited

$$\Rightarrow R_{off} = 2*5\Omega$$

Attenuator $2*15\Omega$ resistors are cut in

$$\Rightarrow R_{off} = 2*15\Omega$$

– Switchover of output BAL/UNBAL
with K113 and K130-A

– Cutting in various impedances

The source impedance of the attenuator is always $2*15\Omega$

Output BAL: with K114, K115 and K116

Output UNBAL: mit K117

7.3.9.2 Controlling the Analog Functions

Devices	BITS			Function
	Pos.	Count	Bitvalue	
Latch D200 K237,K236	0	2	0 1 2 3	Signal: ADDER cut in Signal: LOW DIST Signal: DAC SIG forbidden !!!
K238	2	1	1/0	HP DIFF on/off
K239	3	1	1/0	EXT SIG on/off (an external module can be connected into circuit here)
K131	4	1	1/0	COMMON ground/float
K132	5	1	1/0	INV2 on/off (inverts channel 2)
	6	2	x	not assigned
				LEVEL CONTROL
D300 Latch D301 N301	8	12	0...4095	Level_bits 0...11
	20	1	1/0	V317 off/on
	21	1	1/0	V316 off/on
	22	1	1/0	V315 off/on
	23	1	1/0	V314 off/on
				Bits 20 to 23 are the Level_Bits 12 to 15 of the 16-bit level setting
K300	24	1	1/0	N302_gain 8/0dB
K301	25	1	1/0	Adder_gain -6/0dB (only acts for DAC SIG)
K302	26	1	1/0	V1_gain 0/6dB (gain Output Amp V1)
	27	1	x	not assigned
- continued on next page -				

Devices	BITS			Function
	Pos.	Count	Bitvalue	
D400	28	12	0...4095	OFFSET DAC Offset_Dac1 (for Output Amp V1)
D401	40	12	0...4095	Offset_Dac2 (for Output Amp V2)
Latch D100				ATTENUATOR (attenuator, source impedance)
K101	52	1	1/0	atten 48dB on/off
K102	53	1	1/0	Attenuator off/on
	54	1	x	not assigned
K103	55	1	1/0	atten 12dB on/off
K104	56	1	1/0	atten 24dB on/off
K105	57	1	1/0	atten 36dB on/off
K107,106	58	2	0 1 2 3	15Ω source impedance 5Ω without attenuator 5Ω with attenuator forbidden !!!
Latch D101				COM ON/OFF BAL/UNBAL
K110	60	1	1/0	COM Chan1 off/on
K120	61	1	1/0	COM Chan2 off/on
K111	62	1	1/0	Chan1 off/on
K121	63	1	1/0	Chan2 off/on
K112	64	1	1/0	R_off Chan1 0/10Ω
K122	65	1	1/0	R_off Chan2 10Ω/0
K123,113,130	66	2	0 1 2 3	not useful, but permissible Output UNBAL Output BAL not useful, but permissible (K113, K130 driven together)
- continued on next page -				

Devices	BITS			Function
	Pos.	Count	Bitvalue	
Latch D102				R SOURCE
K124,114	68	2	0	not useful, but permissible
			1	BAL Source 10Ω/30Ω
			2	BAL Source >30Ω
			3	not useful, but permissible
K126,116 K125,115	70	4	9	BAL Impedance 200Ω
			10	BAL Impedance 600Ω
			6	BAL Impedance user all other bit combinations are not useful, but permissible
K127,117	74	2	0	not useful, but permissible
			1	R_Unbal user
			2	R_Unbal 5Ω/15Ω
			3	not useful, but permissible
D103	76	8	48H	Board identification With the \overline{RD} pulse, the BOARD ID is inserted into the data stream

The 8 bits 52 to 59 can be summed up in a superior function 'Attenuation':

Attenuation	Source: 5Ω		Source: 15Ω	
	Bit value	Latch D100	Bit value	Latch D100
0 dB	65	01000001	2	00000001
12 dB	136	10001000	8	00001000
24 dB	144	10010000	16	00010000
36 dB	160	10100000	32	00100000
48 dB	131	10000011	3	00000011
60 dB	137	10001001	9	00001001
72 dB	145	10010001	17	00010001
84 dB	161	10100001	33	00100001

7.3.9.3 Measuring Instruments

Measuring instr.	Specifications	R & S
Sinewave generator	2Hz...300kHz	AFG, AFGU or ADS
DC voltmeter	0.5%	UDS5, URE2/3 or UPD
AC voltmeter	2Hz...110kHz	URE3
Oscilloscope	—	—
Frequency counter	50ppm	UPD

7.3.9.4 Testing and Troubleshooting

1. Testing the Jumpers

X200.1 - .2
 X202.1 - .2
 X300.1 - .2
 X301.1 - .2
 X400, X401
 X402.1 - .2
 X700, X701
 X800, X801
 X900, X901

2. Testing the Operating and Reference Voltages

Test point	Nominal value	Tolerance
X100.1	+5V	± 0.15V
.2	+15V	± 0.75V
.3	-15V	± 0.75V
.4	+24V	± 1.20V
.5	-24V	± 1.20V
.6	+6V	± 0.20V
X101.1	+2.5V	± 0.25V
X101.2	+6.2V	± 0.31V

3. Testing the board identification (BOARD ID)

The byte at the parallel input of shift register D103 (coded with pull_{up} and _{down} resistors) is referred to as BOARD ID.

BOARD ID = 01001000B = 48H

The BOARD ID is inserted into the serial data stream with the \overline{RD} pulse and read in by the Digital Generator during the system start of the UPD only.

Testing see Analog Motherboard (page 7.175)

4. Testing the highpass HP DIFF

- | | | |
|-------------------|------------|-------------|
| Generator setting | Instrument | ANLG 110kHz |
| | Function | SINE |
| | Frequency | 50kHz |

- Cut in the highpass HP DIFF in service mode:
(see also controlling the analog functions)

OPTIONS Panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	OUT
	Position	2
	Count(Bit)	1
	Bitvalue	1
	Execute	YES

- Testing the frequency response
 - Measure voltage at X202 ($\approx 2.5V_{rms}$) → reference
 - Measure voltage at X300:
 - Stop band: < 1kHz, attenuation >26dB, typ. 30dB
 - Passband: 5kHz ... 110kHz, max ± 0.3 dB ripple

5. Testing the signal adder

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15 Ω
	Function	DFD
	Low Dist	ON
	Mean Freq	14.000kHz
	Diff Freq	800Hz
	Settling	PRECISION
	Total Volt	3.0000 Vpp

- Check signal at X200: Sine, 14.4kHz, $2.46V_{rms}$
- Check signal at X202: Sine, 13.6kHz, $2.46V_{rms}$
- Check signal at X300: DFD signal, $1.74V_{rms}$, $3.48V_{pk}$
- Remove jumper X200: ⇒ at X300 sine, 13.6kHz, $1.23V_{rms}$
- Remove jumper X202: ⇒ at X300 sine, 14.4kHz, $1.23V_{rms}$

6. Testing the offset DACs

- Control the offset DACs in service mode:
(see also controlling the analog functions)

OPTIONS Panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	OUT
	Position	see table
	Count(Bit)	12
	Bitvalue	see table
	Execute	YES

- Remove jumper X301 so that no AC voltage is applied to the output of the output stages which might impair the DC measurement at X700 and X701.
- Testing the offset DAC D400
Set bit value according to the table and measure voltages:

Position	Bit value	⇒ DC at P400	⇒ ΔDC at X700
28	2047	≈0V	≈0V → reference
28	0	<-10V	>+200mV
28	4095	>+10V	<-200mV

- Testing the offset DAC D401
Set bit value according to the table and measure the voltages:

Position	Bit value	⇒ DC at P401	⇒ ΔDC at X701
40	2047	≈0V	≈0V → reference
40	0	<-10V	>+200mV
40	4095	>+10V	<-200mV

7. Testing the overload detection OVERLOAD INTERRUPT

Testing using the function description, see page 7.195

8. Testing the level setting

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	1
	Output	see table
	Impedance	see table
	Function	SINE
	Low Dist	OFF
	Voltage	V_o acc. to table

- Check input signal: $V_i \approx 2.46V$ at X300

The following circuits are involved with level setting:

- LEVEL CONTROL: Fine level adjustment 0 ... -6dB, $\Delta < 0.001dB$
- Output stage V1: 0dB or +6.02dB
- Attenuator: 0 ... -84dB, $\Delta = 12dB$

The level setting depends on the generator settings Output and Impedance:

Output	Impedance	Level setting
UNBAL	15Ω, user	Table 1
BAL	30Ω, 200Ω, 600Ω, user	Table 1
COMTST	30Ω, 200Ω, 600Ω, user	like UNBAL, table 1
UNBAL	5Ω	Table 2
BAL	10Ω	Table 2
COMTST	10Ω	like UNBAL, table 2

With output COMTST the voltage V_o is applied to pin2 and pin3 of the XLR socket against ground (GEN COM).

The tables on the next two pages illustrate the relationship between the output voltage V_o of the generator and the associated level setting boards. The settings of LEVEL CONTROL and output stage V1 are repeated with all attenuator settings. Therefore, they are only indicated in detail for the 12-dB setting; for the other settings, only the thresholds of the attenuator are indicated.

9. Testing the Output Switching

Testing by way of the function description, see page 7.196

Level table for generator output: UNBAL 15Ω and BAL 30Ω						
LEVEL CONTROL		Output stage V1		Attenuator	Generator Output	
V ₁ /dB	Voltage at X301	V ₂ /dB	Voltage at X402		UNBAL 15Ω V _o	BAL 30Ω V _o
7.747	6.00V	6.02	12.00V	0dB	12.00V	24.00V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0.133	2.500V	6.02	5.00V	0dB	5.00V	10.00V
0.1	2.495V	6.02	4.99V	0dB	4.99V	9.98V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
-5.88	1.25V	6.02	2.50V	⋮	2.50V	5.00V
0.1	2.49V	0	2.49V	⋮	2.49V	4.98V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
-5.82	1.26V	0	1.26V	0dB	1.26V	2.52V
0.1	2.49V	6.02	4.98V	12dB	1.25V	2.50V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
-5.88	1.25V	6.02	2.50V	⋮	628mV	1.26V
0.133	2.50V	0	2.50V	⋮	627mV	1.25V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
-5.82	1.26V	0	1.26V	12dB	316mV	632mV
0.1	2.49V	6.02	4.98V	24dB	315mV	630mV
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	24dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	79.25mV	158.5mV
⋮	⋮	⋮	⋮	36dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	19.90mV	39.8mV
⋮	⋮	⋮	⋮	48dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	5.00mV	10.0mV
⋮	⋮	⋮	⋮	60dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	1.26mV	2.52mV
⋮	⋮	⋮	⋮	72dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	316μV	632μV
⋮	⋮	⋮	⋮	84dB	⋮	⋮
V ₁ = X301/X300						
V ₂ = X402/X301 = V1_gain						
With voltages >2.5V at X301, an additional gain of 7.722 dB is cut in for N302 by means of relay K300						

Level table for generator output: UNBAL 5Ω and BAL 10Ω						
LEVEL CONTROL		Output stage V1		Attenuator	Generator Output	
V ₁ /dB	Voltage at X301	V ₂ /dB	Voltage at X402		UNBAL 5Ω V _o /V	BAL 10Ω V _o /V
7.747	6.00V	6.02	12.00V	0dB	12.00V	24.00V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0.133	2.500V	6.02	5.00V	0dB	5.00V	10.00V
0.1	2.495V	6.02	4.99V	0dB	4.99V	9.98V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
-5.88	1.25V	6.02	2.50V	⋮	2.50V	5.00V
0.1	2.49V	0	2.49V	⋮	2.49V	4.98V
⋮	⋮	⋮	⋮	⋮	⋮	⋮
-16.00	388mV	0	388mV	0dB	388mV	776mV
0.1	2.49V	6.02	4.98V	12dB	387mV	774mV
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
-5.82	1.26V	0	1.26V	12dB	97.2mV	194.4mV
⋮	⋮	⋮	⋮	↓	97.0mV	194.0mV
⋮	⋮	⋮	⋮	24dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	24.4mV	48.8mV
⋮	⋮	⋮	⋮	36dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	6.14mV	12.28mV
⋮	⋮	⋮	⋮	48dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	1.54mV	3.08mV
⋮	⋮	⋮	⋮	60dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	387μV	774μV
⋮	⋮	⋮	⋮	72dB	⋮	⋮
⋮	⋮	⋮	⋮	↓	97.2μV	194.4μV
⋮	⋮	⋮	⋮	84dB	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
V ₁ = X301/X300						
V ₂ = X402/X301 = V1_gain						
With voltages >2.5V at X301, and additional gain of 7.722 dB is cut in for N302 by means of relay K300.						
Except for the 0-dB setting of the attenuation, an additional attenuation of 10.22 dB is always active						

7.3.9.5 External Interfaces

Motherboard connector X1						
name	Signal description	=	source dest.	range	connector	comment
Input signals						
LOW DIST		I	LowDist	2.85V ... 0.25V 10Hz ... 110kHz Sine	X1.A31	
DAC SIG		I	DacBoard	2.50V ... 0.25V 2Hz ... 110kHz	X1.C31	
Output signals, value range see data sheet						
BAL 1-2	Channel 1	O	Front panel		X1.C10	XLR, pin2
BAL 1-3	Bal (XLR)	O	Front panel		X1.A10	XLR, pin3
BAL 2-2	Channel 2	O	Front panel		X1.C2	XLR, pin2
BAL 2-3	Bal (XLR)	O	Front panel		X1.A2	XLR, pin3
UNBAL 1 HI	Channel 1	O	Front panel		X1.A8	Inner conductor
UNBAL 1 LO	Unbal (BNC)	O	Front panel		X1.C8	Outer conductor
UNBAL 2 HI	Channel 2	O	Front panel		X1.A4	Inner conductor
UNBAL 2 LO	Unbal (BNC)	O	Front panel		X1.C4	Outer conductor
Serial data interface DATA LINK						
CLK.	Clock	I	DigGen	TTL, 1 ... 3 MHz	X1.A25	
SDI	Data in	I	DacBoard	TTL	X1.C25	
SDO	Data out	O	X23/Mux	HCMOS	X1.A23	
/WR.	Write Data	I	DigGen	TTL	X1.C24	
/RD.	Read (Board ID)	I	DigGen	TTL	X1.A24	
ENABLE		I	MothBoard	TTL	X1.C23	
External signal, not used						
EXT OUT		O	MothB X23	2.5V / 2Hz...110kHz	X1.C28	
EXT IN		I	MothB X23	2.5V / 2Hz...110kHz	X1.A28	
Overload Interrupt						
INT		O	DigGen	> +10V < -10V	X1.A22	no interrupt Interrupt
Operating voltages						
-24V		I		-24±1.2V < 250mA	X1.A.C14	
+24V		I		-24±1.2V < 250mA	X1.A.C15	
-15V		I		-15±0.75V < 80mA	X1.A.C17	
+15V		I		15±0.75V < 80mA	X1.A.C18	
+6V		I		6±0.2V < 700mA	X1.A.C20	
+5V		I		5±0.15V < 40mA	X1.A.C21	
Ground	floating				X1.A.C 1,3,5,7,9,11, 12,13,16 X1.A.C 19,26,27,29,30, 32 X1.C 22	
Ground	Chassis				X1.A.C 6	
Explanation: =: I:Input, O:Output, B:Bidirectional, P:Power						

7.3.10 Low Distortion Generator

Circuit diagram	1031.2699.01 S
Component location plan	1030.2699
Parts list	1030.2699.01 SA

7.3.10.1 Function

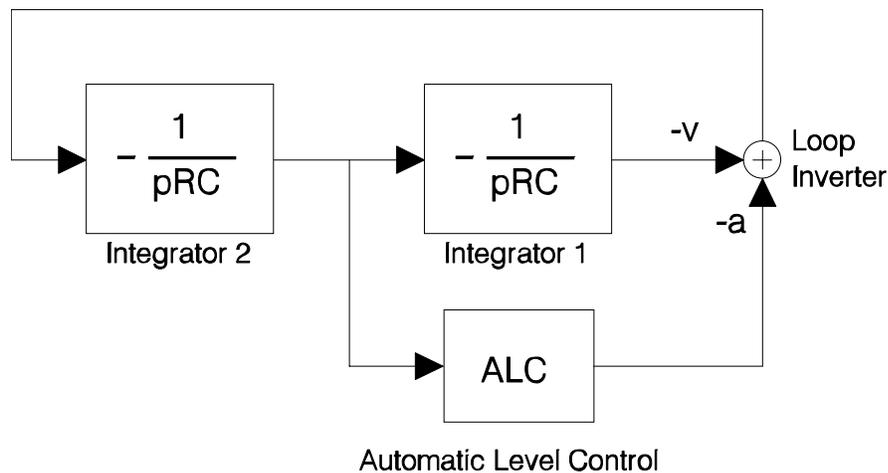
- Oscillator

(Circuit diagram, sheets 3, 4, 5)

- Sheet3: Integrator 1 (N32 with circuitry)
Limiting circuit (V314, V315, V316)
Controlling the decade-C switchover (D31, N33)
Loop inverter (N34)
12-bit frequency fine tuning (D32, N35)
- Sheet4: Integrator 2
- Sheet5: LEVEL CONTROL (ALC)

The oscillator operates according to the principle of the state-variable oscillator:

Two integrators (INTEGRATOR 1 and 2) are connected in series and are fed back via an inverter (LOOP INVERTER):



When determining the system function of this circuit, the following equation is obtained:

$$1 - \frac{a}{pRC} + \frac{g}{(pRC)^2} = 0$$

where $p = \sigma + j\omega$ is the complex frequency

$a = 0$ results in:

$$p^2 = -\frac{g}{(RC)^2}$$

With $p = j\omega = j2\pi f$ the following frequency f is obtained:

$$f = \frac{\sqrt{g}}{2\pi RC}$$

The oscillation frequency f of the oscillator is thus set by the time constant $1/RC$ of the integrators and the gain g of the inverter. The condition $a = 0$ for a stable oscillation is produced by the level control.

For frequency setting, two settling modes are provided in the generator panel:

Settling	g	Frequency accuracy
FAST	0.98	The tolerance of $C(\pm 1\%)$ is eliminated by calibration. The tolerance of R of typ. $\pm 0.1\%$ is left.
PRECISION	0.96 ... 1.00	The frequency is first set like Settling FAST, measured internally and reset to an accuracy of better than $\pm 0.1\%$ using the frequency fine tuning circuit.

In Settling Mode FAST, the following applies to the oscillation frequency f :

$$f = \frac{\sqrt{g}}{2\pi RC} \quad \text{with} \quad \sqrt{v} = \sqrt{0.98} = 0.99$$

with	in integrator 1	in integrator 2
R	R300 ... R305 D30, N30, R306 ... R309	R400 ... R405 D40, N40, R406 ... R409
C	C302 ... C305	C402 ... C405

The capacitors C are switched in decades with Frq_range

Frq_range		C / nF	Frequency range
binary	decimal		
000	0	0.56	110kHz ... 22kHz
001	1	2.76	22kHz ... 1.8kHz
010	2	33.56	1.8kHz ... 185Hz
100	4	330.56	185Hz ... 10Hz

The resistor R is set with Frq_Bits (0 ... 65535): minimally 2.5kΩ, 16-bit resolution.

$$R = 2500 * \frac{65535}{65535 - Frq_Bits} \Omega$$

Thus, the following relationship exists between the frequency f, C and Frq_Bits:
(with f in Hz, C in F)

$$f = \frac{65535 - Frq_Bits}{2\pi * C * 2500 * 65535} * 0.99$$

or

$$Frq_Bits = 65535 * \left(1 - \frac{2\pi f * C * 2500}{0.99}\right)$$

Example: f=1kHz \Rightarrow Frq_range = 010 \Rightarrow C = 33.56nF
Frq_Bits = 30638.66 = 77AFH

- Frequency fine tuning

(FRQ FINE TUNE, circuit diagram sheet3)

The oscillation frequency f of the oscillator is given by: $f = \frac{1}{2\pi RC} * \sqrt{g}$

The dependence of oscillation frequency f of the gain g of the inverters is used for frequency fine tuning in settling mode PRECISION:

The circuit with D32 and N35 is a multiplying D/A converter with 12-bit resolution. The 12 bits of the DAC (D32) are referred to as Frq_fine_tune: Frq_fine_tune = 0...FFFH (0...4095).

Input voltage V_i at P31, D32.15

Output voltage V_o at P32, N35.6

The following applies to the voltage at the output of opamp N35:

$$V_o = V_i * Frq_fine_tune / 4096 \quad \text{with} \quad Frq_fine_tune = 0 \dots 4095$$

The output voltage V_o of N35 is applied via R343 to the LOOP INVERTER, varying its gain g:

Frq_fine_tune	V_o/V_i	gain g	Frequency variation
0	0	1	+1%
2047	0.5	0.98	0
4095	1	0.96	-1%

Frequency variation referred to g = 0.98 (Settling FAST)

- Level control

(LEVEL CONTROL (ALC), circuit diagram sheet 5)

The output signal COS of the oscillator is set to a constant amplitude of $\approx 3.8V$ ($\approx 2.7V_{rms}$). The level reference is generated with zener diode V500 and applied to amplifier N51.

The signal SIN is the input voltage of integrator 1, the signal COS is its output voltage. Therefore, there is a phase difference of 90° between the two signals.

The inverting comparator N52 changes the SIN signal to a squarewave signal: the rising edge is exactly in the maximum, the falling edge is exactly in the minimum of the COS signal.

This signal configuration is used to measure the amplitude of the COS signal in a two-stage track&hold circuit (V504, N53 and V510, N55).

The time constant of control integrator N54 is matched to the signal frequency using the FET V512, which is switched synchronously with the track&hold amplifier 2:

⇒ Transient response independent of frequency

For noise suppression, the FETs V502 and V503 switch the bandwidth of the track&hold amplifier 1:

Frequency	FETs V502 and V503	Bandwidth (3dB)
> 22kHz	both cut in	$\approx 2.5\text{MHz}$ (1nF·60Ω)
< 22kHz	V502 off, V503 on	$\approx 600\text{kHz}$ (1nF·274Ω)
< 1.8kHz	both off	$\approx 90\text{kHz}$ (1nF·1.8kΩ)

- IMD level setting

(IMD ATTEN, circuit diagram sheet 2)

This circuit is only used if the generator generates a two-tone signal (DFD, MODDIST or DIM) and the Low Distortion Generator is activated.

The circuit with D22 and N20 is a multiplying D/A converter with 12-bit resolution. The 12 bits of the DAC (D22) are referred to as IMD_gain: $IMD_gain = 0\dots\text{FFFH}$ (0...4095).

Input voltage V_i at X2, D22.15 (=output signal COS of oscillator)

Output voltage V_o at P21, N20.6

The following applies to the voltage at the output of opamp N20:

$$V_o = V_i * IMD_gain / 4096 \quad \text{with} \quad IMD_gain = 0 \dots 4095$$

7.3.10.2 Controlling the Analog Functions

Devices	BITS			Function
	Pos.	Count	Bitvalue	
Latch D21 K2	0	1	1/0	IMD ATTEN on/off
	1	1	x	not assigned
	2	1	1/0	V503 off/on
	3	1	1/0	V502 off/on
	4	4	x	not assigned
D30, D40 Latch D31, 41 N31, N41	8	12	0...4095	FREQUENCY CONTROL Frq_Bits 0...11
	20	1	1/0	V307, V407 off/on
	21	1	1/0	V306, V406 off/on
	22	1	1/0	V305, V405 off/on
	23	1	1/0	V304, V404 off/on
				Bits 20 to 23 are the bits 12 to 15 of the total of 16 Frq_Bits
	N33	24	3	0
1				Frq_range \leq 22kHz
2				Frq_range \leq 1.85kHz
			4	Frq_range \leq 185Hz
	27	1	x	not assigned
D32	28	12	0...4095	Frq_fine_tune (2047 für Settling FAST)
D22	40	12	0...4095	IMD_gain
D23 D23	52	8	58H	Board identification BOARD ID is inserted into the data stream with the \overline{RD} pulse

7.3.10.3 Measuring Instruments

Measuring instr.	Specifications	R&S
DC voltmeter	0.5%	UDS5, URE2/3 or UPD
AC voltmeter	10Hz ... 110kHz	URE2/3
Sinewave generator	2 channels Phase settable	ADS
Oscilloscope	Digital storage 4 channels, 100MHz	—
Frequency counter	50ppm	UPD

7.3.10.4 Testing and Troubleshooting

1. Testing the Jumpers

- X2.1 - .2
- X50.1 - .2
- X51.1 - .2
- X52.1 - .2

2. Testing the Operating Voltages

Test point	Nom. value	Tolerance
X1.1	+5V	$\pm 0.15V$
.2	+15V	$\pm 0.75V$
.3	-15V	$\pm 0.75V$
.4	-24V	$\pm 1.20V$
.5	+6V	$\pm 0.20V$
P20	+2.5V	$\pm 0.25V$
P55	-6.2V	$\pm 0.31V$

3. Testing the board identification (BOARD ID)

The byte at the parallel input of shift register D23 (coded with pull_up and _down resistors) is referred to as BOARD ID.

BOARD ID = 01011000B = 58H

The BOARD ID is inserted into the serial data stream with the \overline{RD} pulse and read in by the Digital Generator during the system start of the UPD only.

Testing see Analog Motherboard (page 7.175)

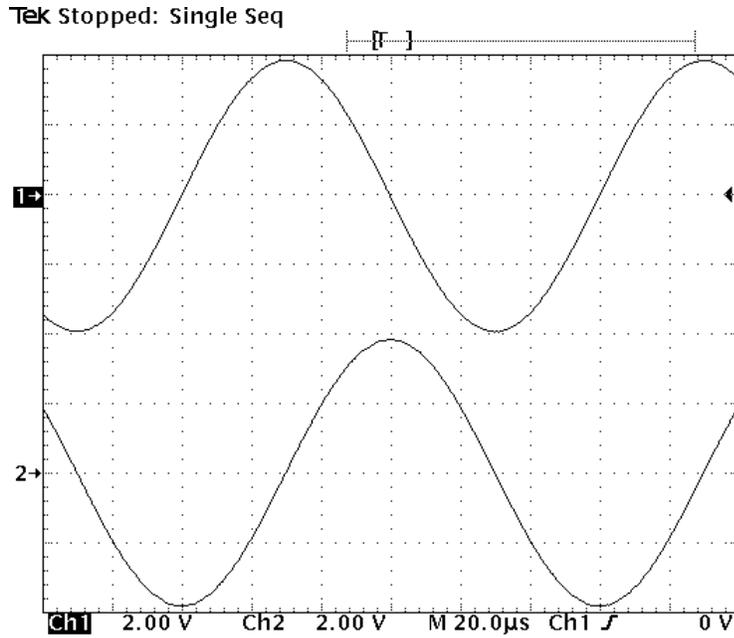
4. Testing the level control

If the oscillator oscillates and provides a sinewave signal with a constant amplitude of $\approx 3.8V$ over the entire frequency range, the level control also works properly and need not be checked. If the oscillator does not oscillate, the level control does not function either.

For testing the level control in this case, two external signals with a phase shift of 90° must be fed in instead of the oscillator signals:

at X51.2 : Sine, 2kHz, $2.7V_{rms}$ (sine)

at X50.2 : Sine, 2kHz, $\approx 2.7V_{rms}$, leading by 90° (cosine)



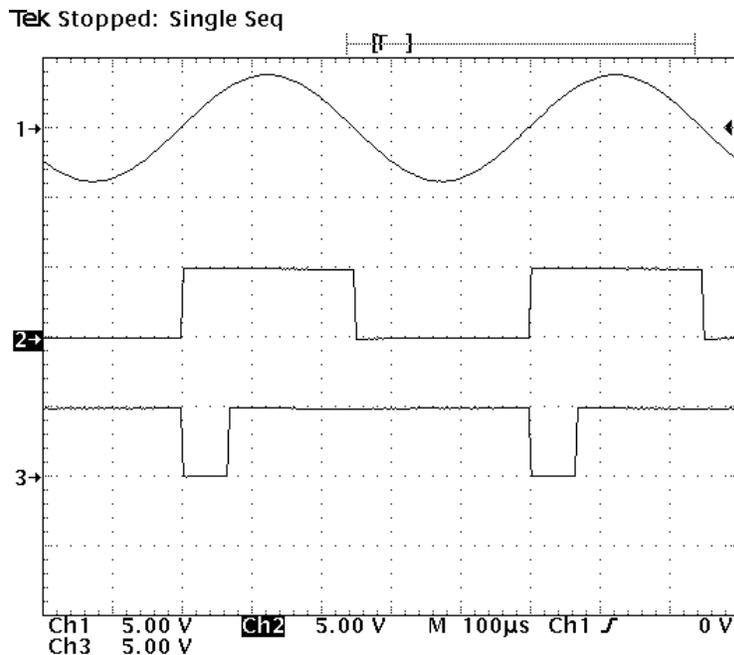
Trace1: X50.2 COS

Trace2: X51.2 SIN

The amplitude of the signal at X50 must be adjusted such that the minimum of the sinusoidal-like output signal of N51 (see illustration after next, trace 2) exactly coincides with 0!

- Testing the track&hold circuit

The comparator N52 and the gate D50 generate the control signals for the track&hold circuits from the sinewave signal at X51.



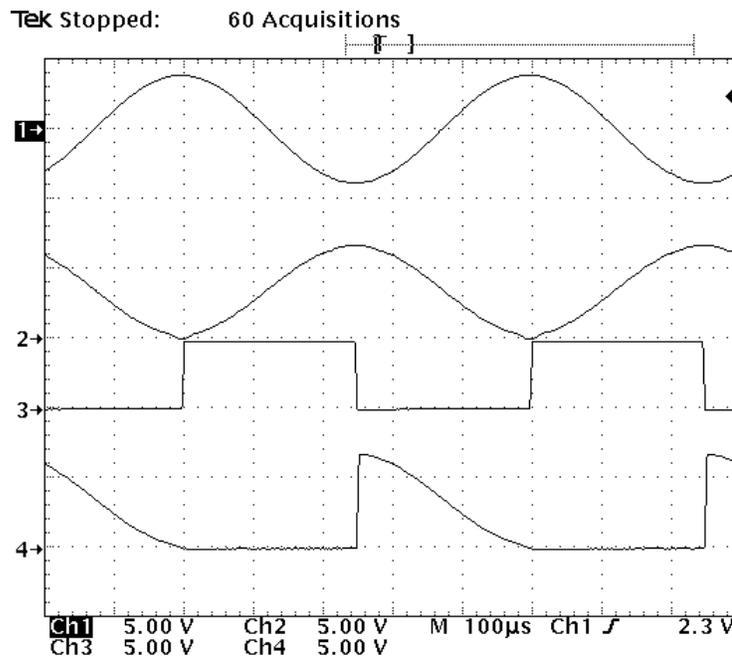
- Trace1: Sinewave signal SIN at X51
- Trace2: P57, control signal for track&hold amplifier 1 (V504, N53)
- Trace3: P54, control signal for track&hold amplifier 2 (V510, N55)

For driving the switching FETs, the output signals of D50 must also pass the level conversion stages with V505, V507 and V506, V508:

P57, P54	Switching FETs V504, V510	T&H circuit
1	-15V ⇒ off	Hold
0	≈0V ⇒ on	Track

The track&hold amplifier 1 switches from track to hold mode exactly when the output signal of N51 reaches its minimum. About 2μs later, the track&hold amplifier 2 switches to track for ≈ 65μs and holds the signal for the remaining signal period. When the signal frequency becomes $f > 1/(2 * 65\mu s) \approx 7.6\text{kHz}$ the two track&hold amplifiers operate alternately: the second T&H amplifier follows the signal during the hold phase of the first one and switches back to hold mode shortly before beginning of the track phase of the first one.

The next illustration shows the signals in the track&hold circuit



- Trace1: input signal COS at X50
- Trace2: N51.6
- Trace3: P57, control signal for track&hold amplifier 1
- Trace4: P56, output signal track&hold amplifier 1

The output signal of the track&hold amplifier 2 at P53 must feature a DC voltage of ≈0V.

- Testing control element D51

D51 is an analog multiplier that multiplies the sinewave signal at pin12 ($\approx 250mV_{rms}$) with the DC output voltage of the control integrator N54 at pin8 and the proportional component at pin4.

The two output signals at D51.2 and .14 are amplified in N56 and applied via R536 to the LOOP INVERTER N34 (circuit diagram sheet 3).

In the steady state, the proportional component is 0 V, the integral-action component lies between -1 V und $+1$ V depending on the frequency.

The control voltage at X52 lies between 3 mV and 100 mV depending on the frequency.

Operating points	pin	DC voltage
	D51.1	7.5V
	D51.3	-13V
	D51.13	-13V
	D51.2	+9.6V
	D51.14	+9.6V
Tolerance $\pm 10\%$		

Equation of multiplication:

$$\Delta V_o \approx 0.8V^{-1} * V_{AC} * \Delta V_{DC}$$

with V_{AC} AC voltage at D51.12 ($\approx 250mV_{rms}$)

ΔV_{DC} DC voltage variation between D51.8 and .4

ΔV_o AC voltage variation at X52

Since the (unknown) DC offset of the multiplier also has an effect on the multiplication characteristic, only the voltage changes may be considered in the evaluation of the above equation!

5. Testing the oscillator

All settings are made in the service mode:

OPTIONS Panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	Low Dist
	Position	see below
	Count(Bit)	see below
	Bitvalue	see below
	Execute	YES

- Formula for the oscillator frequency (uncalibrated, settling FAST)

$$f = \frac{1}{2\pi RC} * 0.99$$

- Testing the frequency setting

– Set Position 24, Count(Bit) 3, Bitvalue 0

⇒ Frequency range 22kHz ... 110kHz, C = 560pF

The FETs V308, 309, 310 and V408, 409, 410 are reverse-biased

- Set Position 8, Count(Bit) 12, Bitvalue 4095
Measure voltage at P33 and P43: $AC \approx 2.7V_{rms}$
- Testing the FETs V304...V307 and V404...V407
Set Position 20, Count(Bit) 4, Bitvalue according to the table and measure the frequency:

Bitvalue		N31, N41 pins				FETs on	$\Rightarrow R$	Frequency
dez	bin	13	14	1	2			
7	0111	0V	-15V	-15V	-15V	V304, V404	5k Ω	56.28kHz
11	1011	-15V	0V	-15V	-15V	V305, V405	10k Ω	28.14kHz
13	1101	-15V	-15V	0V	-15V	V306, V406	20k Ω	14.07kHz
14	1110	-15V	-15V	-15V	0V	V307, V407	40k Ω	7.035kHz
Frequency error max. $\pm 1.2\%$								

If a frequency is out of tolerance, this may be due to resistor R or the associated FETs. Normally, the ON resistors of the FETs are $< 0.1\%$ of the resistors they switch – and can therefore be neglected. If all frequencies are out of tolerance in the same direction, the fault lies in the capacitor.

- Testing the DACs D30, D40
Set Position 20, Count(Bit) 4, Bitvalue 14
Measure voltage at P30 and P40: $V_i (\approx 2.7V_{rms})$
Set Position 8, Count(Bit) 12, Bitvalue according to the table, measure voltage and frequency:

Bitvalue	P33/ V_{ie}	P43/ V_i	Frequency
4095	1	1	7.035kHz
2047	0.5	0.5	10.658kHz
0	0	0	14.07kHz

- Testing the frequency range switching

- Set frequency:
Set Position 8, Count(Bit) 12, Bitvalue 4095
 \Rightarrow Voltage at P33 and P40: $AC \approx 2.7V_{rms}$
Set Position 20, Count(Bit) 4, Bitvalue 7
 $\Rightarrow R = 5k\Omega$
- Set Position 24, Count(Bit) 3, Bitvalue according to the table and measure frequency:

Bitvalue		N33 pin			Frequency range	C / nF	Frequency
dec	bin	13	14	1			
0	000	-24V	-24V	-24V	110kHz ... 22kHz	0.56	56.28kHz
1	001	-24V	-24V	0V	22kHz ... 1.8kHz	2.76	11.42kHz
2	010	-24V	0V	-24V	1.8kHz ... 185Hz	33.56	939Hz
4	100	0V	-24V	-24V	185Hz ... 10Hz	330.56	95.3Hz
Frequency error max. $\pm 1.2\%$							

The FETs V308, 309, 310 in integrator 1 and the FETs V408, 409, 410 in integrator 2 are commonly driven by N33. The FETs are activated with $\approx 0V$ applied to the gate and are reverse-biased with $\approx -24V$.

If a frequency is out of tolerance, this is due to the associated capacitor C. If all frequencies are out of tolerance in the same direction, resistor R (R300, R301 and

V304 in integrator 1 as well as R400, R401 and V404 in integrator 2) should be checked using an ohmmeter.

6. Testing the frequency fine tuning

CAUTION: The adjustment range of the frequency fine tuning is only $\pm 1\%$. This corresponds to the maximum tolerance for the frequency if the frequency accuracy is not calibrated. Therefore, the PRECISION mode only works properly if the frequency accuracy of the Low Dist Generator is calibrated.
 \Rightarrow first check the calibration factors CF_ldg_frq[...]
 (see also section Adjustment and Calibration, page 7.118)

Generator setting	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15 Ω
	Function	SINE
	Low Dist	ON
	Frequency	1.000kHz
	Settling	FAST
	Voltage	1.000V

OPTIONS panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	LDG
	Position	28
	Count(Bit)	12
	Bitvalue	2047
	Execute	YES

Measure frequency at P21, X1.A16 or at output (BNC connector)

Measure AC at P32

Set bit value: Check frequency at P21, voltage at P32

Bitvalue = 2047: Measure frequency ($\approx 1\text{kHz}$) \rightarrow reference
 at P32 $\approx 1.35V_{rms}$

Bitvalue = 0000: Frequency change $> +0.8\%$ (*typ* + 1.0%)
 at P32 0V

Bitvalue = 4095: Frequency change $< -0.8\%$ (*typ* - 1.0%)
 at P32 $\approx 2.70V_{rms}$

If the frequency fine tuning functions properly, but the frequency is not correctly set in the settling mode PRECISION, the signal LDFREQ should be checked:

TTL signal with the frequency of the Low Dist Generator:

- from D50.8

- via the optocoupler U300 (on the Analog Motherboard)
- as far as to frequency counter PFC D40.5 (on the Digital Analyzer)

7. Testing the intermodulation level setting IMD ATTEN

- Generator setting

Generator Panel	Instrument	ANLG 110kHz
	Channel(s)	1
	Output	UNBAL
	Impedance	15Ω
	Function	DFD
	Low Dist	ON
	Mean Freq	5.000kHz
	Diff Freq	500Hz
	Total Volt	1.000V

OPTIONS panel	SERVICE	password ok
	Diag State	ON
	DAC VoltAC	0.955
	DAC VoltDC	0
	Enable Bit	ON
	AGEN Board	LDG
	Position	40
	Count(Bit)	12
	Bitvalue	4095
	Execute	YES

- Testing the accuracy:

Measure AC at P21 ($\approx 2.7V_{rms}$) → reference

Set bit value according to the table and check the voltage at P21:

Bitvalue	$\Rightarrow V_{P21}/reference$
4095	1.0
3072	0.75
2047	0.5
512	0.125
410	0.1

permissible tolerance: $\pm 2\%$

- Testing the frequency response:

Set the bit value, e.g. according to the above table

Vary Mean Freq from 5 kHz to 100 kHz

Measure AC at P21

Permissible tolerance: $\pm 2\%$, reference is the voltage at Mean Freq = 5kHz

CAUTION: For this measurement, the frequency response of the Low Distortion Generator must be adjusted.

7.3.10.5 External Interfaces

Motherboard connector X1						
name	Signal description	≡	source dest.	range	connector	comment
Output signals						
LOW DIST	Sine output	O	OutCirc	2.85V ... 0.25V 10Hz ... 110kHz	X1.A16	
LDFREQ		O	DigAna	Sinus 10Hz ... 110kHz L: 3 ... 8mA H: 0 ... 0.5mA (voltage ≈ 3.6V)	X1.A1	
Serial data interface DATA LINK						
CLK.	Clock		DigGen	TTL, 1 ... 3 MHz	X1.A6	
SDI	Data in		Mux X23	TTL	X1.C6	
SDO	Data out	O	Mux X26	HCMOS	X1.A4	
/WR.	Write Data		DigGen	TTL	X1.C5	
/RD.	Read (Board ID)		DigGen	TTL	X1.A5	
ENABLE			MothBoard	TTL	X1.C4	
+5V(OPT)	to Data Mux X26	O		5±0.15V	X1.A7	
Operating voltages						
-24V				-24±1.2V < 15mA	X1.A.C8	
-15V				-15±0.75V < 150mA	X1.A.C9	
+15V				15±0.75V < 100mA	X1.A.C10	
+6V				6±0.2V < 35mA	X1.A.C11	
+5V				5±0.15V < 10mA	X1.A.C12	
Ground	floating				X1.C 1,7,16 X1.A.C 2,3,13,14,15	
Explanation: ≡: :Input, O:Output, B:Bidirectional, P:Power						

7.4 Digital Boards DSP

7.4.1 Testing the Rated Specifications

7.4.1.1 Digital Analyzer

Most test functions of the UPD are implemented by means of a digital signal processor (DSP) on a plug-in card in the PC installed in the instrument. This signal processor as well as the associated memory are automatically tested when the instrument is switched on. Proper functioning of the interfaces (parallel, serial) is to be checked manually. Since the test functions are implemented by the software, a checksum of the software is tested when switching on.

1. General function test

Test setup: Connect UPD analyzer internally to UPD generator in digital operation.

Setting: Instrument DIG48, input and output INTERNAL each, single-channel, the sampling rate being fixed.

Measurements:

- FFT and sine test:
 - Generator: Function = Sine, Frequency = 997Hz, Voltage = 0.9FS, no dither;
 - Analyzer: Function = FFT, FFT-Size = 8192, ZOOM = OFF, Window = RIFE VINC 3.
 - Nom. result: FFT display, all spurious < -130dB, frequency readout 997.0 Hz; input peak = 0.9FSpk
- ZOOM FFT:
 - Generator: Function = Sine, Frequency = 997Hz, Voltage = 0.9FS, no dither;
 - Analyzer: Function = FFT, FFT-Size = 8192, ZOOM ON, Center 500Hz, Span 1000Hz, Window KAISER, $\beta=16$.
 - Nom. result: FFT display, all spurious < -130dB, frequency readout 997.0 Hz;
- THD:
 - Generator: Sine, 997Hz, 0.9FS, no dither;
 - Analyzer: Function = THD, Unit = dB, Mode = Auto.
 - Nom result: readout < -130dB, frequency readout 997.0 Hz;
- RMS:
 - Generator: Function = Sine, 997Hz, 0.9FS, no dither;
 - Analyzer: Function = RMS, Unit = FSpk, Mode = Auto.
 - Nom. result: readout = 0.9FS = 0.6363FSpk, frequency readout 997.0 Hz;
- PEAK:
 - Generator: Function = Sine, 997Hz, 0.9FS, no dither;
 - Analyzer: Function = PEAK, Unit = FSpk, Mode = Auto.
 - Nom. result: readout = 0.9FSpk, frequency readout not avail.

2. Testing the serial interface

- **Function test:**
 - Test setup:** Connect UPD analyzer via a 15-contact DSUB connection to its own generator or a second UPD. For this purpose, use a cable where the lines SCLKA (=Pin 9), SDATAA (=Pin 10), SWSA (=Pin 11) (channel A), SCLKB (=Pin 15), SDATAB (=Pin 14), SWSB (=Pin 13) (channel B) and 7 and 8 (GND) are through-connected (included in service kit).
 - Settings:** Instrument: DIG48, Channel: 1, Input: SERIAL, Wrd Lngth: 32, FUNCTION: FFT, Size: 8192, Window: RIFE VINC 3
 - Measure:** Set 997 Hz, 0.9 FS on generator, measure using FFT. Spurious in the FFT smaller than -130 dB. Repeat measurement with channel 2.
- **Output clock (Word clock):**
 - Test setup:** Connect frequency counter to serial interface, pin 5 (SWSOUT)
 - Settings:** Instrument: DIG48, Channel: 1, Input: SERIAL, Wrd Lngth: 32
 - Measure:** Set Samplefrq = 32000, 44100, 48000 Hz one after the other on the analyzer, check using frequency counter. Permissible tolerance: 50ppm
- **Output clock (bit clock):**
 - Test setup:** Connect frequency counter to serial interface, pin 4 (ACLKOUT)
 - Setting:** Instrument: DIG48, Channel: 1, Input: SERIAL, Wrd Lngth: 32, Sample Frq: 48000Hz
 - Measure:** Check bit clock using frequency counter. Nom. value: $32 * 48000\text{Hz} = 1536 \text{ kHz}$, permissible tolerance: 50ppm
- **Testing the Framesync position and polarity**
 - Test setup:** Connect logic generator to serial input.
 - Settings:** Instrument: DIG48, Channel: 1, Input: SERIAL, Wrd Lngth: 32, Bit Order: MSB-first, Data Format: 2's Compl., Sample Frq: 48000, Function: RMS, Mode: FAST
 - Measure:** Set a bit pattern according to Fig. 2-22 in section 2.6.3. of the operating manual (configuration of digital interfaces) on the logic generator. Data bits: $00111..11 = 0.5 * \text{greatest possible number}$. With correct setting of the word offset, an input peak of 0.5 FS and an RMS value of 0.707 FS is measured. Repeat the measurement with all Framesync positions.

3. Testing the parallel interface

- **Function test:**
 - Test setup:** Connect UPD analyzer via 37-contact DSUB connection (all lines (except pin 17=OUT5V) through-connected, included in service kit) to its own generator or a second UPD.
 - Settings:** Instrument: DIG48, Channel: 1, Input: Parallel, FUNCTION: FFT, Size: 8192, Window: Hanning
 - Measure:** Set 997 Hz, 0.9 FS on the generator, measure with FFT. Spurious in the FFT smaller than -130 dB. Repeat the measurement with channel 2 with the option UPD-B3 (Highspeed) installed.

- Output clock (word clock):
 - Test setup: Connect frequency counter to parallel interface. (Pin 37, line PWSOUT)
 - Settings: Instrument: DIG48, Channel: 1, Input: PARALLEL
 - Measure: Set Samplefrq = 32000, 44100, 48000 Hz one after the other on the analyzer, check using frequency counter. Tolerance: 50ppm
- Output clock (bit clock):
 - Test setup: Connect frequency counter to parallel interface, pin 36 (PCLKOUT)
 - Settings: Instrument: DIG48, Channel: 1, Input: PARALLEL, Sample Frq: 48000Hz
 - Measure: Check bit clock using frequency counter. Nom. value: $32 * 48000\text{Hz} = 1536 \text{ kHz}$, Tolerance: 50ppm

4. Testing the internal interfaces

The interfaces to the internal analog hardware are implicitly checked when testing the analog boards.

7.4.1.2 Digital Generator

All signal generators in the UPD (exception: Option UPD-B1, Low Distortion Gen) are implemented by means of a digital signal processor (DSP) on a plug-in card in the PC installed in the instrument. This signal processor as well as the associated memory are automatically checked when the instrument is switched on. Proper functioning of the interfaces (parallel, serial) is to be checked manually. Since the test functions are implemented by the software, a checksum of the software is tested when switching on.

1. General function test

Test setup: Connect UPD analyzer internally to UPD generator in digital operation.

Setting: Instrument DIG48, Input and output INTERNAL each, single-channel, the sampling rate is fixed.

Measurements:

- Sine:
 - Generator: Function = Sine, Frequency = 997Hz, 0.9FS, no dither;
 - Analyzer: Function = FFT, FFT-Size = 8192 dots, ZOOM OFF, Window = RIFE VINC 3.
 - Nom. result: Indication of a single line at 997Hz, all spurious < -130dB, Frequency readout 997.0 Hz;
- MODDIST:
 - Generator: Function = MODDIST, Voltage Peak = 0.9FS, no dither;
 - Analyzer: Function = FFT, FFT-Size = 8192 dots, ZOOM OFF, Window = RIFE VINC 3.
 - Nom. result: Indication of the two generator lines in the correct amplitude ratio, frequency indication of the higher line. Spurious < -130dB.
- DFD:
 - Generator: Function = DFD, Center = 11kHz, Delta = 997Hz, 0.9FS, no dither;
 - Analyzer: Function = DFD, Unit = dB, Mode = Auto.
 - Nom. result: Readout (both for d2 and d3 measurement) < -130dB;

2. Testing the serial interface

- Function test:
 - Test setup: Connect UPD generator via 15-contact DSUB connection (lines 9, 10, 11 (channel A), 13, 14, 15 (channel B) as well as 7 and 8 (GND) through-connected) to its own analyzer or a second UPD (included in service kit).
 - Settings: Analyzer: Instrument: DIG48, Channel: 1, Input: SERIAL, Wrd lngth: 32, FUNCTION: FFT, Size: 8192, Window: Hanning
 - Measure: Set 997 Hz, 0.9 FS on generator, measure with FFT. Spurious in the FFT < -130 dB. Repeat measurement with channel 2.
- Output clock (word clock):
 - Test setup: Connect frequency counter to serial interface, pin 11 (SWSA).
 - Settings: Instrument: DIG48, Channel: 1, Output: SERIAL, Wrd lngth: 32
 - Measure: Set Samplefrq = 32000, 44100, 48000 Hz one after the other on the generator, check using the frequency counter. Tolerance: 50ppm

- Output clock (bit clock):
 - Test setup: Connect frequency counter to serial interface, pin 9 (SCLK).
 - Settings: Instrument: DIG48, Channel: 1, Output: SERIAL, Wrd lngth: 32, Sample Frq: 48000 Hz
 - Measure: check bit clock using frequency counter. Nom. value: $32 * 48000\text{Hz} = 1536 \text{ kHz}$, Tolerance: 50ppm
- Testing the external clock:
 - Test setup: Connect frequency counter to serial interface, pin 11 (SWSA). Connect clock source (TTL, 1.5 MHz) to pin 4 (SCLKIN).
 - Settings: Instrument: DIG48, Channel: 1, Output: SERIAL, Wrd lngth: 32, Sample Frq: EXTERN
 - Measure: Check word clock using frequency counter. Nom. value: externally applied clock / 32;
- Testing the framesync position and polarity
 - Test setup: Connect oscilloscope to serial output (SCLK, SWSA, SDATAA), trigger on word clock (SWSA).
 - Settings: Instrument: DIG48, Channel: 1, Input: SERIAL, Wrd lngth: 32, Sample Frq: 48000, Function: Sine, frequency = 2Hz
 - Measure: Check a bit pattern according to Fig. 2-15 in section 2.5.3. on the oscilloscope. The data line „pulsates“ with 2Hz.
Repeat measurement with all Framesync positions.
Repeat measurement with channel 2.
Invert bit clock or word clock and check on the oscilloscope.

3. Testing the parallel interface

- Function test:
 - Test setup: Connect UPD generator via 37-contact DSUB connection (all lines (except pin 17) through-connected) to its own analyzer or a second UPD.
 - Settings: Analyzer: Instrument: DIG48kHz, Channel: 1, Input: PARALLEL, FUNCTION: FFT, Size: 8192, Window: RIFE VINC 3
 - Measure: Set 997 Hz, 0.9 FS on the generator, measure using FFT. Spurious in the FFT smaller than -130 dB.
- Output clock (word clock):
 - Test setup: Connect frequency counter to parallel interface, pin 35 (STROBE OUT).
 - Settings: Instrument: DIG48, Channel: 1, Output: PARALLEL
 - Measure: Set Samplefrq = 32000, 44100, 48000 Hz one after the other on the generator, check using the frequency counter. Tolerance: 50ppm

4. Testing the internal interfaces

The interfaces to the internal analog hardware are implicitly checked when testing the analog boards.

7.4.1.3 Option AES/EBU

1. Function test:

Perform the measurements as with the Digital Analyzer, but select AES/EBU, S/P DIF or OPTICAL (each two-channel) instead of the INTERNAL interface, single-channel. Select a clock rate of 48 kHz both for the generator and the analyzer.

Select PROTOCOL in the DISPLAY panel as operation. The involved errors are indicated in the error window. There must not be any error message (indication: NONE).

2. Testing the outputs and inputs

Perform one loop measurement each with AES/EBU, S/P DIF and OPTICAL. The required cables are included in the service kit.

Generator setting	Instrument	DIG 48kHz
	Channel(s)	1 & 2
	Output	S/P DIF
	Sample Freq	48kHz
	Audio Bits	20
	Dig. Vpp	1.000 V
	Max Volt	1.000 FS
	Ref Freq	1000.0 Hz
	Function	SINE
Analyzer setting	Voltage	0.71 FS
	Instrument	DIG 48kHz
	Channel(s)	1 & 2
	Input	S/P DIF
	Sample Freq	48kHz
	Audio Bits	20
	FUNCTION	RMS

Measurement result: 0.5 FS

3. Testing the output levels

See section 7.4.5.4, page 7.253.

4. Testing the input sensitivity

See section 7.4.5.4, page 7.255.

7.4.2 Digital Analyzer

Circuit diagram	1030.8506.01 S
Component location plan	1030.8506
Parts list	1030.8506.01 SA

Diagram overview	
Sheet:	Contents
1/11:	Block diagram
2/11:	Connection to the AT bus, decoding, SERPA
3/11:	DSP CPU, wait state logic
4/11:	External serial interface, internal interface ANLG22 and PFC
5/11:	Internal parallel interface (ANLG 110 and 300)
6/11:	External parallel interface, control register and link of DSP
7/11:	DSP memory, fast and slow, small version, R/W decoder
8/11:	External ROM code (not fitted)
9/11:	DSP memory, fast and slow, large version
10/11:	Pin assignment
11/11:	AT-bus assignment

7.4.2.1 Function

The Digital Analyzer board is plugged into the PC Mainboard (Standard AT) installed in the UPD: It accommodates the AT-bus interface, the DSP used for signal analysis with associated memory, the interface logic for the external and internal ports as well as the digital section of the frequency counter.

- AT bus interface

The bus interface consists of an address comparator (D24) with series-connected decoder (D22). From this, a chip-select signal is derived for the SERPA (SERial-PArallel converter) which also internally links IOW, IOR, DACK6 and the remaining addresses.

The SERPA generates control signals for switching over the direction of the bus drivers and for operation of external registers (Board ID and CONTROL).

The two DSPs are connected via two fast serial links (each consisting of DATA, CLOCK and FRAME SYNC, see also the illustration on page 6.8). (DSP A is located on this board (connected with channel 1), DSP B is located on another board which may be installed as Option UPD-B3 (connected with channel 2).)

The addresses are inserted on four base address areas. This base can be selected via a jumper on 290H-293H or 390H-393H (default) (i.e. the Digital Analyzer decodes the address bits A15, A15, etc. which are not used on the AT otherwise).

Set addresses:

without jumper X9:	Base:	0390H - 0393H
(default)	further addr.:	0B90H - 0B93H (+ n * 800H)
with jumper X9:	Base:	0290H - 0293H
	further addr.:	0A90H - 0A93H (+ n * 800H)

The addresses reach as far as max 3FFFH. (A14 and A15 = low), the PFC addresses range from 4000H to 7FFFH with the same base address as the SERPA.

Addresses (without jumper X9)			
0390H	Data channel 0, low word	2390H	Transmit control
0392H	Data channel 0, high word	2392H	WR strobe
0B90H	Data channel 1, low word	2B90H	reserved
0B92H	Data channel 1, high word	2B92H	wrb0ex - Strobe
1390H	Interrupt control register	3390H	Receiver 0 control
1392H	Analog data register	3392H	wrb1ex - Strobe
1B90H	Setting bit clock	3B90H	Receiver 1 control
1B92H	Analog strobe	3B92H	Test register SERPA

Control registers D612 and D613, line IWR0, address 02B92H:		
Bit:	Name	Meaning
0	LINKA0	Receive multiplexer DSP A
1	LINKA1	0=A, 1=B, 2=GEN, 3=D(AES-EBU)
2	LINKA2	Receive multiplexer DSP B (Highspeed)
3	LINKA3	0=A, 1=B, 2=GEN, 3=D(AES-EBU)
4	STRBPOLA	Clock polarity parallel DSP A
5	STRBPOLB	Clock polarity parallel DSP B
6	RESETA	Reset DSP A
7	RESETB	Reset DSP B
8	RESETC	Reset analog converter
9	ENACLK	Enable clock outputs (serial, parallel)
10	DSPHOLDB	HOLD DSP B
11	ASMUX	Serial input select DSP A
12	BSMUX	Serial input select DSP B
13	ENALINK	Enable send on link
14	DSPHOLDA	HOLD DSP A
15	WREN	Enable analog settings

The AT can be addressed via 2 interrupt lines which are selectable by means of jumpers:

IRQ10: with jumper X9.1 (default)

IRQ12: with jumper X9.2 (not inserted)

The SERPA can also release the DRQ6. This is done in the case of video transmissions and block transmissions of normal data. The DSP always sends 32 bits which are received in the SERPA. The latter sets the DMA request and is requested by means of DACK6 to apply its data to the AT bus. At the same time, the signals are provided for a memory access of the AT. DRQ6 is only cancelled after the second data transfer comprising 16 bits so that two DMA cycles are performed in close succession.

- Voltage supply of the clock generators:

An additional stabilization (implemented as additional board for board versions 4 and 5) permits to suppress interference on the +5-V path of the AT current supply. This stabilization operates as a series regulator with a power FET with a low dropout of 0.1 V. The reference voltage is derived from the provided 5 V by division and lowpass filtering.

For measurements using the internal converter, the 73.76-MHz crystal is cut off by an FET in order to avoid interference with the converter clock.

- Setting the analog hardware

The analog hardware is set by means of a shift register supplied with data, shift clock and the transfer pulse by the SERPA. The line IAIDI permits to read in data from the analog hardware (e.g. for identification and selftest).

In order to avoid clock interference with the analog hardware, the clock is only active during a data transmission. Eight bits are transferred one after the other in each case. After filling the shift register of the analog hardware (whose length may vary depending on the options fitted) the contents is transferred into the registers of the analog card with a write pulse (IAIWR).

By means of a read pulse (IAIRD), information is transferred from the analog cards (e.g. board identification) into the SR and read in by shifting.

- DSP

The ROM code version of the TMS 320C30 is used as DSP. The DSP has a cycle time of 60 ns and uses 32-bit floating numbers (not IEEE-compatible, however, it is converted by the access routine in the DSP when writing and reading DSP addresses).

The DSP uses a 33.5-MHz clock, providing 16.75 MHz to pin H1 with a correct clock.

The internal ROM contains a bootstrap program as well as selftest routines. The bootstrap program is activated when starting the UPD for the first time (see section 6.1.2.1, page 6.7).

The DSP is provided with 4 interrupt inputs which are assigned as follows:

INT0:	Gate array SERPA (thus used with: ANLG22, SERIAL (+MUX))
INT1:	Parallel interface internal (ADS 112) (thus used with: ANLG110 and ANLG300)
INT2:	Parallel interface external (thus used with: PARALLEL, PARAL MUX)
INT3:	not used

- DSP memory

The complete memory is located at the primary bus, consisting of 2 banks with different access times.

The address A21 is inverted and fed back to the input /READY, i.e. all addresses $N * (2^{22}) + x$ with $x < 2^{22}$ are addressed with 0 wait states.

Address:	Memory area
000000-00FFFF:	2 WS via hardware logic: EPROM (This hardware logic is not fitted normally; if the EPROM is fitted, the wait state logic must be fitted and jumper X9.6 (ROM) plugged in)
200000-207FFF:	0 WS via A21 feedback: FAST SRAM (25ns): Code and data
400000-41FFFF:	2 WS via software: SLOW SRAM (85ns): only data

Bus programming:

Software wait states and hardware ready; the wait state logic is only required if EPROMs are fitted.

- DSP ports

Address:	Signal	Port
8000x0-8000x7:		Gate array SERPA
8004x0-8004x0:	ECSWRT:	WR clock generation fast converter
8004x0-8004x0:	ECSINT:	RD parallel interface internal
8004x1-8004x1:	ECSEXT:	RD parallel interface external

Note: The gate array SERPA is driven with 0 wait states via hardware ready (MSB of the address).

- Internal analog converter, parallel (sheet 5)

The clock ADSCLK (6.144MHz) generated by the SERPA is divided to obtain the desired clock (ANLG100: 334kHz, ANLG300: 1.024MHz) in divider D50. The division factor is written into register D52 (ECSWRT) by the DSP.

On line SOC, a pulse with the width of an output clock is generated, followed by a variable pause. The duration of the pause is used to set the sampling rate.

Since the converter on the ADC Board uses 'binary offset' as data format, the MSB is inverted with EXOR D64 in order to achieve the twos complement representation.

After SOC, the converter responds with EOC, which is also used to load the data into the receive register and also send an interrupt INT1 to the DSP. The latter is reset when reading the receive register with ECSINT.

- Internal digital link

All DSPs in the UPD are connected with each other via a four-way serial link. Each DSP is assigned a transmission line and can switch its input to all other transmission lines (also its own one) using a 4:1 multiplexer. In addition, a SYNC line can be set and read by all DSPs (see page 6.15).

- Serial interface

The universal serial input is connected to the serial input 1 of the SERPA via a multiplexer (control of the multiplexer with ASMUX or BSMUX). Interrupt used on the DSP: INTO.

- Frequency counter (PFC)

For measurement of frequency and phase (analog) as well as the sampling rate with the interfaces AES/EBU, S/P DIF and OPTICAL, the gate array PFC (Programmable Frequency Counter) is used.

The 10-MHz reference clock is generated by crystal oscillator B43. This reference clock is used to supply the counters for the frequencies and to synchronize the signals for the phase measurement (output CLK10M).

The ready signal PFCREADY is applied to interrupt input 0 of the AT SERPA.

The PFC is driven by the analog hardware with the signals FAMESS, FBMESS, PHASA and PHASB.

The line LDFREQ is used to control the frequency of the analog sinewave generator (LDG), the input clock frequency for AES/EBU is measured via the line CLOCKDI. (See page 6.11)

- Jumper settings:

Jumper	Inscription	inserted
X9A.1 - X9B.1	I10	yes
X9A.2 - X9B.2	I12	no
X9A.3 - X9B.3	290	no
X9A.6 - X9B.6	ROM	no
X22A.1 - X22B.1	INT	yes
X22A.2 - X22B.2	LINK	no
X22A.3 - X22B.3	FREQ0	yes
X22A.4 - X22B.4	FREQ1	yes
X22A.5 - X22B.5	FREQ2	yes
X42.1 - X42.2	10MHz crystal	yes

7.4.2.2 Measuring Instruments

C30 Emulator XDS500 (PC plug-in card and software)

Oscilloscope, bandwidth >150MHz

Logic generator

7.4.2.3 Troubleshooting

On occurrence of the following error messages, proceed as follows:

- Digital Analyzer not found
 - Check: Manual reading (e.g. via debugger) of port address 02B92H: contents 04 or 05 (only the least significant byte is valid).
 - AT bus may be faulty. In this case, other cards cannot be properly addressed either.
 - New hardware on old software
 - Fault in bus address decoder D24; when the card is accessed, pin 19 must briefly become LOW.
 - Fault in the SERPA; in this case, no read pulse is applied to pin 19 when register D25 is accessed, or the bus direction is not switched over (D26 and D27, pin 1)
- Status message (in the OPTION panel) Highspeed -NA- (not available)
 - Check the detection line: Manual reading (e.g. via debugger) of port address 2B90H (test register of the SERPA: Bit 5 must be low. (Otherwise check connection cable AB-CONN).
 - New hardware on old software (which identifies the read board identification as invalid).
- Can't boot DSP . . .

This fault may be due to a variety of causes.

 - Fault in AT SERPA: When a boot attempt is made, signals must arrive on line DR0 at the DSP (similar to RS232). The DSP must respond by sending a signal on line DX0.

- Fault when writing to the control register (D612 and D613). The control register must always be enabled after the program start (OUTEN, pin 1 at LOW). Check the lines RESET and HOLD of the respective DSP. (see boot procedure, page 6.7)
 - Fault in clock supply on AT side: 14.318 MHz must be applied to SERPA D2, Pin 55 (FREQ 2).
 - Fault in clock supply on DSP side: 33.5 MHz with a deviation of 4 V must be applied to DSPCLK (Pin 16). Otherwise check jumper X22.
 - Fault in DSP or DSP memory: For further diagnosis, an XDS 500 must be connected to the emulation connector.
- Message Input ??, Press SHOW IO in the readout, the message no input signal appearing after SHOW IO although all external connections are made properly.
 - Check the respective interrupt inputs of the DSP for the signal applied (see DSP manual).
 - In the case of SERIAL (INT0): Check the input signal at the SERPA following the multiplexer, check the multiplexer select line. Check the connection cable (16-contact) to the front panel.
 - In the case of PARALLEL (INT2): Check PSTROBE before and after the EXOR (D64-A).
 - In the case of INTERNAL: Check the connection cable (16-contact) to the generator. Check the multiplexer setting of the link, serial input 1 of the DSP.
 - in the case of AES/EBU, S/P DIF and OPTICAL: Check the connection cable (16-contact) to the generator. Check the connection cables (10-contact, 3-contact and 2*coax) from the AES/EBU board to the front panel. Check the multiplexer setting of the link, serial input 1 of the DSP.
- The signal measured features a very poor S/N ratio on the digital interface, in particular harmonics and/or white spectrum can clearly be seen.
 - A bit on the port or expansion bus of the DSP *got stuck*. The best thing to do is to apply a non-subharmonic, fully driven sinewave signal and check whether each bit „flips“.
 - Faulty samples are read in; check the signals at the input for correct level and transfer edge.
- Status message ANLO: ORUN:
 - An interrupt on the DSP *got stuck* and causes permanent interrupt. Therefore, the communication program to the AT is no longer assigned any CPU time.
 - The software in the DSP has crashed; remedy by a new start of the UPD after resetting the DSPs by means of the command `logdsp -f`.
- No display with function FFT and SCOPE, or error message DMA Timeout . . . :
 - DRQ6 provides no signal. In this case, the DMA controller cannot be started.
 - The Digital Analyzer does not respond with data to DACK6. The display is completely filled in this case.
 - The AT-BIOS is not configured properly. Check according to section 4 of the operating manual.

7.4.2.4 Testing and Adjustment

Testing:

The DSP with the memory and the AT interface are checked using the built-in selftest routine. Check the interfaces according to section 7.4.1 Testing the Rated Specifications.

Adjustment:

There is no need for an adjustment.

7.4.2.5 Disassembly and Assembly

After opening the instrument, remove the bracket above the digital section and unscrew the clip at the rear. Remove the cables from the analog section to the generator (16-contact), from the analog section to the analyzer (34-contact), the cables to the generator (16-contact) and to the option -B3 (Highspeed) (50-contact), if installed.

During replacement make sure that the correct (upper) 34-contact connection cable to the Analog Motherboard is plugged in. Do not forget the serial connection cable to the front panel.

7.4.2.6 External Interfaces

Parallel audio interface (37-contact DSUB connector, M)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X60.1,16,19	
OUT5V		0		5V ± 5%, 50mA	X60.17	
GND					X60.18	
DA27	Dig Audio (MSB)		external	TTL	X60.2	
DA26	Dig Audio		external	TTL	X60.3	
DA25	Dig Audio		external	TTL	X60.4	
DA24	Dig Audio		external	TTL	X60.5	
DA23	Dig Audio		external	TTL	X60.6	
DA22	Dig Audio		external	TTL	X60.7	
DA21	Dig Audio		external	TTL	X60.8	
DA20	Dig Audio		external	TTL	X60.9	
DA19	Dig Audio		external	TTL	X60.10	
DA18	Dig Audio		external	TTL	X60.11	
DA17	Dig Audio		external	TTL	X60.12	
DA16	Dig Audio		external	TTL	X60.13	
DA15	Dig Audio		external	TTL	X60.14	
DA14	Dig Audio		external	TTL	X60.15	
DA13	Dig Audio		external	TTL	X60.20	
DA12	Dig Audio		external	TTL	X60.21	
DA11	Dig Audio		external	TTL	X60.22	
DA10	Dig Audio		external	TTL	X60.23	
DA09	Dig Audio		external	TTL	X60.24	
DA08	Dig Audio		external	TTL	X60.25	
DA07	Dig Audio		external	TTL	X60.26	
DA06	Dig Audio		external	TTL	X60.27	
DA05	Dig Audio		external	TTL	X60.28	
DA04	Dig Audio		external	TTL	X60.29	
DA03	Dig Audio		external	TTL	X60.30	

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- continued -						
name	Signal description	≡	source dest.	range	connector	comment
DA02	Dig Audio		external	TTL	X60.31	Polarity selectable Frequency settable Frequency settable
DA01	Dig Audio		external	TTL	X60.32	
DA00	Dig Audio (LSB)		external	TTL	X60.33	
LR	Wordselect		external	TTL	X60.34	
PSTROBE	Clock		external	TTL	X60.35	
PCLKOUT	Bit clock	O	Dig Gen	CMOS ($R_i = 50\Omega$)	X60.36	
PWSOUT	Audio clock output	O	Dig Gen	CMOS ($R_i = 50\Omega$)	X60.37	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Serial audio interface (16-contact flat connector or 15-contact DSUB)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X40.1	=1
GND					X40.3	=2
GND					X40.13	=7
GND					X40.15	=8
OUT5V		O	external	$5V \pm 5\%, 50mA$	X40.8	=12
SCLKA	Channel A		external	TTL	X40.2	=9, Bit clock
SDATAA			external	TTL	X40.4	=10, Data bits
WORDSELA			extern	TTL	X40.6	=11, Framesync.
SCLKB	Channel B		external	TTL	X40.14	=15, Bit clock
SDATAB			external	TTL	X40.12	=14, Data bits
WORDSELB			external	TTL	X40.10	=13, Framesync.
ACLKOUT	Bit clock output	O	external	CMOS ($R_i = 50\Omega$)	X40.7	=4, Frequency settable
SWSOUT	Audio clock output, Frame	O	external	CMOS ($R_i = 50\Omega$)	X40.9	=5, Frequency settable
SLROUT	Audio clock output, L/R	O	external	CMOS ($R_i = 50\Omega$)	X40.11	=6, Frequency settable

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Internal interface to Analog Analyzer (ANACONN) (34-contact flat connector)						
name	Signal description	≡	source dest.	range	connector	comment
GND			AnaMoth		X30A.1	= Line 1
PEAKA	Interrupt A		AnaMoth	TTL	X30B.1	=2
FAMESS	Freq. A		AnaMoth	TTL	X30A.2	=3
PEAKB	Interrupt B		AnaMoth	TTL	X30B.2	=4
FBMESS	Freq. B		AnaMoth	TTL	X30A.3	=5
LDFREQ	Freq. Low D.		AnaMoth	TTL	X30B.3	=6
PHASA	Phase A		AnaMoth	TTL	X30A.4	=7
IAIRD	Read Strobe	O	AnaMoth	TTL	X30B.4	=8
IAIWR	Write Strobe	O	AnaMoth	TTL	X30A.5	=9
IAIDO	Data Out	O	AnaMoth	TTL	X30B.5	=10
IAICLK	Clock	O	AnaMoth	TTL	X30A.6	=11
IAIDI	Data In		AnaMoth	TTL	X30B.6	=12
WREN	Write Enable	O	AnaMoth	TTL	X30A.7	=13
SCKLOUT	Audio Clock	O	AnaMoth	TTL	X30B.7	=14
CCLK	Audio Clock	O	AnaMoth	TTL	X30A.8	=15

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name	Signal description	≡	source dest.	range	connector	comment
CDATA	Audio Data		AnaMoth	TTL	X30B.8	=16
CLR	Wordclock	O	AnaMoth	TTL	X30A.9	=17
CATP	Stereosync.	O	AnaMoth	TTL	X30B.9	=18
PHASB	Phase B		AnaMoth	TTL	X30A.10	=19
SOC	Start Conv.	O	AnaMoth	TTL	X30B.10	=20
EOC	End Conv.		AnaMoth	TTL	X30A.11	=21
ADS0	Paral. Data of ADS112		AnaMoth	TTL	X30B.11	=22
ADS1			AnaMoth	TTL	X30A.12	=23
ADS2			AnaMoth	TTL	X30B.12	=24
ADS3			AnaMoth	TTL	X30A.13	=25
ADS4			AnaMoth	TTL	X30B.13	=26
ADS5			AnaMoth	TTL	X30A.14	=27
ADS6			AnaMoth	TTL	X30B.14	=28
ADS7			AnaMoth	TTL	X30A.15	=29
ADS8			AnaMoth	TTL	X30B.15	=30
ADS9			AnaMoth	TTL	X30A.16	=31
ADS10			AnaMoth	TTL	X30B.16	=32
ADS11			AnaMoth	TTL	X30A.17	=33
GND			AnaMoth		X30B.17	=34

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Internal interface to Highspeed Option (ABCONN) (50-contact flat connector)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X71A.1	= 1
FREQ0	49.152MHz	O	DSP B	CMOS	X71B.1	= 2
GND				D	X71A.2	= 3
FREQ1	67.7376MHz	O	DSP B	CMOS	X71B.2	= 4
GND				D	X71A.3	= 5
FREQ2	73.728MHz	O	DSP B	CMOS	X71B.3	= 6
GND				D	X71A.4	= 7
ADATA	Audio Data A	O	DSP B	TTL	X71B.4	= 8, from FP
ACLK	Bit clock	O	DSP B	TTL	X71A.5	= 9
AFS	Framesync.	O	DSP B	TTL	X71B.5	=10
BDATA	Audio Data B	O	DSP B	TTL	X71A.6	=11
BCLK	Bit clock	O	DSP B	TTL	X71B.6	=12
BFS	Framesync.	O	DSP B	TTL	X71A.7	=13
GND					X71B.7	=14
CLR	Analog Sync	O	DSP B	TTL	X71B.8	=16
BFSX0	DSP B to		DSP B	TTL	X71B.9	=18
BCLKX0	Serpa		DSP B	TTL	X71A.10	=19
GND					X71B.10	=20
BFSR0	Data from	O	DSP B	TTL	X71A.11	=21
BDR0	SERPA to	O	DSP B	TTL	X71B.11	=22
CLKR0	DSP B	O	DSP B	TTL	X71A.12	=23
ENALINK	Enable Link	O	DSP B	TTL	X71B.12	=24
+5V		O		5V (±5%), 1A	X71A.13	=25
RESETB	Reset DSP B	O	DSP B	TTL	X71B.13	=26
GND					X71A.14	=27
SYNC	Sync of DSP	B	DSP B	TTL	X71B.14	=28
STRBPOLB	Parallel SN	O	DSP B	TTL	X71A.15	=29 H=inverted
LINKA2	Link address	O	DSP B	TTL	X71B.15	=30 see control reg.

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name	Signal description	≡	source dest.	range	connector	comment
LINKA3		O	DSP B	TTL	X71A.16	=31
GND					X71B.16	=32
FSXG	Link Gen.	B	all DSPs		X71A.17	=33
CLKXG		B	all DSPs		X71B.17	=34
TXDG		B	all DSPs		X71A.18	=35
FSXD	Link D	B	all DSPs		X71B.18	=36
CLKXD		B	all DSPs		X71A.19	=37
TXDD		B	all DSPs		X71B.19	=38
GND					X71A.20	=39
FSXB	Link B	I	all DSPs		X71B.20	=40
CLKXB		I	all DSPs		X71A.21	=41
TXDB		I	all DSPs		X71B.21	=42
FSXA	Link A	O	all DSPs		X71A.22	=43
CLKXA		O	all DSPs		X71B.22	=44
TXDA		O	all DSPs		X71A.23	=45
GND					X71B.23	=46
BDSPCLK	33.5 MHz	O	DSP B	5V (± 5%), 1A	X71A.24	=47
+5V		O	DSP B		X71B.24	=48
BSMUX	Ser. Select	O	DSP B		X71A.25	=49
n.c.					X71B.25	=50

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Internal interface to Digital Generator (DSPLINK)						
(16-contact flat connector, above)						
name	Signal description	≡	source dest.	range	connector	comment
GND		O		CMOS	X70. 1	
TXDA	Link A	B	all DSPs	CMOS	X70. 2	
CLKXA		B	all DSPs	CMOS	X70. 3	
FSXA		B	all DSPs	CMOS	X70. 4	
TXDB	Link B	B	all DSPs	CMOS	X70. 5	
CLKXB		B	all DSPs	CMOS	X70. 6	
FSXB		B	all DSPs	CMOS	X70. 7	
TXDD	Link D	B	all DSPs	CMOS	X70. 8	
CLKXD		B	all DSPs	CMOS	X70. 9	
FSXD		B	all DSPs	CMOS	X70.10	
TXDG	Link G	B	all DSPs	CMOS	X70.11	
CLKXG		B	all DSPs	CMOS	X70.12	
FSXG		B	all DSPs	CMOS	X70.13	
LDSPCLK	33.5 MHz	B	all DSPs	CMOS	X70.14	
SYNC	Sync DSPs	B	all DSPs	CMOS	X70.15	betw. D and G
CLOCKDI	AES-Clock	I	DSP D	CMOS	X70.16	clock meas.

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.4.3 Option UPD-B4 Highspeed

Circuit diagram	1030.8506.04 S
Component location plan	1030.8506
Parts list	1030.8506.04 SA

Function

This card is a version (04) of the Digital Analyzer of the basic instrument. All bus interface devices, the PFC for frequency measurement and the crystals for clock generation are not fitted. Control lines for the second DSP board (ending with ..B) are short-circuited by 0 Ω resistors in version 04 with the *normal* control lines (ending with ..A).

The other functions of the board are identical with those of the analyzer of the basic instrument. The card is connected with the normal Digital Analyzer via a 50-contact connection cable. The lower 34-contact flat cable is used for connection to the analog hardware.

7.4.4 Digital Generator

Circuit diagram	1030.8706.01 S
Component location plan	1030.8706
Parts list	1030.8706.01 SA

Diagram Overview	
Sheet:	Contents
1/12:	Block diagram
2/12:	Connection to AT bus, decoding, SERPA
3/12:	DSP CPU, wait state logic
4/12:	external serial interface, internal interface audio data
5/12:	Setup memory (CMOS)
6/12:	External parallel interface, control register and link of DSP
7/12:	DSP memory, fast and slow, small version, R/W decoder
8/12:	External ROM code (not fitted)
9/12:	DSP memory, fast and slow, large version
10/12:	Keyboard decoder PERIF
11/12:	Pin assignment
12/12:	AT-bus assignment

7.4.4.1 Function

The Digital Generator is inserted into the PC mainboard (standard AT) installed in the UPD. It accommodates the AT-bus interface, the DSP for signal generation including the associated memory, the interface logic for the external and internal ports as well as the keyboard decoder.

- AT-bus interface

The bus interface consists of an address comparator (D24) with series-connected decoder (D22). From this, a chip-select signal is derived for the SERPA, which also internally links IOW, IOR, DACK5 and the remaining addresses.

The SERPA generates control signals for switching over the direction of the bus drivers (D26 and D27) and for operation of external registers (Board ID and CONTROL).

The two DSPs are connected via two fast serial links (DATA, CLOCK and FRAME SYNC in each case; see also illustration on page 6.8). (DSP G is located on this board, DSP D refers to the DSP on the Option UPD-B2 (AES-EBU))

The addresses are inserted on four base address areas. This base can be selected via a jumper on 290H or 390H (default). (i.e. the Digital Generator decodes the address bits A15, A14, etc. which are normally not used on the AT).

Set addresses:

without jumper X9:	Base:	8390H - 8393H
	further addr.:	8B90H - 8B93H (+ n * 800H)
with jumper X9:	Base:	8290H - 8293H
	further addr.:	8A90H - 8A93H (+ n * 800H)

The addresses begin with 8000H and reach as far as max BFFFH. (A14 = low and A15 = high).

The address area of the PERIF starts with C000H and lies at the same base addresses as the SERPA.

Addresses (without jumper X9)			
8390H	Data channel 0, low word	A390H	Transmit control
8392H	Data channel 0, high word	A392H	WR strobe
8B90H	Data channel 1, low word	AB92H	reserved
8B92H	Data channel 1, high word	AB92H	wrb0ex - strobe
9390H	Interrupt control register	B390H	Receiver 0 Control
9392H	Analog data register	B392H	wrb1ex - strobe
9B90H	Setting bit clock	BB90H	Receiver 1 control
9B92H	Analog strobe	BB92H	Test register SERPA

Control register port D612 and D613, line IWR0, address 0AB92H		
Bit:	Name	Meaning
0	LINKA0	Receive multiplexer DSP G
1	LINKA1	0=A, 1=B, 2=GEN, 3=D(AES-EBU)
2	LINKA2	Receive multiplexer DSP D (AESEBU)
3	LINKA3	0=A, 1=B, 2=GEN, 3=D(AES-EBU)
4	CLKPOL	Clock polarity output signal
5	SADR16	Switchover address 16 setup RAM
6	RESETG	Reset DSP G
7	RESETD	Reset DSP D
8	ENA INTERN	Enable internal output (D/A converter)
9	ENA EXCLK	Enable external clock
10	ENA PAROUT	Enable parallel output
11	CNTRAM	Select counter or setup RAM
12	FRAMEWS	Select FSX or Wordsel output
13	ENA PARCLK	Enable clock output parallel
14	ENA SEROUT	Enable serial output
15	WREN	Enable analog settings

The AT can be addressed via two interrupt lines which are selectable by means of jumpers:

IRQ9: with jumper X9.1 (not inserted)

IRQ11: with jumper X9.2 (default)

The SERPA can also release the DRQ5. This is only the case with video transmissions or block transmissions of normal data. Both cases do not happen on the Digital Generator during normal operation of the UPD. DMA operation see page 7.228.

- Voltage supply of the clock generators:

An additional stabilization (only implemented with board versions 82 and 83 as additional board) is used to suppress interference on the +5-V path of the AT current supply. This stabilization operates as series regulator with a power FET with a low dropout of 0.1 V. The reference voltage is derived from the provided 5 V by division and lowpass filtering.

- Setting the analog hardware

Identical with Digital Analyzer, see page 7.229.

- DSP

The ROM code version of the TMS 320C30 is used as DSP. The DSP features a cycle time of 60ns and uses 32-bit floating numbers (not IEEE-compatible, however, it is converted by the access routine in the DSP when writing and reading DSP addresses).

The DSP is provided with 4 interrupt inputs which are assigned as follows:

INT0:	Gate array SERPA (thus used with: ANLG25, SERIAL (+MUX))
INT1:	not used
INT2:	Parallel interface external (thus used with: PARALLEL, PARAL MUX)
INT3:	not used

- DSP memory

The complete memory is at the primary bus, consisting of 2 banks with different access times.

The address A21 is inverted and fed back to the input /READY, i.e. all addresses $N * (2^{22}) + x$ with $x < 2^{22}$ are addressed with 0 wait states.

Address:	Memory area
000000-00FFFF:	2 WS via hardware logic: EPROM (This hardware logic is usually not fitted; if the EPROM is fitted, the wait state logic must be fitted and jumper X9.6 (ROM) inserted)
200000-207FFF:	0 WS via A21 feedback: FAST SRAM (25ns): Code and data
400000-407FFF:	2 WS via software: SLOW SRAM (85ns): only data

Bus programming:

Software wait states and hardware ready; the wait state logic is only required if the EPROMs are fitted.

- DSP ports

Address:	Signal	Port
8000x0-8000x7:		Gate array SERPA
8004x0-8004x0:	ECSWRT:	WR parallel interface external

Note: The gate array SERPA is driven with 0 wait states via hardware ready (MSB of the address).

- Controlling the internal converter

The internal converter for ANLG25 (sampling rate 96 kHz) and ANLG110kHz (sampling rate 384kHz) is connected to serial output 1 of the SERPA. The bit clock is 24 times the sampling rate (2.304 MHz or 9.216 MHz).

- Parallel output

The parallel data are output via two series-connected registers. The internal clock signal is generated by SERPA FSX and output as STROBE OUT via a delay line (D68). As a result of this, the edge transition on the data is in about the middle between two clock edges.

The (data) output clock drives the output latches, at the same time, a 1 is loaded into interrupt register D69. This 1 occurs as INT2 on the DSP, which subsequently fills the first register again and resets D69.

The 5 volts for an external circuit are generated by a separate series regulator in order to avoid short-circuits of the switching power supply.

- Internal digital link

All DSPs in the UPD are connected with each other via a four-way serial link. Each DSP is assigned a transmission line and can switch its input to all other transmission lines (including its own) by means of a multiplexer. In addition, a SYNC line can be set and read by all DSPs (see page 6.15).

- Setup RAM

For storing the internal instrument states, a 64-kbyte CMOS-RAM (organized in 32k * 16) is used, whose voltage supply is maintained by a lithium battery (3.4 V) after switching off the UPD. The battery is soldered in on the Digital Generator and secured by cable clamps.

This RAM stores calibration data (see page 7.243).

Transistors V50 and V51 permit to switch between AC supply and battery operation; the two diodes V52 in the battery line reduce the bias to 2 volts, causing the current consumption of the CMOS RAMs to decrease further.

The RAM is accessed via a register designed as a counter. There, the first address to be read is loaded; with each further access to the RAM, the counter is increased by one address at the end of the access.

The control line CNTRAM (see page 7.239) makes a distinction between write access to the counter (CNTRAM = 1) or to the RAM (CNTRAM = 0).

The CMOS RAM can be fitted with 256 kbytes optionally; in this case, the line SADR16 is used to differentiate between the least and the most significant 128 kbytes.

- Keyboard decoder PERIF

The front-panel keyboard is controlled via gate array PERIF which also performs evaluation of the rotary knob.

The keyboard is designed as matrix between ROW and COL of the PERIF. The keyboard decoder is only activated on actuation of a key; it debounces the key and provides the appropriate repeat keystrokes when a key is permanently pressed.

A keystroke is reported to the AT via PERIF_INT, which is routed via the SERPA of the AT bus and its interrupt controller. The interrupt service routine picks up the sign and stores it in the keyboard buffer of the BIOS.

The parallel port of the PERIF is used for controlling the LEDs on the front panel and the backlighting of the LCD.

⇒ The mask version 1 of the PERIF may pretend bouncing of the internal keyboard on certain conditions. This fault is eliminated in version 2 (serial number 042 or greater).

- Jumper settings:

Jumper	Inscription	inserted
X9A.1 - X9B.1	I9	no
X9A.2 - X9B.2	I11	yes
X9A.3 - X9B.3	290	no
X9A.6 - X9B.6	ROM	no
X22A.1 - X22B.1	INT	yes
X22A.2 - X22B.2	LINK	no
X22A.3 - X22B.3	FREQ0	yes
X22A.4 - X22B.4	FREQ1	yes
X22A.5 - X22B.5	FREQ2	yes

7.4.4.2 Measuring Instruments

C30 Emulator XDS500 (PC plug-in card and software)
Oscilloscope, bandwidth >150MHz

7.4.4.3 Troubleshooting

On occurrence of the following error messages proceed as follows:

- Digital Generator not found
 - Check: Manual reading (e.g. via debugger) of the port address AB92H: Contents 82 or 83 (only the least significant byte is valid).
 - AT bus may be faulty. In this case, other cards cannot be properly addressed either.
 - New hardware on old software
 - Fault in bus address decoder D24; when the card is accessed, pin 19 must briefly become LOW.
 - Fault in the SERPA; in this case, no read pulse is applied to pin 19 when register D25 is accessed, or the bus direction is not switched over (D26 and D27, Pin 1)

- Can't boot DSP . .

This fault may be due to a variety of causes.

- Fault in AT SERPA: When a boot attempt is made, signals must arrive on line DR0 on the DSP (similar to RS232). The DSP must respond by sending a signal on line DX0.
- Fault when writing to the control register (D612 and D613). The control register must always be enabled after the program start (OUTEN, pin 1 applied to LOW). Check the lines RESET and HOLD of the respective DSPs. (see boot procedure, page 6.7)
- Fault in the clock supply on AT side: 14.318 MHz must be applied to SERPA D2, pin 55 (FREQ 2).
- Fault in the clock supply on DSP side: 33.4 MHz with a deviation of 4 volts must be applied to DSPCLK (pin 16). Otherwise check jumper X22.
- Fault in DSP or DSP memory: For further diagnosis, an XDS500 must be connected to the emulation connector.

- No output signal although all external connections are made properly.
 - Check the respective interrupt inputs of the DSP for the applied signal (see description DSP).
 - With SERIAL (INT0): Check the clock signal at the SERPA, Check the output drivers. Check the connection cable (16-contact) to the front panel.
 - With PARALLEL (INT2): Check the clock signal and the output drivers.
 - With INTERNAL: Check the connection cable (16-contact) to the analyzer. Check the transmission driver.
 - With AES/EBU, S/P DIF and OPTICAL: Check the connection cable (40-contact) between generator and AES/EBU board. Check the connection cables (10-contact, 3-contact and 2*coax) from the AES/EBU board to the front panel. Check the SYNC line (see page 6.15).
- The generated signal features a very poor S/N ratio, in particular harmonics and/or white spectrum can clearly be seen.
 - A bit on the port or expansion bus of the DSP *got stuck*. The best thing to do is to set a non-subharmonic, fully driven sinewave signal and check whether each bit „flips“.
 - Faulty samples are generated; check the clock signals for correct level and transfer edge.
- Status message GEN: HALTED:
 - An interrupt on the DSP *got stuck* and causes permanent interrupt. Therefore, the communication program to the AT is no longer assigned any CPU time.
 - The software in the DSP has crashed; remedy by new start of the UPD after resetting the DSPs using the command `logdsp -f`.
 - This message occurs regularly if the Digital Generator has been interrupted in the calculation of a complex waveform by an operation.

7.4.4.4 Testing and Adjustment

Testing:

The DSP with the memory and the AT interface are checked using the built-in selftest routine. Check the interfaces according to section 7.4.1 Testing the Rated Specifications.

Adjustment:

There is no need for an adjustment.

7.4.4.5 Disassembly and Assembly

After opening the instrument remove the bracket above the digital section and unscrew the clip at the rear.

Remove the cables from the analog section to the generator (16-contact), the connection to the analyzer (16-contact), the connection to the Option B2 (AES/EBU) (40-contact), if installed, and the connection to the front panel.

CAUTION:

This board contains the CMOS RAM, where the calibration values are stored. They are provided on the hard disk as a backup copy.

After installing the new Digital Generator, its CMOS RAM should be cleared by the DOS command

```
clr_cmos -d
```

before starting the UPD: The calibration data are then restored from the hard disk when starting the UPD.

7.4.4.6 External Interfaces

AT-Bus: acc. to P996 Working Group, Microprocessor Standards Committee (see section 7.6.1.7, Digital Motherboard, page 7.275).

Parallel audio interface (37-contact DSUB connector, W)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X61.1,16,19	
OUT5V		O		5V ± 5% 50mA	X60.17	
GND					X61.18	
DA27	Dig Audio (MSB)	O	external	TTL	X61.2	
DA26	Dig Audio	O	external	TTL	X61.3	
DA25	Dig Audio	O	external	TTL	X61.4	
DA24	Dig Audio	O	external	TTL	X61.5	
DA23	Dig Audio	O	external	TTL	X61.6	
DA22	Dig Audio	O	external	TTL	X61.7	
DA21	Dig Audio	O	external	TTL	X61.8	
DA20	Dig Audio	O	external	TTL	X61.9	
DA19	Dig Audio	O	external	TTL	X61.10	
DA18	Dig Audio	O	external	TTL	X61.11	
DA17	Dig Audio	O	external	TTL	X61.12	
DA16	Dig Audio	O	external	TTL	X61.13	
DA15	Dig Audio	O	external	TTL	X61.14	
DA14	Dig Audio	O	external	TTL	X61.15	
DA13	Dig Audio	O	external	TTL	X61.20	
DA12	Dig Audio	O	external	TTL	X61.21	
DA11	Dig Audio	O	external	TTL	X61.22	
DA10	Dig Audio	O	external	TTL	X61.23	
DA09	Dig Audio	O	external	TTL	X61.24	
DA08	Dig Audio	O	external	TTL	X61.25	
DA07	Dig Audio	O	external	TTL	X61.26	
DA06	Dig Audio	O	external	TTL	X61.27	
DA05	Dig Audio	O	external	TTL	X61.28	
DA04	Dig Audio	O	external	TTL	X61.29	
DA03	Dig Audio	O	external	TTL	X61.30	
DA02	Dig Audio	O	external	TTL	X61.31	
DA01	Dig Audio	O	external	TTL	X61.32	
DA00	Dig Audio (LSB)	O	external	TTL	X61.33	
LR	Wordselect	O	external	TTL	X61.34	
STROBOUT	Takt	O	external	TTL	X61.35	Polarity selectable
EXSTRBIN	Bit clock	I	external	TTL	X61.36	Frequency settable
n.c.						
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						
- continued -						

- continued -						
name	Signal description	≡	source dest.	range	connector	comment

Serial audio interface (16-contact flat connector or 15-contact DSUB)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X40.1	=1
GND					X40.3	=2
GND					X40.13	=7
GND					X40.15	=8
OUT5V		O	external	5V ± 5%, 50mA	X40.8	=12
SCLKA	Channel A	O	external	CMOS	X40.2	=9, Bit clock
SDATAA		O	external	CMOS	X40.4	=10, Data bits
WORDSELA		O	external	CMOS	X40.6	=11, Framesync.
SCLKB	Channel B	O	external	CMOS	X40.14	=15, Bit clock
SDATAB		O	external	CMOS	X40.12	=14, Data bits
WORDSELB		O	external	CMOS	X40.10	=13, Framesync.
SCLKIN	Bit clock input	I	external	TTL	X40.7	=4
SWSOUT	Audio clock output, Li-Re	O	external	CMOS (R _i = 50Ω)	X40.11	=6, Frequency settable
n.c.					X40.9	=5

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Internal interface to AES-EBU Option (DG-CONN)						
name	Signal description	≡	source dest.	range	connector	comment
GND		O			X50.1	= 1
FREQ0		O		CMOS	X50.2	= 2 Audio clock
+5V		O			X50.3	= 3
FREQ1		O		CMOS	X50.4	= 4 Audio clock
GND		O			X50.5	= 5
DDX0		I		CMOS	X50.6	= 6 ser. SN from
DFSX0		I		CMOS	X50.7	= 7 DSP D
DCLKX0		I		CMOS	X50.8	= 8
GND		O			X50.9	= 9
+5V		O			X50.10	=10
DFSR0		O		CMOS	X50.11	=11 ser. SN to
DDR0		O		CMOS	X50.12	=12 DSP D
CLKR0		O		CMOS	X50.13	=13
GND		O			X50.14	=14
RESETD		O		CMOS	X50.15	=15 Reset DSP D
+5V		O			X50.16	=16
DDSPCLK	Clock of DSP	O		CMOS	X50.17	=17
GND		O			X50.18	=18
LINKA2	Link addr. D	O		CMOS	X50.19	=19
LINKA3		O		CMOS	X50.20	=20
SYNC	Audio Req.	B		CMOS	X50.21	=21
GND		O			X50.22	=22
FSXG	Link, G	O		CMOS	X50.23	=23
CLKXG		O		CMOS	X50.24	=24
TXDG		O		CMOS	X50.25	=25
FSXD	Link, D	I		CMOS	X50.26	=26
CLKXD		I		CMOS	X50.27	=27

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
TXDD				CMOS	X50.28	=28
+5V		O			X50.29	=29
FSXB	Link, B			CMOS	X50.30	=30
CLKXB				CMOS	X50.31	=31
TXDB				CMOS	X50.32	=32
FSXA	Link, A			CMOS	X50.33	= 33
CLKXA				CMOS	X50.34	= 34
TXDA				CMOS	X50.35	= 35
GND		O			X50.36	= 36
CLOCKDI				CMOS	X50.37	= 37
+12V		O			X50.38	= 38
-12V		O			X50.39	= 39
n.c.					X50.40	= 40

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Internal interface to Analog Generator (GENCONN)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X30.8,12,16	
VCC		O			X30.10,13	
IAICLK	Clock	O		CMOS	X30.4	
IAIDI	Data in			TTL	X30.3	
IAIDO	Data out	O		CMOS	X30.5	
IAIWR	Write	O		CMOS	X30.6	
IAIRD	Read	O		CMOS	X30.2	
WREN		O		CMOS	X30.1	
GENINT				TTL	X30.7	
GCLK	Clock	O		CMOS	X30.15	
GD0	Data out	O		CMOS	X30.11	
GD1	Data out	O		CMOS	X30.9	
GFSX	Frame Sync	O		CMOS	X30.13	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Internal interface to Connector Board/Keyboard (26-contact flat cable, top)						
name	Signal description	≡	source dest.	range	connector	comment
GND		O			X90. 1	
+5V		O			X90.26	
Row0	Keyboard	B			X90.23	
Row1		B			X90.24	
Row2		B			X90.21	
Row3		B			X90.22	
Row4		B			X90.19	
Row5		B			X90.20	
Row6		B			X90.17	
Row7		B			X90.18	
Col0		B			X90.13	
Col1		B			X90.14	
Col2		B			X90.11	
Col3		B			X90.12	
Col4		B			X90.9	
Col5		B			X90.10	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
Col6	LED	B		Ri 1.5Ω	X90.7	
Col7		B			X90.8	
PIO0		B			X90.3	
PIO1		B			X90.4	
PIO2		B			X90.5	
PIO3		B			X90.6	
PIO4	B	X90.2				
PIO5	B	X90.25				
RMK1	Rotary knob	I			X90.15	
RMK2		I			X90.16	
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

Internal interface to Digital Analyzer (DSPLINK) (16-contact flat connector, top)						
name	Signal description	≡	source dest.	range	connector	comment
GND	Link A	O	all DSPs	CMOS	X70. 1	
TXDA		B			X70. 2	
CLKXA		B			X70. 3	
FSXA	Link B	B	all DSPs	CMOS	X70. 4	
TXDB		B			X70. 5	
CLKXB		B			X70. 6	
FSXB	Link D	B	all DSPs	CMOS	X70. 7	
TXDD		B			X70. 8	
CLKXD		B			X70. 9	
FSXD	Link G	B	all DSPs	CMOS	X70.10	
TXDG		O			X70.11	
CLKXG		O			X70.12	
FSXG	33.5 MHz	O	all DSPs	CMOS	X70.13	
LDSPCLK		B			X70.14	
SYNC		B			X70.15	
CLOCKDI	AES clock	E	DSP D	CMOS	X70.16	betw.D and G clock meas.
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

7.4.5 AES/EBU (Option UPD-B2)

Circuit diagram	1031.2399.01 S
Component location plan	1031.2399
Parts list	1031.2399.01 SA

Diagram overview	
Sheet:	Contents
1/12:	Block diagram
2/12:	Connectors
3/12:	DSP CPU, wait state logic
4/12:	SERPA, external bus, control register, parity hardware
5/12:	Output level setting
6/12:	Input amplifier, input multiplexer and link of DSP
7/12:	DSP memory, fast and slow, small version, R/W decoder
8/12:	External ROM code (not fitted)
9/12:	DSP memory, fast and slow, large version
10/12:	Clock recovery
11/12:	Clock synchronization
12/12:	AT-bus assignment

7.4.5.1 Function

The option AES/EBU - S/P-DIF (in the following and elsewhere only referred to as AES/EBU) is plugged into the PC mainboard (industrial standard AT) installed in the UPD. The slot is only used for mechanical fastening and for current supply, all control and communication lines are routed via the 40-contact connector DG-CONN.

The board accommodates the input amplifier circuit, the clock recovery, the output amplifier with level setting and the DSP for analysis and generation including the associated memory.

- Input circuit (INPUT CIRCUIT, circuit diagram sheet 6)

Three different inputs are provided:

- AES-EBU:

The signal is taken from the front panel (XLR connector) via flat cable W51 (pins 8 and 9) to the input transformer T60. The input impedance is approx. $10k\Omega$ for monitor measurements on terminated lines. For standardized termination measurements, relay K60 connects a 110Ω resistor in parallel. Amplifier N60 attenuates the signal by 6 dB before it is set to TTL level in the following comparator (U60) with a threshold of approx. $50mV_{pp}$. Integrator (N61-A) with a very large time constant stabilizes the opamp N60, because there is no negative feedback of the DC voltage because of the transformer.

- S/P DIF:

The signal is taken from the front panel (BNC connector) via the coax cable W512 to the input comparator (U61) with a threshold of approx. $50mV_{pp}$ and then to the input multiplexer (D60).

- OPTICAL:

At the output of the optical receiver (system TOSLINK, on the Adapter Board), a TTL signal is provided, which is directly applied to the input multiplexer (D60) via flat cable W51 (Pin 4).

- Clock recovery (sheet 10)

The AES-EBU-coded data signal (AES-DR0) is applied to an EXOR chain with incorporated RC-sections. Each edge transition at the input causes an about 20-ns wide negative pulse at the output of the last EXOR.

These pulses are applied via R106 and C112 to transistor V100, which triggers an LC resonant circuit (consisting of L100, C115 to C118). Its output is conditioned by comparator U100 to form the receive clock AES-CLKR0. The resonant circuit bridges the time during which no pulses are applied to the input (e.g. during a preamble).

In order for the frequency of the resonant circuit to correspond exactly to the bit rate at 32, 44.1 or 48 kHz, the resonant frequency of the circuit is matched by 2 selectable capacitors C116 and C117.

To this end, the output pulses of the EXOR are also applied to a non-retriggerable digital monoflop (pulse width 230 ns). One pulse sets flip-flop D105; this causes a 1 to be shifted through the two shift registers D103 and D104 and the complete logic to be reset finally. Further pulses at the input only set the (already provided) 1. By means of this monoflop, exactly one output pulse is generated for each input bit, irrespective of whether a 0 (only one edge transition) or a 1 (two edge transitions) is applied to the input.

The output pulses of the monoflop (D103, pin 3) are smoothed by an RC section after buffer amplifier D102 and compared with fixed threshold values. The control signals for switching the resonant circuit are thus derived.

- Clock synchronization (sheet 11)

The PLL (D112) can be operated with different command inputs and feedback signals depending on the desired clock source.

In the operating mode EXTERNAL, the BNC connector on the rear panel is selected (LS6 = low). In this case, the feedback is accomplished via a 128-fold divider in order for the PLL to oscillate at the bit clock frequency.

In the operating mode SYNCHRONOUS, the recovered input clock is used (LS6 = high). The feedback is not divided in this case.

In both external cases, D61 switches the output clock to the SERPA, line AES-CLKX.

The output clock is also taken to the connector (CLOCKDI, see also clock rate measurement, page 6.11).

- Output circuit (OUTPUT LEVEL CONTROL, block diagram sheet 5)

The digital audio signal AES-DX0 from the SERPA is processed according to the output selected and taken to the front panel. The other outputs are deactivated.

- AES/EBU und S/P DIF:

The signal is taken via buffer D41-D and jumper X52 to the inputs of the NOR gates D50 and D54. The data lines LD0...LD7 switch the input signal via the binary-coded resistors R500...R524 to the opamp N52 with a gain of 6dB. The output voltage of N52 (test point P51) can thus be set with a resolution of 8 bits:

$$\begin{aligned} 1\text{LSB} &\hat{=} 40\text{mV}_{pp} \\ V_{max} &\hat{=} 10.24\text{V}_{pp} \end{aligned}$$

After the output transformer, relay K50 switches either to the AES/EBU or to the S/P DIF output:

AES/EBU	Source impedance 110Ω Sym. cable W511 to XLR connector on the front panel $V_{pp} = 5.12V \dots 20mV$ with 110Ω termination
S/P DIF	Source impedance 75Ω Coax cable W510 to BNC socket on the front panel (The center tap of T50 is the ground) $V_{pp} = 2.56V \dots 10mV$ with 75Ω termination

– OPTICAL:

The signal is taken via a driver (D100-B, switched by LS7 of the control register) and flat cable W51 to the Adapter Board, where the optical transmitter (System TOSLINK) is located.

- Word clock output (sheet 5)

The BNC connector on the rear panel is supplied with a squarewave output signal, whose frequency is equal to the sampling rate. In order to synchronize this signal with the left-right sequence, the clock signal AES-FXS0 is controlled with AES-LR and then applied to the BNC connector X500 via an output driver.

- DSP

The ROM code version of the TMS 320C30 is used as DSP. The DSP features a cycle time of 60 ns and operates with 32-bit floating numbers (not IEEE-compatible, however is converted by the access routine in the DSP when writing and reading DSP addresses).

The DSP is provided with 4 interrupt inputs which are assigned as follows:

INT0:	Gate array SERPA (thus used both for transmission and reception)
INT1:	not used
INT2:	not used
INT3:	not used

- DSP memory

The complete memory is at the primary bus, consisting of 2 banks with different access times.

The address A21 is inverted and fed back to the /READY input, i.e. all addresses $N * (2^{22}) + x$ with $x < 2^{22}$ are addressed with 0 wait states.

Address:	Memory area
000000-00FFFF:	2 WS via hardware logic: EPROM (This hardware logic is normally not fitted; if the EPROM is fitted, the wait state logic must be fitted and jumper X9.6 (ROM) plugged in)
200000-207FFF:	0 WS via A21 feedback: FAST SRAM (25ns): Code and data
400000-407FFF:	2 WS via software: SLOW SRAM (85ns): only data

Bus programming:

Software wait states and hardware ready; the wait state logic is only required if the EPROMs are fitted.

- DSP ports

Address:	Signal	Port
8000x0-8000x7:		Gate array SERPA
800400:	ECSWRTP:	WR parity logic
800400:	BIDRD:	RD board ID and parity result
800401:		WR level setting (8 bit DAC)
800402:		WR control register

Control register (Port 800402)	
Bit:	Meaning
LS0-2	Input multiplexer: 0 = AES/EBU 1 = S/P DIF 2 = OPTICAL 3 = E-DRO; 4 = E-DX0 (only for test) 5,6,7 = not used
LS3	Clock enable for external clock
LS4	Input impedance
LS5	Output selection: 0 = AES/EBU; 1 = S/P DIF
LS6	Output synchronization 0 = external word clock; 1 = Input
LS7	Enable optical output

Note: The gate array SERPA is driven with 0 wait states via hardware ready (MSB of the address). Because of the somewhat *strange* interrupt input connection of the C30 and because of an internal fault in the C30, the interrupt output of the SERPA is followed by a pulse generation circuit. It generates a pulse for each newly occurring interrupt. If the logic is reset with IACK and there is still an interrupt, a new pulse is generated. These pulses are synchronized with H1 of the CPU.

- Parity logic and board identification (sheet 4):

Since the C30 does not have a parity command or parity status, the parity check and generation is implemented with an external logic circuit (consisting of the devices D401 - D405). The result (equal to logic 1, if the input parity is EVEN) can be read in as bit 7 into the board ID register (addr. 0800400H).

The board identification is coded with resistors, the LSB being reserved for a different version.

- Internal digital link

All DSPs in the UPD are connected with each other via a four-way serial link. Each DSP is assigned a transmission line and can switch its input to all other transmission lines (including its own) via a multiplexer. In addition, a SYNC line can be set and read by all DSPs (see page 6.15).

- Jumper settings:

Jumper	Inscription	inserted
X52.1 - X52.2	I	yes

7.4.5.2 Measuring Instruments

Emulator XDS500 (PC plug-in card and software)

Voltmeter

Oscilloscope, bandwidth > 150MHz

7.4.5.3 Troubleshooting

On occurrence of the following error messages, proceed as follows:

- Status message (in OPTION panel) AES/EBU -NA- (not available)
 - Check the detection line: Manual reading (e.g. via debugger) of the port address AB90H (test register of the SERPA): Bit 5 must be low. (Otherwise check connection cable).
 - New hardware on old software (which identifies the read board identification as invalid).

- Can't boot DSP . .

This fault may be due to a variety of causes.

- Fault in the AT SERPA: When a boot attempt is made, signals must arrive on line DRO on the DSP. (similar to RS232). The DSP must respond by sending a signal on line DX0.
 - Fault when writing to control register (D612 and D613). The control register must always be enabled after the program start (OUTEN, pin 1 applied to LOW). Check the lines RESETD and HOLD of the respective DSP. (see boot procedure, page 6.7)
 - Fault in clock supply on AT side: 14.318 MHz must be applied to SERPA D2, pin 55 (FREQ 2). (In this case, the DSP G cannot be booted either.)
 - Fault in clock supply on DSP side: 33.4 MHz with a deviation of 4 volts must be applied to DSPCLK (pin 16). Otherwise check jumper X22.
 - Fault in DSP or DSP memory: For further diagnosis, an XDS 500 must be connected to the emulation connector.
- No AES/EBU output signal
 - Check the output multiplexer and the signal before the multiplexer (AES-DX0).
If the signal is already missing there:
 - * Check the clock signals at the SERPA.
 - * Check the input INTO of the DSP and the interrupt output of the SERPA;
 If there is a signal at the output multiplexer:
 - * Check the level setting (Caution: control bits of D/A converter are inverted)
 - * Check the connection cables (10-contact, 4-contact and coax) to the front panel.
 - The generated signal features a very poor S/N on the digital interface, in particular harmonics and/or white spectrum can clearly be seen.

- A bit on the port or expansion bus of the DSP *got stuck*. The best thing to do is to set a non-subharmonic, fully driven sinewave signal and check whether each bit „flips“.
- Faulty samples are generated; check the clock signals for correct level and transfer edge.
- Check the SYNC line (see page 6.15).
- Check the Digital Generator

7.4.5.4 Testing and Adjustment

1. DSP, Interface

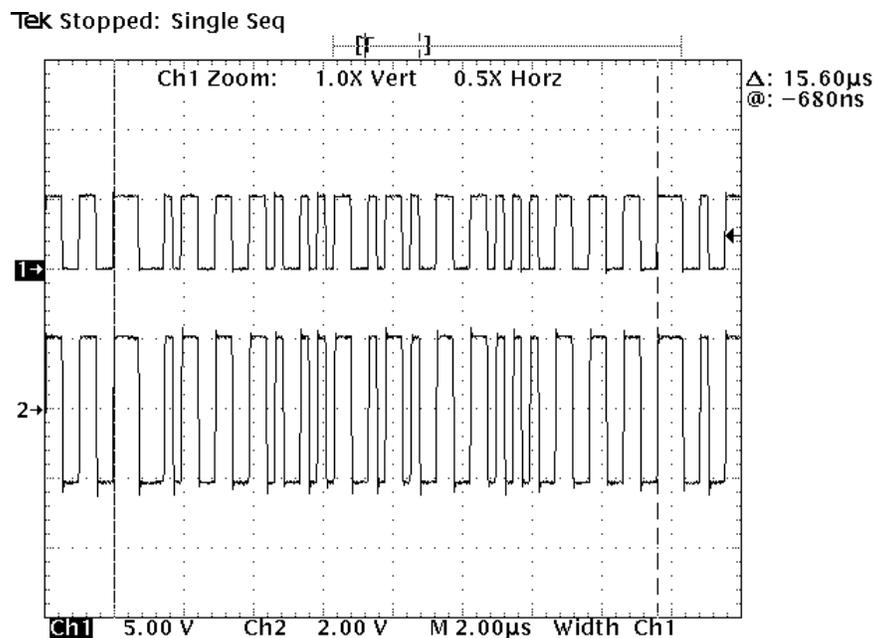
The DSP with the memory and the AT interface are checked using the built-in selftest routine. The levels and waveforms of the digital outputs as well as the clock generation and recovery are to be checked according to section 7.4.1 Testing the Rated Specifications, page 7.221.

2. OUTPUT LEVEL CONTROL

(circuit diagram sheet 5)

Generator setting	Instrument	DIG 48kHz
	Channel(s)	1
	Output	S/P DIF
	Sample Freq	32kHz
	Audio Bits	20
	Dig. Vpp	1.000 V
	Max Volt	1.000 FS
	Ref Freq	1000.0 Hz

- Testing the operating voltage for D50, D54
DC measurement at P50: 5V ± 0.25V
- Output signal AES-DX0 from SERPA D40.64



Trace1: AES-DX0 signal at X52

Trace2: same signal at P51

The two vertical cursor marks are each positioned to the beginning of a preamble, the information for a channel lies in-between.

The preambles arrive at intervals $\Delta t = 15.6\mu s$.

$$\frac{1}{2 * 15.6\mu s} = 32kHz = SampleFreq$$

- Testing the output switchover

Set the outputs according to the table in the generator panel and measure at the indicated test points (accuracy of oscilloscope is sufficient).

Generator Output	ADR 800402H, D406		Output	Test point	Signal
	LS	Bit			
OPTICAL	7	0	OPT on	X51.1	TTL
	7	1	OPT off	X51.1	0V
AES/EBU	5	0	AES/EBU on	X511.1 .2	$1V_{pp}$
			S/P DIF off	X510	0V
S/P DIF	5	1	OPT off	X51.1	0V
			AES/EBU off	X511.1 .2	0V
			S/P DIF on	X510	$2V_{pp}$
			OPT off	X51.1	0V

The signal voltages at the outputs AES/EBU and S/P DIF apply to open circuit.

- Testing the level setting at the output S/P DIF

The voltage Dig. V_{pp} at the output S/P DIF applies to termination with a nominal impedance of 75Ω (connect output to input).

Prior to the measurement, the output voltage must be adjusted:

- Set Dig. $V_{pp} = 1.000V$
- Use R526 (accessible from the top through the screening panel) to adjust the voltage at the output S/P DIF to the nominal value!

Dig. V_{pp} / mV	ADR 800401H Latch D407
1280	0111 1111
1000	1001 1011
640	1011 1111
320	1101 1111
160	1110 1111
80	1111 0111
40	1111 1011
20	1111 1101
10	1111 1110

- Testing the Impedances

Set the generator output according to the table:

Measure voltage at the indicated test point without/with load. The load can be produced, e.g., by connecting the respective input in parallel via a T-junction.

The accuracy of an oscilloscope is sufficient for the measurement.

S/P DIF Measurement at X510 or at the BNC connector on the front panel
 - Open circuit: → reference
 - 75Ω load: -6dB

AES/EBU Measurement at X511.1 and .2 or at pin 2 and 3 of the XLR connector on the front panel
 - Open circuit: → reference
 - 110Ω load: -6dB
 (Measurement against ground, connect the ballast resistance symmetrically **between** the pins)

3. INPUT CIRCUIT

(circuit diagram sheet 4)

Analyzer setting	Instrument	DIG 48kHz
	Channel(s)	1
	Input	AES/EBU
	Ch1 Imped	110Ω
	Sample Freq	32kHz
	Audio Bits	20
	Dig. Vpp	1.000 V
	Max Volt	1.000 FS
	Ref Freq	1000.0 Hz

The output signals can be used as test signals (it may be necessary to check the outputs before).

- Input AES/EBU

Generator setting: Output AES/EBU with Dig.Vpp = 2.5V

Connect output to input, set Ch1 Imped according to the table and measure the voltage at the indicated test points:

Test point	Ch1 Imped	
	$10\text{k}\Omega$	110Ω
X51.8 .9	$2.50V_{pp}$	$1.25V_{pp}$
P60	$2.75V_{pp}$	$1.375V_{pp}$
P62	TTL	TTL
D60.6	HCMOS	HCMOS

Testing the input sensitivity:

Dig.Vpp = 100mV ⇒ TTL at P62

Dig.Vpp = 20mV ⇒ no signal (1 or 0)

≈21mV DC at U60.4

- Input S/P DIF

Generator setting: Output S/P DIF with Dig.Vpp = 1.0V

– Measure output voltage: → reference

– Connect input in parallel via T-junction: ⇒ output voltage -6dB

– at P61 TTL

– at D60.6 HCMOS

Testing the input sensitivity:

Dig. $V_{pp} = 100\text{mV} \Rightarrow$ TTL at P61
Dig. $V_{pp} = 20\text{mV} \Rightarrow$ no signal (1 or 0)
 $\approx 21\text{mV DC}$ at U61.4

- Input OPTICAL
Generator setting: Output OPTICAL
 - Connect output to input
 - at X51.4 TTL
 - at D60.6 HCMOS

7.4.5.5 Disassembly and Assembly

After opening the instrument, remove the bracket above the digital section and unscrew the clip at the rear.

Remove the cable to the generator (40-contact) and the connections to the front panel.

7.4.5.6 External Interfaces

Internal interface to Generator (DG-CONN)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X50.1	= 1
FREQ	49.152 MHz		DigGen	CMOS	X50.2	= 2 Audio clock
+5V					X50.3	= 3
FREQ1	67.56 MHz		DigGen	CMOS	X50.4	= 4 Audio clock
GND					X50.5	= 5
DDX0	to AT	O	DigGen	CMOS	X50.6	= 6 ser. SN from
DFSX0		O	DigGen	CMOS	X50.7	= 7 DSP D
DCLKX0		O	DigGen	CMOS	X50.8	= 8
GND					X50.9	= 9
+5V					X50.10	=10
DFSRO	from AT		DigGen	CMOS	X50.11	=11 ser. SN to
DDRO	Pulldown			CMOS	X50.12	=12 DSP D
CLKR0				CMOS	X50.13	=13
GND					X50.14	=14
RESETD			DigGen	CMOS	X50.15	=15 Reset DSP D
+5V					X50.16	=16
DDSPCLK	Clock off DSP			CMOS	X50.17	=17, 33.5 MHz
GND					X50.18	=18
LINKA2	Link addr.D		DigGen	CMOS	X50.19	=19
LINKA3				CMOS	X50.20	=20
SYNC	Audio Req.	B	all DSP	CMOS	X50.21	=21
GND					X50.22	=22
FSXG	Link, G		DigGen	CMOS	X50.23	=23
CLKXG				CMOS	X50.24	=24
TXDG				CMOS	X50.25	=25
FSXD	Link, D	O	all DSP	CMOS	X50.26	=26
CLKXD		O		CMOS	X50.27	=27
TXDD		O		CMOS	X50.28	=28
+5V					X50.29	=29
FSXB	Link, B		DigAna2	CMOS	X50.30	=30
CLKXB				CMOS	X50.31	=31
TXDB				CMOS	X50.32	=32
FSXA	Link, A		DigAna	CMOS	X50.33	= 33
CLKXA				CMOS	X50.34	= 34
TXDA				CMOS	X50.35	= 35
GND					X50.36	= 36
CLOCKDI	approx. 3 MHz	O	PFC	CMOS	X50.37	= 37, clock rate
+12V			AT		X50.38	= 38
-12V					X50.39	= 39
n.c.					X50.40	= 40

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Expansion connector (EXPCONN)						
name	Signal description	≡	source dest.	range	connector	comment
E-CLKR	Clock			CMOS	X30.2	
E-FSR	Frame in			TTL	X30.4	
E-DR1	Data in		InMux	CMOS	X30.5	
LS7	Control bit	O		CMOS	X30.7	
E-DX0	AES_out	O		CMOS	X30.8	
E-DR0	AES_in			CMOS	X30.9	
AES_CLKR0	AES-Clkin			TTL	X30.10	
AES_CLKX	Clock	O		CMOS	X30.12	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
TCLK0	Control bit	B		CMOS	X30.13	
AES_DX1	Data out	O		CMOS	X30.14	
AES_FSX1	Frame Sync	O		CMOS	X30.15	
GND		O			X30.1,11,16	
VCC		O			X30.3	
n.c.					X30.6	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

BNC connectors rear						
name	Signal description	≡	source dest.	range	connector	comment
WRDCLK	IN	I	external	TTL	X110	
WRDCLK	OUT	O	external	TTL	X500	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Connection to front panel						
name	Signal description	≡	source dest.	range	connector	comment
AES/EBU	bal, max. 3.072 MHz	I		100mV _{pp} ... 10V _{pp}	X51.8,9	
GND	Shielding	P	AESEBU		X51.7,10	
Opt In		O		TTL, max 3.072MHz	X51.4	
Opt Out		O		TTL, max 3.072MHz	X51.1	
GND		P	AESEBU		X51.3,6	
+ 5 V		I		+5V ±0.2V	X51.2,5	
Unbal In	S/P DIF In, max. 3.072 MHz	I		100 mV... 5 V	X512.1	
GND		P	AESEBU		X512	Shield
AES/EBU	bal, max. 3.072 MHz	O		100mV _{pp} ... 10V _{pp}	X511.1,2	
GND		P	AESEBU		X511.4	
—	Connector coding		AESEBU		X511.3	
Unbal Out	S/P DIF Out, max. 3.072 MHz	A		100 mV... 2 V	X510.1	
GND		P	AESEBU		X510	Shield

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.5 Digital Boards DSP

7.5.1 Monitor Output (Option UPD-B5)

Circuit diagram	1031.5300.01 S
Component location plan	1031.5300.01
Parts list	1031.5300.01 SA

Circuit Diagram Overview	
Sheet:	Contents
1/8:	Block diagram
2/8:	Parallel port
3/8:	Level setting, filter, phones and loudspeaker output
4/8:	Stereo D/A converter, analog inputs
5/8:	Register for hardware control
6/8:	FIFO register, PLL clock conditioning
7/8:	Serial/parallel registers A and B
8/8:	DSP LINK inputs, switchover

7.5.1.1 Function

The Monitor Output board is inserted into the PC mainboard (industry standard AT) mounted in the UPD. Via the AT plug-in location, the board is supplied with current and controlled by the main processor for the individual modes. Digital DSP link signals are applied to the board via the 16-contact connector X3, the analog monitor signals are applied via the two inputs X5 and X6. These monitor signals as well as the D/A-converted DSP link signals can be monitored with this board using external phones or the internal loudspeaker. Besides, the board contains a complete parallel port for controlling an external signal source switcher.

- Digital inputs, DSP link switchover (DSP Link Input, circuit diagram sheet 8)

DSP link inputs:

- DSP LINK A and DSP LINK B:

The digital analyzer output signal is taken via DSP link A and B to the Monitor Output board. The FUNCTION RMS & S/N permits to monitor the measured or filtered signal. If no High Speed Option is installed in the UPD, the digital output signal is always sent from the analyzer via DSP link A (Ch1 or Ch2), with the High Speed Option fitted, CH1 is sent via DSP link A and Ch2 via DSP link B, allowing for stereo reception. On the average, the sampling rate of both link channels corresponds to the sampling rate set on the UPD or applied to the test input (30 kHz ... 50 kHz).

- DSP LINK D:

The digital analyzer input signal from the AES/EBU board is transmitted via this DSP link. DSP link D is used if the signal is to be monitored at the digital input. Both channels (left and right) are transferred in multiplex operation. The average sampling rate is twice the sampling rate set on the UPD or applied to the digital input.

DSP LINK switchover:

The individual DSP link signals are applied via input buffers D11, D12, D13 and D5 to multiplexers D7, D8, D9 and D10. Via these multiplexers, the desired DSP link channel is

connected to the following serial/parallel registers. The multiplexer is controlled by latch D2 (see sheet 5).

- Serial/parallel registers A and B (Circuit diagram sheet 7)

The two registers A and B consist of the cascaded 8-bit shift registers with integrated latch (D46, D47, D48, D49 or D40, D42). They convert the serial DSP link signals into parallel data for the following FIFO registers. Register A features a memory depth of 32 bits, register B 16 bits. The 16 most significant bits of the DSP data words are used for the following FIFO registers. The shift registers D39, D43, D44 and D45 or D50 and D41 are used to delay the strobe of the DSP link frame signals, as, at the link inputs, the frame signal is sent prior to the serial data. If the data input is switched to DSP link D, the LSB of the 32-bit data word contains the information on whether the data word belongs to the left or right channel. In the case of the left channel, the LSB is set (high).

- FIFO registers, PLL clock recovering (FIFO, PLL, circuit diagram sheet 6)

The two FIFO registers D16 and D17 enable synchronous data output of the sampled values applied at the DSP link input asynchronously. The readout clock of the serial FIFO data is generated by a PLL that is connected to the input sampling rate of the FIFOs. The PLL mainly consists of device D20; the active loop filter is implemented by means of N7. Relay K1 is used to switch the VCO range according to the input sampling rate. The clock signals for the subsequent D/A converter and for the readout logic of the FIFO data are derived from divider D21. The two flip-flops of device D18 enable a defined start of readout when a quarter of the FIFO is filled (AEF output of the FIFO). Multiplexer D19 is used to combine the data of both FIFOs to a single data stream for the stereo D/A converter. The subsequent D/A converter is operated by a master clock featuring 256 times the frequency of the sampling rate at the input. The bit clock for the serial data is 32 times the sampling rate, the LR clock corresponds to the frequency of the sampling rate. Depending on the logic level of the signal, the data word is used for the left or right D/A converter output.

- Stereo D/A Converter, Analog Input (circuit diagram sheet 4)

The D/A converter D6 is a highly integrated device, in which two complete converter paths with digital and analog filter are integrated. The D/A conversion is performed according to the DELTA/SIGMA procedure with simultaneous digital filtering and subsequent analog filtering of the internal sampling frequency. Thus, the necessary circuitry is reduced to a minimum. The D/A converter uses 16 bits in this case. The two RC networks R17/C21 and R18/C22 are used for suppression of the internal sampling frequency, which is 64 times the word rate. The D/A converter is supplied with ± 5 volts via the two voltage regulators N2 and N6. The analog output signals of the converter are applied to the analog switch D1. This switch is used to switch the monitor output between the analog channels and digital monitoring operation. The two resistor dividers R14/R20 and R19/R21 permit to match the level of the input signals. Besides, analog switch D1 at the input of the two opamps N1 is used to switch the monitor output between mono and stereo in analog monitor operation. Mono mode means that either channel 1 or channel 2 is output to both phones.

- Filter, level setting, phones and loudspeaker output (OUTPUT, circuit diagram sheet 3)

The two analog signals (left and right) from switch D1 are taken to the reference inputs of the multiplying D/A converters D25 and D26. These two D/A converters are used for volume setting of the output signal. The lowpass filter at the output ensures additional noise suppression in particular of the stereo D/A converter signal components exceeding the audible

range. The two volume D/A converters are controlled by means of the 8-bit register D3 (sheet 5). The outputs of the two D/A converters operational amplifiers D27 and D28 are taken via an RF filter to phones connector X8. The output impedance of the phones output is determined by the resistors R78/R84 or R96/R104. With the phones connected, the internal loudspeaker is usually switched off. Analog switch D51 permits the internal loudspeaker to be operated in parallel with the connected phones and switched on/off irrespective of the phones (Phone OUT PERMANENT or SPK CONFORM).

- Register for hardware control (CONTROL, circuit diagram sheet 5)

The complete control of the monitor output is effected with registers D2, D3 and D4. Register D2 features the AT-bus address 678hex and controls the selection of the DSP link to be switched to registers A and B and to the FIFO memories. Register D3 features the AT-bus address 679H and controls the volume of the monitor output. Register D4 features the AT-bus address 67AH and controls additional hardware signals and the switchover between digital-monitor and analog-monitor operation.

- Parallel Port (PARALLEL PORT, circuit diagram sheet 2)

The Parallel Port on the board is used for controlling an external switcher with the UPD via the 25-contact connector X2. This connector provides data and control lines, which permit a connected switcher to be detected and controlled. Registers D34 and D36 as well as the input drivers D30, D35 and D37 are used for control. They are addressed by means of the AT-bus addresses 278H, 279H and 27AH. The devices D29, D31 and D38 are used for address decoding of the board.

7.5.1.2 Measuring Instruments and Auxiliary Means

DC voltmeter

AC voltmeter

Distortion meter

Oscilloscope

Adapter cable 6.3mm stereo jack plug on 2x BNC connector (female)

600Ω feed-through terminations 2 pcs

7.5.1.3 Troubleshooting

In the case of errors at the monitor output, proceed as follows:

- No output signal at the monitor output in the operating mode Analog Analyzer SPEAKER INPUT
 - Check the set volume; loudspeaker on?
 - Check analog input signals at X5 and X6. Standard level $3V_{rms}$
 - Check analog signals at opamp outputs test points P3 and P4. Maximum level $4V_{pp}$
 - Check signals of the D/A converter outputs D25 and D26 at P5 and P6
 - Check analog signals at filter outputs at P13 and P14
 - Check loudspeaker amplifiers N5, V10, V13, V19, V14
- No output signal in the operating mode Analog Analyzer 22 kHz SPEAKER FNCT

- Check the set volume; loudspeaker on?
 - Check PRE GAIN setting. This also determines the volume at the output. Standard setting 0 dB
 - Check signals of D/A converter D6 at P3 and P4
 - Check digital signals LRCLK, BICK, SDATA and XT1 at D/A converter input at P7, P8, P9 and P10.
 - Check reference frequency signal for PLL at P1.1. Signal frequency corresponds to set sampling frequency.
 - Check DSP LINK signal at multiplexer outputs D7.7, D7.9 and D8.7 or at the outputs D9.7, D9.9 and D10.7. The signals must correspond to the signals at the DSP link A or DSP link B inputs at connector X3.
- No output signal in the operating mode Digital Analyzer 48 kHz SPEAKER AES
 - First check the board in the operating mode Analog Analyzer 22kHz SPEAKER FNCT. see above.
 - Check reference frequency signal for PLL at P1. Signal frequency corresponds to sampling frequency.
 - Check DSP LINK signals at multiplexer outputs D7.7, D7.9 and D8.7 or at the outputs D9.7, D9.9 and D10.7. The signals must correspond to the signals at the DSP Link D input at connector X3. Frame sync frequency of DSP Link D corresponds to twice the sampling frequency.
- Disturbed output signal at the monitor output in the operating mode Digital Analyzer or Analog Analyzer 22 kHz SPEAKER FNCT
 - First check the respective signal path according to the above error list: no output signal
 - Check the VCO control voltage at P2: Level range 1V...4V DC.
 - Check the VCO_Range switchover at D4.6 by varying the sampling frequency on the UPD Analyzer between 32 kHz and 48 kHz
 - Check the reset function for the D/A converter and FIFO at control latch D4.2 when changing e.g. speaker signal sources
 - Check the sampling frequency at P1

7.5.1.4 Testing and Adjustment

The board does not require any adjustment. It is to be checked only for proper functioning. To meet particular requirements placed on the level accuracy and the synchronism of the two monitor outputs left and right, optional trimmers are provided in the layout of the board.

1. Monitor Output at Analog Analyzer Input

(Circuit diagram sheet 3 and sheet 4)

In this operating mode, the complete analog section of the monitor output is checked. To this end, a sinewave signal with a standard level of 3 V_{rms} produced by corresponding settings of the UPD generator and analyzer must be applied to the two analog inputs X5 and X6. Connect the generator outputs and analyzer inputs. Connect adapter cable to phones output X8. The monitor output (Phone OUT) can be switched to PERMANENT for measurements. The LOCAL key thus only switches off the internal loudspeaker. The monitor output is measured at the BNC connectors of the adapter cable. The two 600Ω feed-through terminations are used as load resistors.

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	1 & 2
	Output	UNBAL BNC
	Function	SINE
	Frequency	1000.0 Hz
	Voltage	3.0000 V

Analyzer setting	Instrument	ANLG 22kHz
	Channel(s)	1 & 2
	Ch1 Input	UNBAL BNC
	Ch2 Input	UNBAL BNC
	Function	RMS & S/N
	Filter	OFF
	Speaker	INPUT Ch1&2
	Spk Volume	100

- Check the signal levels at the analog inputs X5 and X6. If necessary, adjust to the required value with generator level.
AC measurement at X5 and X6: $V_{rms} = 3V \pm 0.01V$ at 1kHz
- Check the signal levels at monitor output left and right with 600Ω termination
AC measurement X8.1 (left) and X8.2 (right) with BNC adapter cable for monitor output:
 $V_{rms} = 5.66V_{rms} \pm 0.3V$ at 1kHz
- Check the frequency response at monitor output left and right with 600Ω termination when varying the generator frequency in the frequency range 20 Hz ... 20 kHz
AC measurement at X8.1 and X8.2 (BNC adapter cable for monitor output): frequency response referred to 1kHz : 0dB +0.2dB, -0.3 dB
- Check the volume setting
Vary the volume and check for monotony of the level at the monitor output.

2. Operating mode Analog Analyzer 22kHz Function

(Circuit diagram sheets 8, 7, 6 and 4)

In this operating mode, the digital signal processing and the stereo D/A converter of the board are checked. The digital signals from DSP link A or DSP link B are used as signal sources in this operating mode. DSP link B is only active if the High Speed Option is installed.

Generator setting	Instrument	ANLG 25kHz
	Channel(s)	1 & 2
	Output	UNBAL BNC
	Function	SINE
	Frequency	1000.0 Hz
	Voltage	1.0000 V
Analyzer setting	Instrument	ANLG 22kHz
	Channel(s)	1
	Channel(s)	2 *)
	Channel(s)	1 & 2 **)
	Ch1 Input	UNBAL BNC
	Ch2 Input	UNBAL BNC
	Function	RMS & S/N
	Filter	OFF
	Speaker	FNCT Ch1
	Speaker	FNCT Ch2 *)
	Speaker	FNCT Ch1&2 **)
	Pre Gain	0 dB
Spk Volume	100%	

*) for checking channel 2, **) for checking with High Speed Option

3. Check the signal levels at monitor output left and right with 600Ω termination

Check switchover between Ch1, Ch2 or Ch1&2 and signal level at output

AC measurement at X8.1 (left) and X8.2 (right) with BNC adapter cable for monitor output:
 $V_{rms} = 5.66V \pm 0.3V$ at 1kHz generator frequency

The frequency response of the stereo D/A converter in the range up to 20 kHz can be neglected and need therefore not be tested separately.

Note:

If the two monitor outputs left and right are to be adjusted accurately, the two trimmers R82 and R102 are to be fitted. The two resistors R83 and R103 are omitted in this case. The output amplitudes left and right are to be adjusted to $V_{rms} = 5.66V$ using R103 or R83.

4. Check the spectral purity of the monitor output with 600Ω termination

Connect distortion meter or spectrum analyzer with high-impedance input to the two channels of the monitor output. Measure the distortion factor at generator frequencies up to 20 kHz

Distortion measurement at X8.1 (left) and X8.2 (right) with BNC adapter cable and 600Ω termination:

Distortion (THD+N) in the range 20 Hz ... 20 kHz better than 1.0%
 (THD only) in the range 20 Hz ... 20 kHz better than 0.1%

5. Operating mode Digital Analyzer 48kHz Speaker AES (only with AES/EBU Option)

In this operating mode, the AES/EBU signal source for the monitor output is checked. The data from DSP link D are used as internal signal source. This DSP link is only active with

the AES/EBU Option installed. Connect the generator output S/P DIF to the analyzer input S/P DIF.

Generator setting	Instrument	DIG 48kHz
	Channel(s)	1 & 2
	Output	S/P DIF
	Sample Frq	48 kHz
	Function	SINE
	Frequency	1000.0 Hz
	Voltage	1.0000 FS
Analyzer setting	Instrument	DIG 48kHz
	Channel(s)	BOTH
	Input	S/P DIF
	Function	RMS & S/N
	Filter	OFF
	Speaker	AES Ch1&2
	Speaker	AES Ch1 *)
	Speaker	AES Ch2 **)
Spk Volume	100	

*) for checking channel 1, **) for checking channel 2

6. Check the signal levels at monitor output left and right with 600Ω termination

Switch the speaker between AES Ch1&2, Ch1 or Ch2 and check signal level at the output.

AC measurement at X8.1 (left) and X8.2 (right) with BNC adapter cable for monitor output:
 $V_{rms} = 5.66V \pm 0.3V$ at 1kHz generator frequency

7. Check the monitor output with different sampling frequencies during AES/EBU operation

Connect oscilloscope to the two outputs left and right with 600Ω termination. Vary the sampling frequency on the generator between 32 and 48 kHz. Vary the generator frequency between 20Hz ... 20kHz (15 kHz).

For every sampling frequency, a stable and proper sinewave signal must be provided at the monitor output. If the PLL is not synchronized for clock conditioning, sudden changes and distortions in the monitor output signal are produced.

7.5.1.5 Disassembly and Assembly

After opening the instrument, remove the angle for the monitor board on the rear panel. After loosening the DSP LINK flat cable (16-contact) and disconnecting the loudspeaker cable W3 as well as the two analog input cables W802B and W803B, the board can be carefully removed from the AT motherboard. The adapter board enclosed in the service kit and the extension for the DSP Link connector permit the board to be operated in such a position that the individual test points on the board are easily accessible.

7.5.1.6 External Interfaces

AT-bus interface to motherboard: see Digital Motherboard, page 7.275

Internal interface to Digital Generator, Analyzer (DSPLINK)						
name	Signal description	≡	source dest.	range	connector	comment
GND					X3.1	
TXDA	Link A		all DSPs	CMOS	X3.2	
CLKXA			all DSPs	CMOS	X3.3	
FSXA			all DSPs	CMOS	X3.4	
TXDB	Link B		all DSPs	CMOS	X3.5	
CLKXB			all DSPs	CMOS	X3.6	
FSXB			all DSPs	CMOS	X3.7	
TXDD	Link D		all DSPs	CMOS	X3.8	
CLKXD			all DSPs	CMOS	X3.9	
FSXD			all DSPs	CMOS	X3.10	
TXDG	Link G		all DSPs	CMOS	X3.11	
CLKXG			all DSPs	CMOS	X3.12	
FSXG			all DSPs	CMOS	X3.13	
LDSPCLK	33.5 MHz				X3.14	
SYNC	Sync DSPs				X3.15	
CLOCKDI	AES-Clock				X3.16	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Analog Monitor connection						
name	Signal description	≡	source dest.	range	connector	comment
A-MON 1	Analog In 1		Analog Mother-Board	$0...3 V_{rms}$	X5	
A-Mon 2	Analog In 2			$0...3 V_{rms}$	X6	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Loudspeaker connection						
name	Signal description	≡	source dest.	range	connector	comment
LS1	LS-OUT coding	O	Speaker	$0...10V_{pp}$ EMF	X4.1	
		O	8Ω		X4.2	
GND	Ground	O			X4.3	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Phones connection						
name	Signal description	≡	source dest.	range	connector	comment
PHONE-L	Left	O	phones	$0...16V_{pp}$ EMF	X8.1	
PHONE-R	Right	O		$0...16V_{pp}$ EMF	X8.2	
GND	Ground			$R_i = 10\Omega$	X8.3	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Parallel port connection						
name	Signal description	≡	source dest.	range	connector	comment
vacant					X2.1	
PD0	Data bus 8 bits			TTL	X2.2	
PD1				TTL	X2.3	
PD2				TTL	X2.4	
PD3				TTL	X2.5	
PD4				TTL	X2.6	
PD5				TTL	X2.7	
PD6				TTL	X2.8	
PD7				TTL	X2.9	
ER	Control lines for switcher	B		TTL	X2.10	open collector
EW		B		TTL	X2.11	open collector
EA		B		TTL	X2.12	open collector
EIRQ				TTL	X2.13	
ATT				TTL	X2.14	
AUX				TTL	X2.15	
ERST		B		TTL	X2.16	open Collector
PWR				TTL	X2.17	
GND	Ground lines			0 Volt	X2.18	
GND					X2.19	
GND					X2.20	
GND					X2.21	
GND					X2.22	
GND					X2.23	
GND					X2.24	
GND					X2.25	
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

7.6 PC and Front Module

7.6.1 Digital Motherboard (PC)

Circuit diagram 1030.8858.01 S
 Component location plan 1030.8858
 Parts list 1030.8858.01 SA

There are two different motherboards: 386SX20 (UPD 02) and 486DX33 (UPD 04 and 05). The UPD may be upgraded from 386 to 486 CPU (Upgrade kit UPD-U1).

7.6.1.1 Function

The Motherboard is an 386SX20 board compatible with industrial standard with the NEAT chip set. The coprocessor 80SX387 is installed in the UPD.

The main board of the UPD contains only little integrated circuits which can only partly be replaced in the case of repair. These include the CPD, the numeric coprocessor, a few bus drivers and the dynamic RAM devices. Most functions are contained in the C&T devices 82C301...306, 215, which cannot be replaced.

- CPU, memory addresses

The processor of the UPD is of the type Intel 80SX386. It uses a 20-MHz clock.

The memory area of the CPU is divided up as follows:

Address (hex)	Position	Function
000000 ... 09FFFF	Main board	Program memory (640 kbytes)
0A0000 ... 0AFFFF	VGA card	Screen memory in graphic mode (64 kbytes)
0B8000 ... 0BFFFF	VGA card	Screen memory in text mode (32 kbytes)
0C8000 ... 0CFFFF	VGA card	VGA-BIOS (32 kbytes) with Shadow
0D0000 ... 0EFFFF	Main board	<i>High</i> memory area
0F0000 ... 0FFFFFF	Main board	BIOS-Eprom (64 kbytes) with Shadow
100000 ... 10FFFF	Main board	<i>Upper</i> memory area, for DOS
100000 ... 3FFFFFF	Main board	Extended Memory (3 Mbytes)
FF0000 ... FFFFFFF	Main board	BIOS-Eprom (64 kbytes) (mirrored from 0F0000)

- Numeric coprocessor 80387

The Intel 80387 device provides the floating-point arithmetic operations in the hardware. It is capable of performing these operations up to 50 times as fast as the CPU in software. In the case of floating-point arithmetic, the UPD software as well as most of the state-of-the-art programming languages (R&S-Basic, Microsoft Quick-Basic, Pascal, C, etc.) check whether a numeric coprocessor is provided and make use of it automatically. Other computation-intensive programs (e.g. Autocad) even require it in any case.

In the event that the BIOS is not able to identify a present coprocessor and therefore does not indicate it in the Setup, this points to a fault in this device. In this case, the UPD is somewhat slower in the case of sweeps and numerical outputs.

- CPU, I/O addresses

The I/O area of the CPU is divided into two parts. Addresses 000 to 0FF are reserved for the main board, those from 100 to 3FF are provided for the additional cards. The 80386 processor being capable of differentiating between 65536 I/O addresses, only 1024 are decoded in industrial standard, i.e. usually, the same I/O address occurs 64 times over the entire I/O address area.

The I/O area of the CPU is divided up as follows on the main board:

Address (hex)	Function
000 ... 00F	DMA controller 1
020 ... 021	Interrupt controller 1 (IRQ0 to IRQ7)
022 ... 023	NEAT configuration
040 ... 043	Timer
060 ... 064	Keyboard controller
070 ... 071	Real-time clock and CMOS memory
080 ... 08F	DMA register
0A0 ... 0A1	Interrupt controller 2 (IRQ8 to IRQ15)
0C0 ... 0DF	DMA controller 2
0F0 ... 0FF	Numeric coprocessor

The I/O addresses, interrupt and DMA channel assignment of the additional cards are described with the respective cards.

- Controlling the peripheral devices (NEAT, buffer)

The complete peripheral equipment and its control (address decoding, timing specification, etc.) of the main board are contained in the large ASICs C&T 82C301 to 82C306 and 206. In detail, these ICs perform the following tasks:

82 C 301	Clock controller, memory access timing
82 C 302	Memory configuration
82 C 303/4/5/6	Data, address and control line buffer
82 C 206	2 DMA controllers (equivalent 8237A), 2 interrupt controllers (8259A), 1 timer (8254), 1 real-time clock with RAM (MC 146818)

The two ICs 82C301 and 302 permit various possible configurations of the UPD memory area (NEAT = New Enhanced AT). The 82C301 permits to vary the memory access time within large limits for 8-bit and 16-bit memory and I/O accesses separately. The 82C302 allows:

- flexible division of the present RAM into the normal program memory (0 to 640 kbytes)
- to superimpose present EPROMS in the range 640 kbytes to 1 Mbyte with the copy of their contents („Shadow-RAM“, faster access times)
- to utilize the RAM memory above 1 Mbyte as „Extended“ or „Expanded Memory“.

The two memory banks that can be fitted in the UPD may contain 1-byte devices each. If two banks with the same devices are fitted, an alternating access method (*Paging* and *Interleaving*) permits to access the RAM faster than would be possible with only one bank.

In addition to the clock registers, the real-time clock (part of the 82C206) also contains an additional 112-byte CMOS-RAM used for storing the computer configuration. The individual memory locations are addressed by outputting the desired address at I/O address 70H (out 070h, adr) and by address 71H reading the information and writing it there (in a1, 71h or out 071h, val).

The BIOS parameters are to be set according to section 4 of the operating manual. The *high* memory areas must in any case be set such that they can be accessed.

NOTE: When using a German keyboard, the characters **Y** and **Z** are exchanged.

- The CMOS-RAM is used as follows:

Address (70h)	Contents (71h)
00-0D	Real-time clock
0E	Diagnostic status
0F	Soft reset status
10	Disk drives A and B
11	reserved
12	Hard disk drives C and D
13	reserved
14	Hardware configuration
15	Memory size base (least significant byte)
16	Memory size base (most significant byte)
17	Memory size extension (least significant byte)
18	Memory size extension (most significant byte)
19-2D	reserved
2E-2F	Checksum over addresses 10 to 2D
30	Memory size extension (least significant byte)
31	Memory size extension (most significant byte)
32	Century
33	Storage location for selftest
34-3F	reserved
40-53	NEAT configuration
54-7D	reserved
7E-7F	Checksum of NEAT configuration

- RAM

The UPD can be fitted with 4 Mbytes (basic configuration) or 8 Mbytes (optional) dynamic RAM.

On failure of a RAM device, the computer can no longer boot. Since there is no stack either, the video control can no longer be initialized either. As a result of this, there is no longer a display on the monitor. If this is the case, the RAM devices should be replaced to make sure that they function properly.

- BIOS-Eprom

The system BIOS contains all routines, which directly drive the hardware of the UPD. This includes the selftest after switching on of the computer, the software interface to the individual hardware components as well the handling of the different hardware interrupts of the peripheral equipment on the main board. The system BIOS is supported by the VGA BIOS Eprom on the VGA card as far as the video control is concerned.

MS-DOS and all (modular, maintainable) programs thus do not access the hardware directly, but via the defined BIOS interfaces. However, there are exceptions in the case of particular requirements.

The BIOS first manages all software interrupts that can be executed by the CPU. Thus, a program wanting to process such software interrupts, has to enter its own routines into the address list of the interrupt routines.

The standard assignment of the interrupts is shown in the following table:

Interrupt No. (Hex)	Function	Hardware interrupt
0	Division by 0	
1	Single step	
2	Parity error	NMI
3	Program interruption	
4	Numerical range exceeded	
5	Print screen contents	
6	Reserved	
7	Reserved	
8	Timer	IRQ 0
9	Keyboard	IRQ 1
A	from 2nd interrupt controller	IRQ 2
B	COM 2	IRQ 3
C	COM 1	IRQ 4
D	LPT 2	IRQ 5
E	Floppy disk	IRQ 6
F	IEC bus	IRQ 7
10	Video	
11	Hardware configuration	
12	Memory size	
3	Floppy disk/hard disk	
14	Serial interfaces	
15	Cassette, special I/O functions, e.g. access to Extended Memory	
16	Keyboard	
17	Printer	
18	reserved	
19	Boot	
1A	Real-time clock	
1B	Keyboard interrupt	
1C	Timer routine	
1D	Video initialization (table)	
1E	Disk parameters (table)	
1F	Character set table	
- to be continued -		

- to be continued -		
Interrupt No. (Hex)	Function	Hardware interrupt
20	MS-DOS Program abort	
21	MS-DOS Function call	
22	MS-DOS End address	
23	MS-DOS Ctrl-Break abort	
24	MS-DOS Serious error	
25	MS-DOS Read absolute sector	
26	MS-DOS Write absolute sector	
27	MS-DOS End of program (TSR)	
28-3F	reserved for MS-DOS	
40-5F	reserved	
60-67	reserved for user routines	
68-6F	not used	
70	Real-time-clock hardware	IRQ 8
71	deviated from IRQ 2 on bus	IRQ 9
72	COM 3	IRQ 10
73	COM 4	IRQ 11
74	UDK or TTL	IRQ 12
75	Coprocessor	IRQ 13
76	Hard disk	IRQ 14
77	UDK or TTL	IRQ 15
78-7F	not used	
80-85	reserved for BASIC	
86-F0	reserved for BASIC (as long as it runs)	
F1-FF	not used	

- Keyboard controller

The keyboard controller is an extra micro-controller of the type 8042. It provides the connection between the external keyboard and the UPD. It converts the serial data coming from the keyboard into parallel data and generates an IRQ9 as soon as a complete byte has been transferred. The CPU may also send data to the keyboard, in which case the controller also performs the parallel-to-serial conversion.

- Jumper settings:

Jumper	Label	used	Meaning
JP3:	JP3	2 — 3	Crystal OSC 1
JP6:	JP6	2 — 3	Power down internal
JP7:	MON/COL	2 — 3	Color
JP8:	JP8	1 — 2	Battery external

7.6.1.2 Function (486DX33)

The Motherboard is a 486DX33 board compatible with industrial standard with VLSI chip set UM82C480. The coprocessor is included in the CPU.

The main board of the UPD contains only little integrated circuits which can only partly be replaced in the case of repair. These include the CPU, a few bus drivers and the dynamic RAM devices.

Most functions are realized with the chip set.

- CPU, Memory Address

The processor of the UPD is of the type Intel 80DX486. It uses a 33 MHz clock.

The memory area of the CPU is divided up same as for 386.

- Numeric Coprocessor

The coprocessor is integrated in the CPU.

- CPU, I/O addresses

Same as 386SX20 board.

- Chip set (UMB, Cache)

The complete peripheral equipment and its control (address decoding, timing specification, etc.) of the main board are contained in the large ASICs UMC 82C481B and UMC 82C482A. In detail, these ICs perform the following tasks:

82 C 481B	DRAM controller, cache controller
82 C 482A	system controller (timing, refresh, A20 gate)
82 C 206	2 DMA controllers (equivalent 8237A), 2 interrupt controllers (8259A), 1 timer (8254), 1 real-time clock with RAM (MC 146818)

The board comes with 256kByte cache memory. This cache and the system memory can be configured with BIOS settings (see the notes for the 386 board).

- CMOS-RAM, RAM, BIOS, Keyboard Controller

Same as 386 board.

Note: 1MB or 4MB SIMMs may be used; 4 SIMMs (one bank) must be identical.

- Jumper Settings:

Jumper	alternative	used	Meaning
JP1:	JP13	2 — 3	Color (not decoded)
JP2:	JP15	open	VESA: CPU \leq 33MHz
JP3:	JP16	open	VESA: 0 WS
JP4:	JP18	open	CPU \leq 25MHz
JP5:	JP19	1 — 2	CPU \leq 33MHz
JP6:	JP20	open	CPU \leq 20MHz
JP7:	JP21	open	CPU \leq 20MHz
JP8:	JP8	1 — 2	256kB Cache
JP9:	JP9	1 — 2	256kB Cache
JP10:	JP24	1 — 2	QFP CPU disabled
JP11:	JP25	1 — 2, 3 — 4	CPU 486 DX or P24T
JP12:	JP26	1 — 2 (2 — 3)	CPU 486 DX CPU P24T

7.6.1.3 Measuring Equipment

Voltmeter, hardware debugger, oscilloscope (> 100MHz)

7.6.1.4 Troubleshooting

- The BIOS issues beeps in the case of various errors:

Number	Meaning
1	DRAM refresh error
2	Base 64kB error
3	Parity error
4	System timer error
5	Processor error
6	A20 gate error, keyboard
7	Virtual mode error
8	VGA error
9	BIOS checksum error

- Clock, date faulty

If the real-time clock or the date are wrong after switching on, the CMOS battery may be flat.

- XCMOS Checksum failure

Battery may be flat, set setup as described in section 4 of the manual.

7.6.1.5 Testing and Adjustment

The installed memory, the CPU, interrupts, coprocessor and access on floppy disk and hard disk are automatically checked in the selftest.

7.6.1.6 Disassembly and Assembly

Disassembly:

Open UPD, remove all digital boards, remove blower; disconnect power cable, keyboard cable, battery cable and loudspeaker; loosen screws and laterally pull out the Motherboard beneath the Digital Power Supply.

Assembly:

Insert motherboard in UPD, reconnect all connection cables; remount digital boards and blower; set switch-on and BIOS parameters (see operating manual, section 4).

7.6.1.7 External Interfaces

AT-Bus						
name	Signal description	=	source dest.	range	connector	comment
acc. to P996 Working Group, Microprocessor Standards Committee						
CHK	Data	B	AT		XA1.1	
SD7		B	AT	TTL	XA1.2	
SD6		B	AT	TTL	XA1.3	
SD5		B	AT	TTL	XA1.4	
SD4		B	AT	TTL	XA1.5	
SD3		B	AT	TTL	XA1.6	
SD2		B	AT	TTL	XA1.7	
SD1		B	AT	TTL	XA1.8	
SD0		B	AT	TTL	XA1.9	
IOCHRDY*		O	AT	TTL	XA1.10	
AEN	I	AT	TTL	XA1.11		
SA19	Addresses	O	AT		XA1.12	
SA18		O	AT		XA1.13	
SA17	Addresses	O	AT		XA1.14	
SA16		O	AT	TTL	XA1.15	
SA15		O	AT	TTL	XA1.16	
SA14		O	AT	TTL	XA1.17	
SA13		O	AT	TTL	XA1.18	
SA12		O	AT	TTL	XA1.19	
SA11		O	AT	TTL	XA1.20	
SA10		O	AT	TTL	XA1.21	
SA9		O	AT	TTL	XA1.22	
SA8		O	AT	TTL	XA1.23	
SA7		O	AT	TTL	XA1.24	
SA6		O	AT	TTL	XA1.25	
SA5		O	AT	TTL	XA1.26	
SA4	O	AT	TTL	XA1.27		
SA3	O	AT	TTL	XA1.28		
SA2	O	AT	TTL	XA1.29		
SA1	O	AT	TTL	XA1.30		
SA0	O	AT	TTL	XA1.31		
GND	Ground		AT	0 V	XB1.1	
RESDRV	Reset	O	AT	TTL	XB1.2	
VDD	Power	O	AT	+5V ±5%	XB1.3	
IRQ9	Interrupt	I	AT	TTL	XB1.4	
-5V			AT	-5V ±5%	XB1.5	
DRQ2		I	AT		XB1.6	
-12V		O	AT	-12V ±5%	XB1.7	
ENDXFR		I	AT		XB1.8	
+12V		O	AT	+12V ±5%	XB1.9	
GND			AT	0 V	XB1.10	
MEMW*	Memory Write	O	AT	TTL	XB1.11	
MEMR*	Memory Read	O	AT	TTL	XB1.12	
IOW*	IO Write	O	AT	TTL	XB1.13	
IOR*	IO Read	O	AT	TTL	XB1.14	
DACK 3		O	AT		XB1.15	
DRQ 3		I	AT		XB1.16	
DACK 1		O	AT		XB1.17	
DRQ 1		I	AT		XB1.18	
RFSH*	Refresh	O	AT	TTL	XB1.19	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
SYSCLK	Interrupt	O	AT	TTL +5 V ±5%	XB1.20	14.31818 MHz
IRQ7		I	AT		XB1.21	
IRQ6		I	AT		XB1.22	
IRQ5		I	AT		XB1.23	
IRQ4		I	AT		XB1.24	
IRQ3		I	AT		XB1.25	
DACK2		O	AT		XB1.26	
TC		I	AT		XB1.27	
BALE		O	AT		XB1.28	
VDD		O	AT		XB1.29	
OSC		O	AT		TTL	
GND	O	AT	0 V	XB1.31		
BHE*	Byte High Ena. Address	O	AT	TTL	XC1.1	
LA23		O	AT	TTL	XC1.2	
LA22		O	AT	TTL	XC1.3	
LA21		O	AT	TTL	XC1.4	
LA20		O	AT	TTL	XC1.5	
LA19		O	AT	TTL	XC1.6	
LA18		O	AT	TTL	XC1.7	
LA17		O	AT	TTL	XC1.8	
MEMR*	Data	O	AT	TTL	XC1.9	
MEMW*		O	AT		XC1.10	
SD8		B	AT		XC1.11	
SD9		B	AT		XC1.12	
SD10		B	AT		XC1.13	
SD11		B	AT		XC1.14	
SD12		B	AT		XC1.15	
SD13		B	AT		XC1.16	
SD14	B	AT	TTL	XC1.17		
SD15	B	AT	TTL	XC1.18		
MEMCS16*	16 Bit I/O	I	AT	TTL	XD1.1	
IOCS16		I	AT		XD1.2	
IRQ10		I	AT		XD1.3	
IRQ11		I	AT		XD1.4	
IRQ12		I	AT		XD1.5	
IRQ15		I	AT		XD1.6	
IRQ14		I	AT		XD1.7	
DACK 0		O	AT		XD1.8	
DRQ 0		I	AT		XD1.9	
DACK 5		O	AT		XD1.10	
DRQ 5		I	AT		XD1.11	
DACK 6	O	AT	XD1.12			
DRQ 6	I	AT	XD1.13			
DACK 7	O	AT	XD1.14			
DRQ 7	I	AT	XD1.15			
VDD	O	AT	+5 V	XD1.16		
MASTER	I	AT		XD1.17		
GND	I	AT	0 V	XD1.18		

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

The current supply of the Digital Motherboard is accomplished via two 6-contact connectors; they are to be inserted such that the ground terminal (blue) points to the inside.

Power Connector						
name	Signal description	≡	source dest.	range	connector	comment
PWGOOD	Voltage OK	I	DigNT	TTL	P8.1	

- continued -

- continued -

name	Signal description	≡	source dest.	range	connector	comment
+5V		I	DigNT	+5V ±0.2V	P8.2	
+12V		I	DigNT	+12V ±1V	P8.3	
-12V		I	DigNT	-12V ±1V	P8.4	
GND		I	DigNT		P8.5,6	
GND		I	DigNT		P9.1,2	
-5V		I	DigNT	-5V ±0.2V	P9.3	
+5V	3A	I	DigNT	+5V ±0.2V	P9.4,5,6	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

External keyboard
(5-contact DIN connector)

name	Signal description	≡	source dest.	range	connector	comment
CLOCK		I	external	TTL	1	from keyboard
DATA		B	external	TTL	2	not used
n.c.					3	
GND					4	
+5V		O	external	TTL	5	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Loudspeaker connection

name	Signal description	≡	source dest.	range	connector	comment
OUT	Speaker	O	LP	TTL	1	
n.c.					2	
GND					3	
+5V		O	LP		4	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Battery connection

name	Signal description	≡	source dest.	range	connector	comment
GND		O	BATT		1	
n.c.					2	
n.c.					3	
+4.5V		O	BATT		4	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.6.2 IEC-bus interface

Circuit diagram	1006.4404.01 S
Component location plan	1006.4404
Parts list	1006.4404.01 SA

7.6.2.1 Function

The IEC-bus interface is used to control the UPD with IEC-bus control devices. The UPD card (plug-in card for PC) can be operated both in talker/listener mode and in controller mode.

- Address decoding

This block (D10-A/D11-A/D12-A/D13-A in the circuit diagram) decodes the address lines applied and generates the Enable signal required for selection of the respective components.

Switches S1-D and S1-E are used to set the card as the 1st or 2nd interface at D13-A; in the UPD, the card is used as the 1st interface.

- Signal buffer (computer interface)

This function block (D1-A/D2-A/D3-A) constitutes the interface between the ISA bus and the further components of the interface.

- PAL

The PAL (D5, Gatearray) serves the function of a status device. With the address, data and control lines, it is connected in parallel with the IEC-bus controller 7210 (D21-A) and generates the control signal required for interrupt and DMA control. The PAL permits to cut down on discrete ICs.

- DMA control

If the bus has picked up or transferred a character, a DRQ is generated by the Controller device (D21-A) in conjunction with the devices D14-B/D18-A/D16-A/D20-D. Using jumper X2A/X3A on DRQ1 . . . DRQ3, this DRQ can be applied to the DMA controller of the computer, which performs the data transfer into the main memory.

UPD setting: DMA channel 1

- Interrupt control

If the final character is detected by the controller, it generates the signal IECINT. Since the interface may be fitted twice, using the same interrupt, a semaphore control is implemented in the block with D4/D6/D14/D16/D17. The following devices D19/D6/D20 are used to determine the interrupt pulse length. The interrupt can be caused using jumper X4A on IRQ3 . . . IRQ9.

UPD setting: Interrupt 7

- UPD 7210

The UPD 7210 is the bus controller and thus the central device (D21-A) of the interface. Controlled by the software (IEC-bus drivers), it controls the standard traffic on the IEC bus.

- Bus driver

Der Controller 7210 is connected with the IEC bus via the transceiver devices (D22-A/D23-A).

- Reading in the bus control lines and internal control signals

Via this block (D24-A/D25A), the control lines of the IEC bus and control signals of the Controller 7210 can be read in.

7.6.2.2 Measuring Equipment

For testing and adjustment, the following components are required:

- UPD and PSA computer
- one IEC-bus cable
- Final test program IECB of PSA

7.6.2.3 Troubleshooting

- Possible faults:
 - IEC driver not loaded
 - Board address not correctly set
 - Board completely faulty
- Interrupt level not correctly set or faulty interrupt control
- Transceiver or IEC cable faulty
- Controller 7210 faulty

7.6.2.4 Testing and Adjustment

Testing:

The final test requires the BASIC main program IECB.BAS and the BASIC module IECT0.BAS. The file ENDTEST.INI is necessary to specify settings such as in-depth testing and, e.g. the log file (default is PROTC). This file must already be provided (created), since it is not generated by the final test program. The final test is started by means of the entry BASIC IECB r or as part of the batch file ENDTEST.BAT.

The program inquires about the number of built-in IEC-bus cards and whether the computer is connected with a further controller via the IEC bus and whether the final test program is executed there. Note that the program has been started on the second controller with the entry BASIC IECT0 r, and the entry SEC=Yes is contained in the control file ENDTEST.INI.

For the performed tests, the program enters 'passed' or 'failed' in the log file.

The programs and files are included on the appropriate floppy disk enclosed with the service kit.

Adjustment:

There is no need for an adjustment.

7.6.2.5 Disassembly and Assembly

After opening the instrument, loosen the lefthand rear-panel clip and remove.

Loosen and remove the safety lock, pull the card out of the slot.

Replacement:

Check the card for correct jumper setting and insert. Mount the lateral safety bracket and the rear-panel clip.

7.6.2.6 External Interfaces

AT-bus interface: see Digital Motherboard, page 7.275.

IEEE connector						
name	Signal description	≡	source dest.	range	connector	comment
GND			external	0V	X10.12,18,19,20 X10.21,22,23,24	
/GPATN		B	external	TTL	X10.11	
/GPEOI		B	external	TTL	X10.5	
/GPSRQ		B	external	TTL	X10.10	open collector
/GPREN		B	external	TTL	X10.17	
/GPIFC		B	external	TTL	X10.9	
/GPSAV		B	external	TTL	X10.6	
/GPNDAC		B	external	TTL	X10.8	open collector
/GPNRED		B	external	TTL	X10.7	open collector
IECD0	Data bus	B	external	TTL	X10.1	
IECD1		B	external	TTL	X10.2	
IECD2		B	external	TTL	X10.3	
IECD3		B	external	TTL	X10.4	
IECD4		B	external	TTL	X10.13	
IECD5		B	external	TTL	X10.14	
IECD6		B	external	TTL	X10.15	
IECD7		B	external	TTL	X10.16	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.6.3 VGA Board and LCD

Circuit diagram	1050.0000.02 S
Component location plan	1050.0000
Parts list	1050.0000.01 SA

7.6.3.1 Function

The R&S VGA card provides a fully AT-compatible, highly integrated graphics system based on the VGA-Controller Cirrus CL-GD6410. It is 100% compatible with IBM VGA hardware. Two VGA monitors and a LCD display can be connected. Simultaneous operation of LCD and CRT is possible.

Components: Cirrus GD6410
 Socket for 8-bit VGA-Bios
 Video RAM
 AT interface 16 bit
 Connector for LCD
 Connector for CRT
 Voltage converter

- VGA controller

The highly integrated single-chip VGA Controller GD6410 incorporates all control functions required for configuring a VGA board and thus enables a minimum form factor. Only little additional components are required for implementation of a graphics card.

- Video memory

The board contains a 256-kbyte video memory consisting of two DRAMs 256 kbytes * 4 (Page Mode, access time 70 - 100 ns).

- Resolution, colours

The video memory allows for a resolution of 640 * 480 or 800 * 600 with 16 colours in each case.

- VGA-BIOS-ROM

A socket (PLCC, 32-contact) for a BIOS-PROM is provided. The VGA-Bios requires 32 kbytes memory space in the memory area C0000 - C7FFF . PROMs of the type 27C256 or 27C512 can be used. The bios is addressed by 8 bits.

- Connectable monitors

Three connectors for monitors are provided:

- Standard VGA connector for CRT

The standard VGA connector is attached to the rear panel as with commercial graphics cards. It permits connection of an external CRT monitor, for example.

- Two-row connector strip (2*8 pins) for CRT

The two-row connector strip is used for connection of an internal CRT monitor.

- Two-row flat connector (2*17 pins, lockable) for LCD

Monochrome dual-scan LCD monitors, colour LCD monitors and EL-displays are supported. When connecting an EL-display, the required +24 V voltage is to be externally applied because of the high current consumption.

- Operating modes

Three operating modes can be selected:

CRT: The LCD monitor is switched off.

LCD: The CRT monitor is switched off.

SimulSCAN: LCD and CRT are operated simultaneously.

The switchover is accomplished via Bios interrupt. For testing purposes, programs are available, which permit to switch over by means of menus or hotkey.

In the operating mode SimulSCAN, the colours of the CRT are converted in grey shades on the LCD.

- LCD Switch-on timing

The operating voltages +5 V and 12 V and the contrast voltages are cut in in a particular order at defined time intervals. This is necessary, since the lifetime of the connected LCD monitor would otherwise be extremely reduced.

- Contrast voltages

The two contrast voltages +23 V and -23 V are generated on the board (loading capacity 50 mA each). These voltages can be set to the value required by the connected display using a regulator.

- Jumpers to be plugged in:

– X10.2 - X10.3

– X11.2 - X11.3

- Setting the DIP switches (S1):

Type of monitor:	S1-A	S1-B	S1-C	S1-D
LCD type monochrome (Dual Scan)	open	closed	closed	closed
LCD type colour	closed	closed	closed	closed
Video RAM (D5 - D7):	S1-E	S1-F		
80 ns	closed	open		
100 ns	closed	closed		

7.6.3.2 Measuring Equipment

For testing and adjustment, the following components are required:

- PC test adapter
- external VGA monitor
- Test program TESTPIC.EXE
- TSR program SWITCHER.COM
- Frequency counter (up to 15 MHz)
- Voltmeter (DC, range ± 30 V)

7.6.3.3 Troubleshooting

- Checking external CRT:
 - Insert card into AT.
 - Connect VGA monitor.
 - Switch on AT and call test program TESTPIC.EXE.
 - Check test patterns (continue by pressing RETURN).
- Checking the connected LCD supply voltages
 - Insert card on PC test adapter in AT.
 - Connect VGA monitor.
 - Switch on AT / UPD.
 - Call test program SWITCHER.COM.
 - Call test program TESTPIC.EXE. First test pattern.
 - Using the key combination CTRL-SHIFT-D, set the type of display to CRT alone (D1.101 and D1.102 LOW).
 - * Check the supply voltage at D10.14 and D11.14: $+12V \pm 5\%$.
 - * Check the output voltage D10.6: $+24V \pm 10\%$.
 - * Check the control signals D1.101 and D1.102: LOW.
 - * Check the output voltages:
X3.6, X3.8, X3.10, X3.12, X3.28, X3.29, X3.30 and X3.32: All 0 V.
 - Using the key combination CTRL-SHIFT-D, set the type of display to LCD alone (VGA monitor shows black display).
 - * Check the control signals D1.101 and D1.102: HIGH.
 - * Check the output voltages under load:

Pin	Level	Load:
X3.6, X3.8, X3.10, X3.12:	$+5V \pm 5\%$	$2k\Omega$
X3.28:	$+24V \pm 10\%$	$1k\Omega$
X3.29, X3.30:	$+12V \pm 10\%$	$3k\Omega$
X3.32:	$-24V \pm 10\%$	$1k\Omega$
 - Using the key combination CTRL-SHIFT-D, set the type of display to CRT and LCD (CRT shows test pattern, D1.101 and D1.102 HIGH).
 - * Repeat the tests accordingly for CRT alone.
- Checking the clock supply
 - D9.1: 14.31818 MHz
 - D1.103: 32.768 kHz
- Checking the LCD signals
 - Using the key combination CTRL-SHIFT-D, set the type of display to LCD alone (VGA monitor shows black display).
Check the following pins to determine whether signals are applied: X3.3, X3.5, X3.7, X3.9

- Using the key combination CTRL-SHIFT-D, set the type of display to CRT and LCD (CRT shows test pattern, D1.101 and D1.102 HIGH).
Check the following pins to determine whether signals are applied: X3.3, X3.5, X3.7, X3.9
- Backlighting
 - Check the current supply to the converter
 - Check the brightness potentiometer
 - Check the output voltage of the converter (caution 1kV!).
 - Check and, if necessary, replace the tube.

7.6.3.4 Testing and Adjustment

Testing:

See troubleshooting.

Adjustment:

There is no need for an adjustment.

7.6.3.5 Disassembly and Assembly

- **Replacing the VGA card:**

Open the instrument and loosen and remove the lefthand rear-panel clip.

Loosen the safety lock and remove, pull the card out of its location.

Replacement:

Check the card for correct jumper setting and insert. Mount the lateral safety bracket and the rear-panel clip.

- **Cleaning the LCD:**

Do not use acids or scouring agent (otherwise the anti-reflecting coat will be damaged)! It is recommended to use standard detergents for optical devices such as glasses, lenses, etc., or water with some rinsing agent.

- **Replacing the tube:**

- Remove the front panel (see section 7.6.6.5, page 7.294).
- Remove the LCD retaining plate (7 screws).
- Loosen the high-voltage cable to the lamp and the data cable to the LCD.
- Loosen 4 screws at the corners, take the LCD module out of the retaining plate.
- Loosen the lamp clamping and replace the lamp.

- **Replacing the high-voltage converter:**

Remove both safety brackets, remove the blower (see page 7.298). Remove the cover and pull the plug.

7.6.3.6 External Interfaces

AT-bus interface: see Digital Motherboard, page 7.275.

VGA connector						
name	Signal description	≡	source dest.	range	connector	comment
R	Red	O	Monitor	0 -0.7 V into 75Ω	X2.1	
G	Green	O	Monitor	0 -0.7 V into 75Ω	X2.2	
B	Blue	O	Monitor	0 -0.7 V into 75Ω	X2.3	
MID2	Monitor ID	I	Monitor	TTL	X2.4	
GND		O	Monitor	0 V	X2.5	
R-GND	Ground red	O	Monitor	0 V	X2.6	
G-GND	Ground green	O	Monitor	0 V	X2.7	
B-GND	Ground blue	O	Monitor	0 V	X2.8	
			Monitor		X2.9	
GND		O	Monitor	0 V	X2.10	
MID0	Monitor ID	I	Monitor	TTL	X2.11	
MID1	Monitor ID	I	Monitor	TTL	X2.12	
HSYNC	Sync.	O	Monitor	TTL	X2.13	
VSYNC	Sync.	O	Monitor	TTL	X2.14	
			Monitor		X2.15	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

LCD connector						
name	Signal description	≡	source dest.	range	connector	comment
MOD		O	LCD	TTL	X3.1	
BLANK*		O	LCD	TTL	X3.2	
LFS		O	LCD	TTL	X3.3	
GND		O	LCD	0 V	X3.4	
LLCLK		O	LCD	TTL	X3.5	
SWVDD		O	LCD	0V, +5V (connected)	X3.6	
FPHDE		O	LCD	TTL	X3.7	
SWVDD		O	LCD	0V, +5V (connected)	X3.8	
PD4	Data	O	LCD	TTL	X3.11	
GND		O	LCD	0V	X3.12	
PD5		O	LCD	TTL	X3.13	
GND		O	LCD	0V	X3.14	
PD6		O	LCD	TTL	X3.15	
GND		O	LCD	0V	X3.16	
PD7		O	LCD	TTL	X3.17	
GND		O	LCD	0V	X3.18	
PD0		O	LCD	TTL	X3.19	
GND		O	LCD	0V	X3.20	
PD1		O	LCD	TTL	X3.21	
GND		O	LCD	0V	X3.22	
PD2		O	LCD	TTL	X3.23	
GND		O	LCD	0V	X3.24	
PD3		O	LCD	TTL	X3.25	
GND		O	LCD	0V	X3.26	
PD8		O	LCD	TTL	X3.27	
SWVPOS1		O	LCD	0V, +24V (connected)	X3.28	
SWVPOS2		O	LCD	0V, +12V (connected)	X3.29	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
SWVPOS2		O	LCD	0V, +12V (connected)	X3.30	
VSYNC		O	LCD	TTL	X3.31	
SWVNEG		O	Contrast	0V, -24V (connected)	X3.32	
HSYNC		O	LCD	TTL	X3.33	
					x3.34	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Internal CRT connector						
name	Signal description	≡	source dest.	range	connector	comment
R	Red	O	AT	0 - 0.7 V an 75Ω	X5A.1	
G	Green	O	AT	0 - 0.7 V an 75Ω	X5A.2	
B	Blue	O	AT	0 - 0.7 V an 75Ω	X5A.3	
MID2	Monitor ID	I	AT	TTL	X5A.4	
			AT		X5A.5	
R-GND	Ground red	O	AT	0 V	X5A.6	
G-GND	Ground green	O	AT	0 V	X5A.7	
B-GND	Ground blue	O	AT	0 V	X5A.8	
			AT		X5B.1	
GND		O	AT	0 V	X5B.2	
MID0	Monitor ID	I	AT	TTL	X5B.3	
MID1	Monitor ID	I	AT	TTL	X5B.4	
HSYNC	Sync.	O	AT	TTL	X5B.5	
VSYNC	Sync.	O	AT	TTL	X5B.6	
			AT		XB5.7	
			AT		XB5.8	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.6.4 Combi Controller

Circuit diagram 1030.8464.01 S
 Component location plan 1030.8464
 Parts list 1030.8464.01 SA

1. Function

The Combi-Controller is a standard IDE (AT-BUS) controller with floppy-disk interface, IDE interface, a parallel port, two serial ports and a gameport (which is not connected in the UPD though).

The front-panel LED drive activity is driven by this board.

There are 2 different (but equivalent) types:

(a) PM-electronic CI91

Setting of the jumpers		
▶ Ser. Port 1 COM1: (3F8H) COM3: (3E8H) COM4: (2E8H) disabled	JP6 - Pos 1 L (bottom) H L L H	JP6 - Pos 2 H L L H
▶ Ser. Port 2 COM2: (2F8H) COM3: (3E8H) COM4: (2E8H) disabled	JP6 - Pos 3 L (bottom) L H H	JP6 - Pos 4 H (top) L L H
▶ Par. Port 1 LPT1: (378H) LPT2: (278H) LPT3: (3BCH) disabled	JP6 - Pos 5 H L L H	JP6 - Pos 6 L H L H
▶ Floppy enable enabled disabled	JP7 - Pos 5 L (bottom) H (top)	
▶ IDE HD enable enabled disabled	JP7 - Pos 4 L (bottom) H (top)	
▶ HDD adr 3F6,3F7,1F0-1F7 376,377,170-177	JP7 - Pos 1 H L	
▶ Floppy select normal A-B change	JP7 - Pos 2 L H	
▶ Floppy adr 3F0-3F7 370-377	JP7 - Pos 3 H L	
▶ PC Type AT XT	JP7 - Pos 3 L H	
▶ INT (Ser. 1) IRQ3 IRQ4 IRQ5	JP8 - Pos: 2 1 3	
- to be continued -		

- to be continued -		
Setting of the jumpers		
▶ INT (Ser. 2) IRQ3 IRQ4 IRQ5	JP8 - Pos: 4 5 6	
▶ INT (Parallel) IRQ7 IRQ5	JP8 - Pos: 7 8	
▶ means: set in the UPD		

(b) PM-electronic CI92

Setting of the jumpers		
▶ Ser. Port 1 COM1: (3F8H) COM3: (3E8H) COM4: (2E8H) disabled	JP7 2-3 closed 1-2 closed 2-3 closed 1-2 closed	JP8 1-2 closed 2-3 closed 2-3 closed 1-2 closed
▶ Ser. Port 1 COM2: (2F8H) COM3: (3E8H) COM4: (2E8H) disabled	JP9 2-3 closed 2-3 closed 1-2 closed 1-2 closed	JP10 1-2 closed 2-3 closed 2-3 closed 1-2 closed
▶ Par. Port 1 LPT1: (378H) LPT2: (278H) LPT3: (3BCH) disabled	JP11 2-3 closed 1-2 closed 2-3 closed 1-2 closed	JP12 1-2 closed 2-3 closed 2-3 closed 1-2 closed
▶ Floppy enable enabled disabled	JP14 1-2 closed 2-3 closed	
▶ HDD adr 3F6,3F7,1F0-1F7 376,377,170-177	JP15 1-2 closed 2-3 closed	
▶ Floppy adr 3F0-3F7 370-377	JP17 1-2 closed 2-3 closed	
▶ INT (Ser. 1) IRQ3 IRQ4 IRQ5	JP18 2 closed 1 closed 3 closed	
▶ INT (Ser. 2) IRQ3 IRQ4 IRQ5	JP18 4 closed 5 closed 6 closed	
▶ INT (Parallel) IRQ7 IRQ5	JP18 7 closed 8 closed	
▶ GAME Port enabled disabled	JP19 2-3 closed 1-2 closed	
▶ means: set in the UPD		

2. Measuring equipment

none

3. Troubleshooting

For troubleshooting, it is recommended to use the Checkit program. Appropriate shorting plugs for the ports are enclosed with the service kit.

4. Testing and adjustment

There is no need for an adjustment

5. Disassembly and Assembly

Disassembly:

After opening the instrument, loosen the lefthand rear-panel clip and remove.

Loosen the lateral safety bracket and remove, pull the card out of its location.

Replacement:

Check the card for correct jumper setting and plug in. Mount the lateral safety bracket and rear-panel clip.

6. Interfaces

AT-bus interface: see Digital Motherboard, page 7.275.

(a) Sitra SAB-960**(b) PM-electronic CI91**

JP1	IDE HDD 40-contact connection (***)
JP2	LED connection (red - top)
JP3	shorted with simple HDD installation
JP4	shorted: printer port is only output open: printer port is input and output, the direction is controlled by the printer.
JP5	IBM: 2-3 connected, otherwise: 1-2 connected
JP9	34-contact floppy connection
JP10	16-contact gameport
JP11	2nd serial interface, 10-contact *)
JP12	1st serial interface, 9-contact
JP13	printer interface, 25-contact

(c) PM-electronic CI92

J1	Printer interface, 25-contact
J2	1st serial interface, 9-contact
JP1	IDE HDD 40-contact connection (***)
JP2	shorted with simple HDD installation
JP3	34-contact floppy connection
JP4	2nd serial interface, 10-contact *)
JP5	LED connection (**)
JP6	16-contact gameport
JP13	shorted: printer port is only output open: printer port is input and output, the direction is controlled by the printer.

Notes:

*) The second serial interface deviates with respect to the pin assignment with the IDE cards. In the case of replacement, make sure to check the pin assignment. (*With CI91 and CI92, however, the same cable can be used.*)

***) The connector for the LED deviates with respect to position and pin assignment with the IDE cards.

***) With CI92, the IDE cable is prolonged by 5 cm.

⇒ A different IDE card was used for the pilot series. It is identical with respect to the functions, however the position of the terminals is different.

7.6.5 Connector Board

Circuit diagram	1030.8906.01 S
Component location plan	1030.8906
Parts list	1030.8906.01 SA

7.6.5.1 Function

The Connector Board interconnects the different front-panel modules and supplies them with current.

- Current supply
The Connector Board is supplied with current by the Digital Power Supply, distributing it to floppy disk, hard disk, blower and high-voltage generator for the backlighting.
- Backlighting
The backlighting is supplied by a high-voltage converter, which is connected to the Connector Board via a relay controlled by the PERIF.
- Brightness control and contrast
The brightness of the backlighting is controlled by a potentiometer on the Keyboard module.
- Blower
see Blower board, page 7.298.

7.6.5.2 Measuring Equipment

Ohmmeter, voltmeter

7.6.5.3 Troubleshooting

Check the respective voltages and control signals

7.6.5.4 Testing and Adjustment

There is no need for an adjustment.

7.6.5.5 Disassembly and Assembly

Disassembly:

Loosen all connections and unscrew the board.

Assembly:

Plug the softkey connector strip into the Connector Board before mounting into the UPD. Mount the board and insert the remaining connectors.

7.6.5.6 External Interfaces

Connector for VGA Board						
name	Signal description	≡	source dest.	range	connector	comment
GND1		P			X13.4,14,16,18,20,22,24,26	
SWVDD	=VDD (+5V)		VGA	+4.9 ... 5.2V	X13.6,8,10,12 (connected)	
SWVNEG	-24,5 V		VGA	-24.1 ... -24.9V	X13.32	
LFS	=S Scan signal		VGA	TTL	X13.3	
LCCLK	=CP1 Data latch		VGA	TTL	X13.5	
FPVDCLK	=CP2 Input clock		VGA	TTL	X13.9	
UPPER0	Data		VGA	TTL	X13.11	
UPPER1			VGA	TTL	X13.13	
UPPER2			VGA	TTL	X13.15	
UPPER3			VGA	TTL	X13.17	
LOWER0	Data		VGA	TTL	X13.19	
LOWER1			VGA	TTL	X13.21	
LOWER2			VGA	TTL	X13.23	
LOWER3			VGA	TTL	X13.25	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Connector for keypad						
name	Signal description	≡	source dest.	range	connector	comment
GND2			Softkey		X9.1	
GND2			Softkey		X9.29,30	
+ 5V			Softkey		X9.26,34	
PIO5	CFTT on		Softkey	TTL	X9.25	
COL0			Softkey	TTL	X9.13	
COL1		O	Softkey	TTL	X9.14	
COL2		O	Softkey	TTL	X9.11	
COL3		O	Softkey	TTL	X9.12	
COL4		O	Softkey	TTL	X9.9	
COL5		O	Softkey	TTL	X9.10	
COL6		O	Softkey	TTL	X9.7	
COL7		O	Softkey	TTL	X9.8	
ROW6			Softkey	TTL	X9.17	
VR1	Brightness		LCD			
VR2	Brightness		LCD		X9.28	
KONTR1	Contrast		LCD		X9.31	
KONTR2	Contrast		LCD		X9.32	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Connector for DC/AC converter						
name	Signal description	≡	source dest.	range	connector	comment
GND1		O	DC/AC		X7.1	
VIN	+ 12 V	O	DC/AC	+12 V ±1V	X7.2	
CNT	Lamp on	O	DC/AC	TTL	X7.3	
VR1	Brightness	O	DC/AC		X7.5	
VR2	Brightness	O	DC/AC		X7.4	

Explanation: ≡: |:Input, O:Output, B:Bidirectional, P:Power

Connector to LCD						
name	Signal description	≡	source dest.	range	connector	comment
S	Scan signal	O	LCD	TTL	1	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
CP1	Input latch	O	LCD	TTL	2	
CP2	Input clock	O	LCD	TTL	3	
VDD	+ 5 V	O	LCD	+5 V ±0.2V	4	
VSS	GND1	O	LCD		5	
VEE	-24.5 V	O	LCD	-24.5 ±0.4V	6	
DU0	Data	O	LCD	TTL	7	
DU1		O	LCD		8	
DU2		O	LCD		9	
DU3		O	LCD		10	
DL0	Data	O	LCD	TTL	11	
DL1		O	LCD		12	
DL2		O	LCD		13	
DL3		O	LCD		14	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Softkey connector						
name	Signal description	≡	source dest.	range	connector	comment
COL0		O	Softkey	TTL	X8.2	
COL1		O	Softkey	TTL	X8.3	
COL2		O	Softkey	TTL	X8.4	
COL3		O	Softkey	TTL	X8.5	
COL4		O	Softkey	TTL	X8.6	
COL5		O	Softkey	TTL	X8.7	
COL6		O	Softkey	TTL	X8.8	
COL7		O	Softkey	TTL	X8.9	
ROW6		I	Softkey	TTL	X8.1	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Power plug						
name	Signal description	≡	source dest.	range	connector	comment
GND3		I	Power supply		X2.2,X2.3	
+12V		I		+12V ± 1V	X2.1	
+5V		I		+5V ± 0.2 V	X2.4	
GND3		I	Floppy		X5.2,X5.3	
+12V		I		+12V ± 1V	X5.1	
+5V		I		+5V ± 0.2 V	X5.4	
GND3		I	Floppy		X6.2,X6.3	
+12V		I		+12V ± 1V	X6.1	
+5V		I		+5V ± 0.2 V	X6.4	
GND3		O	Blower		X10.3	
+12V		O		+12V ± 1V	X10.2	
SENSE		O			X10.1	
GND3		I	free		X20.1,X50.1,X60.1	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.6.6 Keyboard

Circuit diagram	1030.9002.01 S
Component location plan	1030.9002
Parts list	1030.9002.01 SA

7.6.6.1 Function

- Keys

The keyboard is designed as a row-and-column matrix, the keys being positioned at the points of intersection between a column and a row. Line 6 is connected to the Connector Board for scanning the softkeys.

- LED

The operating states OUTPUT OFF, LCD OFF and REMOTE are indicated by LEDs controlled by the PERIF on the Digital Generator. The necessary series resistors (1.5k Ω) are also accommodated on the Digital Generator.

- POTI

This module accommodates the potentiometers for the brightness and contrast setting of the LCD. (see page 7.281)

- Rotary knob

The rotary knob with 24 magnetic detent positions is evaluated by 2 Hall sensors mounted with a phase shift of 90° (referred to the magnetization). The resulting pulse sequences are evaluated by the PERIF with respect to phase position (results in the direction) and number (results in the rate). If a given minimum pulse rate is achieved, the PERIF activates an acceleration algorithm in order to enable fast cursor movements.

7.6.6.2 Measuring Equipment

Voltmeter, ohmmeter

7.6.6.3 Troubleshooting

The program PERIF.EXE permits optical checking of the actuated keys on the screen (using a stylized keypad).

7.6.6.4 Testing and Adjustment

Testing:

Call PERIF.EXE;

actuate all keys and the rotary knob and observe the output on the screen.

Adjustment:

There is no need for an adjustment.

7.6.6.5 Disassembly and Assembly

Removing the front panel:

- Loosen the rotary knob using a 2-mm Allen-type wrench.
- Loosen 4 screws at the corners and 3 mini-screws on the front panel.
- Take off the front-panel cover
- Loosen the screws marked like this  (8 pcs).
- Detach the Bowden cable of the power switch at the rear of the power supply using angle tweezers (do not twist the screw).
- Loosen all flat cables and the power cable on the Connector Board.
- If UPD-B2 is fitted, disconnect 10-contact flat cable and coaxial cable from AES/EBU.
- Tilt the front module towards the front.

Loosen the keyboard cable and take out the keyboard.

Assembly:

There is nothing special to be observed.

7.6.6.6 External Interfaces

Male connector						
name	Signal description		source dest.	range	connector	comment
GND			DigGen		X1,29,30	
+ 5V			DigGen	+ 5V \pm 0.2V	X26,34	
COL0			DigGen	TTL	13	
COL1			DigGen	TTL	14	
COL2			DigGen	TTL	11	
COL3			DigGen	TTL	12	
COL4			DigGen	TTL	9	
COL5			DigGen	TTL	10	
COL6			DigGen	TTL	7	
COL7			DigGen	TTL	8	
ROW0		O	DigGen	TTL	23	
ROW1		O	DigGen	TTL	24	
ROW2		O	DigGen	TTL	21	
ROW3		O	DigGen	TTL	22	
ROW4		O	DigGen	TTL	19	
ROW5		O	DigGen	TTL	20	
VR1	Brightness		ConB		27	
VR2	Brightness		ConB		28	
KONTR1	Contrast		ConB	-22.5 V ... -13.5 V	31	
KONTR2	Contrast		ConB		32	
PIO0	Led Data		DigGen	TTL	3	
PIO1	Led Remote		DigGen	TTL	4	
PIO2	Led Output		DigGen	TTL	5	

- continued -

- continued -						
name	Signal description	≡	source dest.	range	connector	comment
PIO3	Led LCD Off	I	DigGen	TTL	6	
Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power						

7.6.7 Adapter Board

Circuit diagram	1030.8806.01 S
Component location plan	1030.8806
Parts list	1030.8806.01 SA

7.6.7.1 Function

The Adapter Board is used for connection and signal conversion with the digital interfaces AES/EBU and OPTICAL. The optical input signals are converted to TTL level using the device X2 (TOSLINK-receiver), the output signals are generated by the device X1. The voltage supply of these devices is decoupled by means of an LC circuit for each of them.

The signals for the AES/EBU interface are only through-connected.

7.6.7.2 Measuring Equipment

Multimeter, current supply, optical cable

7.6.7.3 Troubleshooting

- AES/EBU: Continuity check
- S/P DIF: Continuity check
- OPTICAL:
 - Transmit: Apply 5 V (+ to X4.2, ground to X4.3)
Apply logic level 0 and 1 to X4.1
Check LED in TOSLINK device X1
 - Receive: Put transmitter into operation
Apply 5 V (+ to X4.5, ground to X4.6) (it may be the same current supply as with the transmitter)
Insert optical cable (system TOSLINK) between X1 and X2
Apply logic level 0 and 1 to X4.1
Check level at X4.4

7.6.7.4 Testing and Adjustment

Testing:

see Troubleshooting

Adjustment:

There is no need for an adjustment.

7.6.7.5 Disassembly and Assembly

After opening the instrument, disconnect the connections to the AES/EBU Option and loosen the front panel (see page 7.294) and tilt towards the front.

The Adapter Board can then be unscrewed.

7.6.7.6 External Interfaces

Connection to AES/EBU Board						
name	Signal description	≡	source dest.	range	connector	comment
GND		P	AESEBU		X4.1,4,6,9,13,16	
+ 5 V		I		+5V ±0.2V	X4.8,11	
Bal In	AES/EBU In	O		100mV _{pp} ... 10 V _{pp}	X4.14,15	max. 3.072 MHz
Unbal In	S/P DIF In,	I		100 mV... 5 V	X4.10	max. 3.072 MHz
Opt In		O		TTL	X4.12	
Bal Out	AES/EBU Out	O		100mV _{pp} ... 5 V _{pp}	X4.2,3	max. 3.072 MHz
Unbal Out	S/P Dif Out	O		100 mV... 2 V	X4.5	max. 3.072 MHz
Opt Out		O		TTL	X4.7	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Connections to front panel						
name	Signal description	≡	source dest.	range	connector	comment
GND		O			X24, X14	
GND1		O			X 20	
GND2		O			X 21	
GND3		O			X 10	
GND4		O			X 11	
GND		P	AESEBU		X4.1,4,6,9,13,16	
Bal In	AES/EBU In	I		100mV _{pp} ... 10 V _{pp}	X22, X23	max. 3.072 MHz
Unbal In	S/P DIF In,	I		100mV... 5V	X25	max. 3.072 MHz
Bal Out	AES/EBU Out	O		100mV _{pp} ... 5 V _{pp}	X12, X13	max. 3.072 MHz
Unbal Out	S/P DIF Out	O		100mV... 2V	X15	max. 3.072 MHz

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

AFTER SERIAL NUMBER 831 333, THE ADAPTER BOARD IS MODIFIED AS FOLLOWS:

Connection to AES/EBU board						
name	Signal description	≡	source dest.	range	connector	comment
AES/EBU	bal, max. 3.072 MHz	O	AESEBU	100mV _{pp} ... 10V _{pp}	X4.8,9	
GND	Shield	P	AESEBU		X4.7,10	
Opt In		O		TTL, max 3.072MHz	X4.4	
Opt Out		O		TTL, max 3.072MHz	X4.1	
GND		P	AESEBU		X4.3,6	
+ 5 V		I		+5V ±0.2V	X4.2,5	

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

Connections to front panel						
name	Signal description	≡	source dest.	range	connector	comment
OPT	Optical In	I			TOSLINK RX176	
OPT	Optical Out	O			TOSLINK TX176	
AES/EBU	Bal Out,	O		100mV _{pp} ... 10V _{pp}	X22, X23	max. 3.072 MHz

Explanation: ≡: I:Input, O:Output, B:Bidirectional, P:Power

7.6.8 Blower

1. Function

The blower of the UPD is a thermostat-controlled DC blower.

2. Measuring equipment

Voltmeter, hot-air blower

3. Troubleshooting

- Blower does not rotate: Check 12-V supply (red = +12V, blue = ground)
- Blower always runs slowly: Temperature sensor faulty or connection (green) interrupted.
- Blower always runs fast: Temperature sensor faulty or connection is shorted against ground.

4. Testing and Adjustment

Switch on instrument, blower runs slowly. Warm up temperature sensor, Blower must run faster.

5. Disassembly and Assembly

Disassembly:

Disconnect blower cable, loosen 2 screws on the upper frame, take out the mounting plate of the blower towards the top. Loosen 4 screws.

Assembly:

Fasten the blower on the mounting plate using 4 screws, paying attention to the screw locking. Install the mounting plate into the instrument (**caution: do not catch cables**), fasten using 2 screws, plug cable onto Connector Board.

7.6.9 Floppy-disk Drive

1. Function

The floppy-disk drive is an IBM-compatible 3.5" drive with a height of 1 inch and a recording capacity of 1.44 Mbytes.

The floppy-disk drive is addressed as drive 0 (=A:) because of the *cable twist* in the control cable, although it is set as drive 1 by jumpers. This is the standard setting with PC drives.

2. Measuring equipment

Voltmeter

3. Troubleshooting

Check the voltage supply (5V). For further troubleshooting, it is recommended to use the Checkit program.

4. Testing and Adjustment

For testing, it is recommended to use the Checkit program. In the event that it is not available, perform the following tests:

- Format an empty floppy disk with `format a: /u`
- Copy data to this floppy disk with `copy *.* a: /v`
- Use the copy protection of the floppy disk and try to delete data on the floppy disk by means of `del a:*.*`.

5. Disassembly and Assembly

Disassembly:

After opening the instrument and removing the bottom cover, disconnect the current supply cable and the 34-contact data cable from the drive. The drive is attached to a sheet support, which, in turn, is fastened with 2 Phillips screws each at the side and at the bottom. After loosening these screws, the sheet support can be pulled out of the guide towards the rear.

Assembly:

Mount the drive on the sheet support and install. Reconnect current supply and data cable, pay attention to the jumpers on the drive (see Function).

6. External Interfaces

34-contact flat cable to the Combi-Controller module

2-contact power cable to the Connector Board

7.6.10 Hard Disk

1. Function

The hard disk is an AT-bus drive, 3.5", 1 inch, recording capacity 40, 120 or 252 Mbytes.

The drive parameters are to be entered in the BIOS with type 47.

A larger drive may be installed in case of exchange.

2. Measuring equipment

Voltmeter

3. Troubleshooting

Check the voltage supply (5V, 12V). For further troubleshooting, it is recommended to use the Checkit program. *Strange* disturbances might be caused by virus.

If the harddisk LED is continuously on, the connector may be plugged with an offset.

4. Testing and Adjustment

For testing, it is recommended to use the Checkit program

In the event that it is not available, at least a coarse test can be carried out using `chkdsk c:.`

Important note: AT-bus hard disks must not be formatted physically (=low level format)!

Drive parameters (to be entered in the BIOS)						
Drive	Cyln	Head	WPcom	LZone	Sect	Size
CP3044	980	5	65535	982	17	41 MB
CP30104	762	8	0	0	39	116 MB
CP30254	895	10	0	0	55	240 MB
NEC	1024	16	0	0	63	504 MB

5. Disassembly and Assembly

Disassembly:

After opening the instrument and removing the bottom cover, disconnect the current supply cable and the 40-contact data cable from the drive. The drive is attached to a sheet support, which is mounted on the intermediate bottom by means of 4 screws. After loosening these screws, the sheet support can be pulled out of the guide at the side.

Assembly:

Reconnect current supply and data cable on the hard disk, then mount the hard disk on the support (inch screws!) and install it. Check the BIOS parameters.

Caution:

Calibration data are stored on the hard disk; they are also stored in the internal CMOS-RAM on the Digital Generator (see page 7.243). If the calibration data are not found on the hard disk when the UPD is started, they are restored using the contents of the CMOS RAM.

New Installation of DOS and UPD

DOS and UPD must be installed after the replacement of the hard disk:

- Partitionate the new hard disk with `FDISK`; reserve the whole disk for DOS (default setting). (`FDISK` is included in archive `DOS.LZH` on UPD system floppy)
- The disk must then be formatted with `FORMAT C:` as DOS drive.

- install DOS: insert UPD system floppy and boot.
- install BASIC (only if option UPD-K1 is installed): insert UPD-K1 floppy and run ACINST.
- install IEC: insert UPD IEC floppy and run IECINST.
- install UPD: insert UPD PROGRAM floppy and run UPDINST.

6. External Interfaces

40-contact flat cable to Combi-Controller module

4-contact power cable to Connector Board

7.6.11 Digital Power Supply

1. Function

The power supply identifies the AC supply voltage (100-120 V and 220-240 V) on switch-on and is automatically switched.

The minimum load is 1 A, the maximum load 20 A at the 5-V output.

If the minimum load is not achieved or the maximum load is exceeded, the power supply switches off. This status is indicated by a slight periodic (1 sec) whistling tone.

The power supply is provided with a thermal overload protection and *Remote Sensing*.

This module is not designed by R&S, but delivered by an external manufacturer. Since the manufacturer does not provide documents such as circuit diagrams or parts lists, repair is not possible.

In the case of a fault, the complete module is to be replaced. The replacement part has the number 1030.8393.98.

2. Measuring equipment

Voltmeter

3. Troubleshooting

Check the input voltage Check the output voltage Check the minimum load and the maximum load

4. Testing and Adjustment

Set the +5-V output voltage to 5.1 V using potentiometer V1. Potentiometer V1 is located directly next to the 5-V output and can be varied using a thin screwdriver through the cover. (Labelling: +5V ADJ).

Set the +12-V output voltage to 12.0 V using potentiometer V2. Potentiometer V2 is located next to V1 (labelling: +12V ADJ).

5. Disassembly and assembly

Open UPD, remove bracket above digital section. Remove all analog cards and unscrew cover above the digital power supply (6 screws). Disconnect grounding cable and take out the power supply towards the top.

For replacing the power supply, proceed in the reverse order.

6. External Interfaces

Cable tree for Connector Board and Digital Motherboard

Power cable